

## Features

- CMOS or LVCMOS Control Logic
- Negative output voltage for GaAs Gate Drive
- 6-bit Serial/Parallel Driver for Attenuator or Phase Shifter Control
- T/R Switch and Amplifier Controls
- Low Power Dissipation
- Lead-Free 5mm PQFN-40LD Plastic Package
- RoHS\* Compliant and 260°C Reflow Compatible

## Description

The MADR-010410 is a dedicated CMOS driver for multifunction modules such as GaAs based Transmit/Receive Modules. The driver translates CMOS/LVCMOS input controls to negative gate control voltages for GaAs FETs.

The driver includes a 6-bit serial/parallel interface designed to drive digital attenuators and/or phase shifters as well as functionality to switch between transmit and receive channels allowing the ability to enable/disable LNAs or PAs. High speed analog CMOS technology is utilized to achieve low power consumption at moderate to high speeds.

## Ordering Information<sup>1</sup>

| Part Number        | Package        |
|--------------------|----------------|
| MADR-010410-000100 | Bulk Packaging |
| MADR-010410-TR0500 | 500 piece reel |

1. Reference Application Note M513 for reel size information.

## Pin Configuration

| Pin No. | Function        | Pin No. | Function |
|---------|-----------------|---------|----------|
| 1       | B2              | 21      | NC       |
| 2       | A2              | 22      | NC       |
| 3       | B1              | 23      | NC       |
| 4       | A1              | 24      | NC       |
| 5       | V <sub>EE</sub> | 25      | GND      |
| 6       | V <sub>CC</sub> | 26      | NC       |
| 7       | S/P             | 27      | P2       |
| 8       | NC              | 28      | P1       |
| 9       | NC              | 29      | L2       |
| 10      | NC              | 30      | L1       |
| 11      | C1/SER IN       | 31      | B7       |
| 12      | C2/CLK          | 32      | A7       |
| 13      | C3/LE           | 33      | B6       |
| 14      | C4              | 34      | A6       |
| 15      | C5              | 35      | B5       |
| 16      | C6              | 36      | A5       |
| 17      | TR              | 37      | B4       |
| 18      | ENABLE          | 38      | A4       |
| 19      | SER OUT         | 39      | B3       |
| 20      | NC              | 40      | A3       |

## Handling Procedures

Please observe the following precautions to avoid damage:

## Static Sensitivity

Silicon Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

<sup>1</sup> \* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

**Module Driver**  
**6-bit Serial/Parallel, Transmit/Receive**

Rev. V2

**Guaranteed Operating Ranges** <sup>2,3,4</sup>

| Parameter                  | Unit | Min. | Typ. | Max. |
|----------------------------|------|------|------|------|
| Positive DC Supply Voltage | V    | 3.0  | 5.0  | 5.5  |
| Negative DC Supply Voltage | V    | -5.5 | -5.0 | -3.0 |
| Operating Temperature      | °C   | -40  | +25  | +125 |

2. Unused logic inputs must be tied to either GND or  $V_{CC}$ .
3. All voltages are relative to GND.
4. 0.01  $\mu$ F decoupling capacitors are required on the power supply lines.

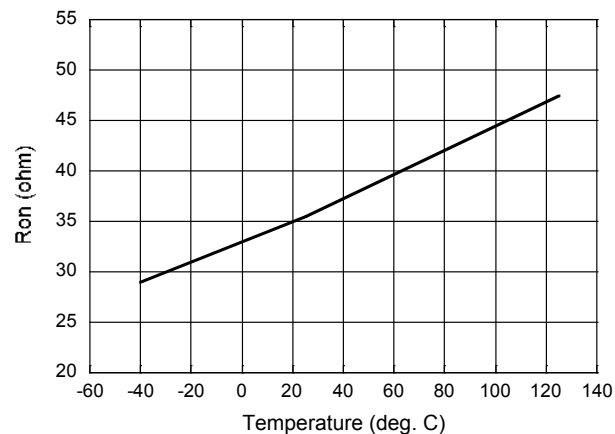
**DC Characteristics over Guaranteed Operating Range**

| Parameter                              | Test Conditions                               | Unit     | Min.                | Typ.           | Max.                |
|--|---|----------|---------------------|----------------|---------------------|
| Input High Voltage                     | Guaranteed High Input Voltage                 | V        | $0.7 \times V_{CC}$ | $V_{CC}$       | $V_{CC}$            |
| Input Low Voltage                      | Guaranteed Low Input Voltage                  | V        | GND                 | GND            | $0.3 \times V_{CC}$ |
| Output High Voltage (An or Bn)         | $I_{OH} = -250 \mu A$                         | V        | —                   | -0.1           | —                   |
| Output Low Voltage (An or Bn)          | $I_{OL} = 250 \mu A$                          | V        | —                   | $V_{EE} + 0.1$ | —                   |
| DC Output Current—High (per Output)    | $V_{EE} = -5.0V$                              | mA       | -1                  | —              | —                   |
| DC Output Current—Low (per Output)     | $V_{EE} = -5.0V$                              | mA       | —                   | —              | 1                   |
| Output High for Serial Out             | $I_{OH} = -100 \mu A$                         | V        | $V_{CC} - 0.2$      | —              | $V_{CC}$            |
| Output Low for Serial Out              | $I_{OL} = 100 \mu A$                          | V        | GND                 | —              | 0.2                 |
| Output Current High for Serial Out     | $V_{CC} = 5.0V, V_{EE} = -5.0V$               | mA       | -1                  | —              | —                   |
| Output Current Low for Serial Out      | $V_{CC} = 5.0V, V_{EE} = -5.0V$               | mA       | —                   | —              | 1                   |
| Quiescent Supply Current               | $V_{IN} = GND$ or $V_{CC}$ , No Output Load   | $\mu A$  | —                   | 0.1            | 5                   |
| Quiescent Supply Current               | $V_{IN} = GND$ or $V_{EE}$ , No Output Load   | $\mu A$  | —                   | 0.1            | 5                   |
| Input Leakage Current                  | $V_{IN} = GND$ or $V_{CC}$                    | $\mu A$  | -1                  | —              | 1                   |
| L,P Ports Open-Drain Output Resistance | $V_{EE} = -5.0V$ or $-3.0V, I_{SINK} = 0.5mA$ | $\Omega$ | —                   | 40             | 200                 |

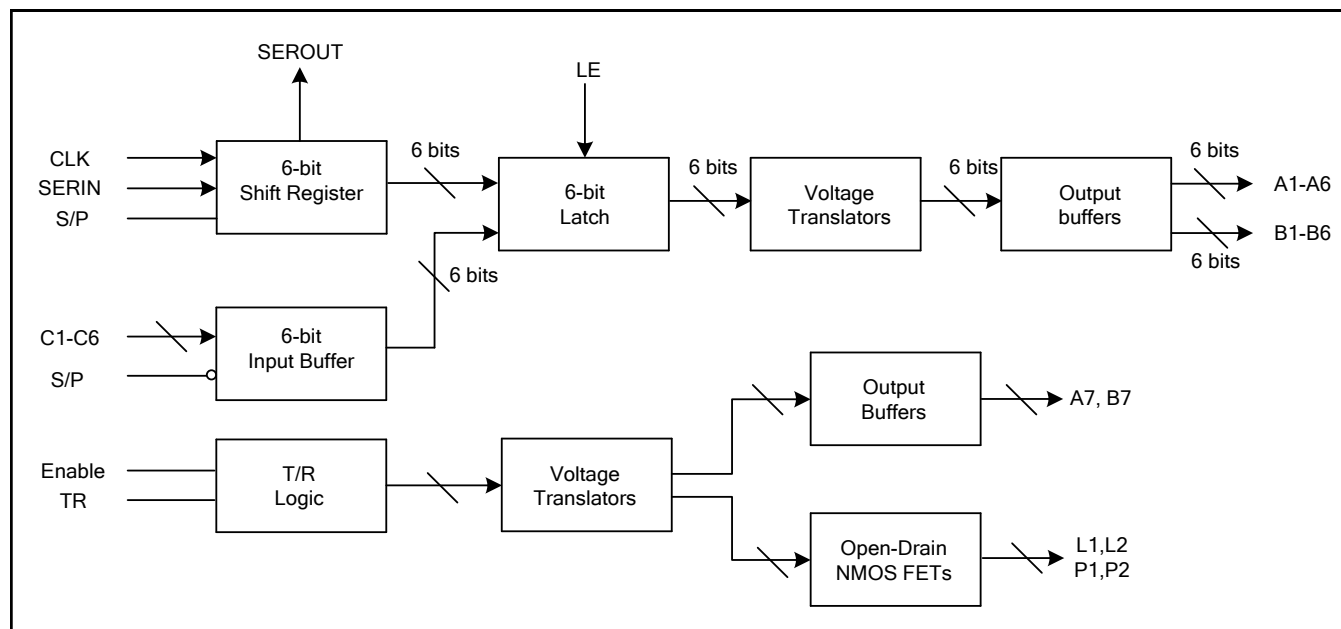
## Absolute Maximum Ratings

| Parameter                  | Unit | Min            | Max |
|----------------------------|------|----------------|-----|
| DC Supply Voltage Positive | V    | -0.5           | 7.0 |
| DC Supply Voltage Negative | V    | -7.0           | 0.5 |
| DC Input Voltage           | V    | $V_{CC} - 0.5$ | 7.0 |
| Operating Temperature      | °C   | -55            | 125 |
| Storage Temperature        | °C   | -65            | 150 |
| ESD Sensitivity            | kV   | 2              | —   |

## Ln/Pn Output On Resistance



## Function Diagram



## Functionality

### 6-bit Serial/Parallel Driver

The 6-bit serial/parallel driver consists of C1-C6 (shared inputs), S/P (mode control), A1 to A6 (in phase outputs), B1 to B6 (complementary outputs), and SerOut.

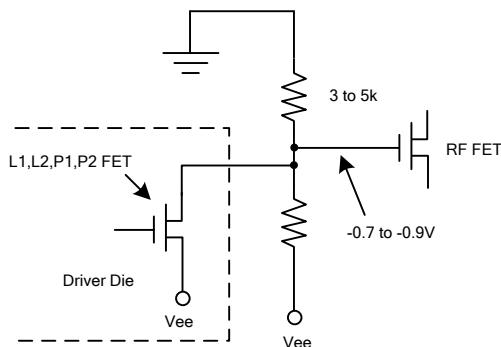
The serial control interface (SERIN, CLK, LE, SE-ROUT) is compatible with SPI protocol. It is activated when S/P is kept high. The 6-bit serial word must be loaded with MSB first. When LE is high, 6-bit data in the serial input register will be transferred to complementary An and Bn outputs. CLK will be masked to prevent data transition during output loading. SEROUT is the SERIN delayed by 6 clock cycles.

The parallel mode is enabled when S/P is set to low. In the parallel mode, the outputs are controlled by the parallel control inputs (C1 to C6) directly.

### T/R Control

The A7 and B7 outputs are designed to drive the SP2T switch(es) in the T/R module, which switch the T/R module between transmit and receive modes.

The combination of TR and Enable inputs will be able to turn on/off the T/R module receive path LNAs and transmit path PAs. Inside L and P outputs are open-drain NMOS FETs. When they are turned on, they will pull down the gate of the GaAs FETs in the amplifiers to shut them down. See Figure 1 for the application circuit.



4 Figure 1. Application Circuit for T/R Amplifiers Control

### Mode Truth Table

| S/P | LE  | Mode            |
|-----|-----|-----------------|
| 1   | X   | Serial          |
| 0   | N/A | Direct Parallel |

### Parallel Mode Truth Table

| INPUTs<br>C1-C6 | OUTPUTS         |                 |
|-----------------|-----------------|-----------------|
|                 | A1-A6           | B1-B6           |
| 0               | V <sub>EE</sub> | GND             |
| 1               | GND             | V <sub>EE</sub> |

### T/R Logic Truth Table

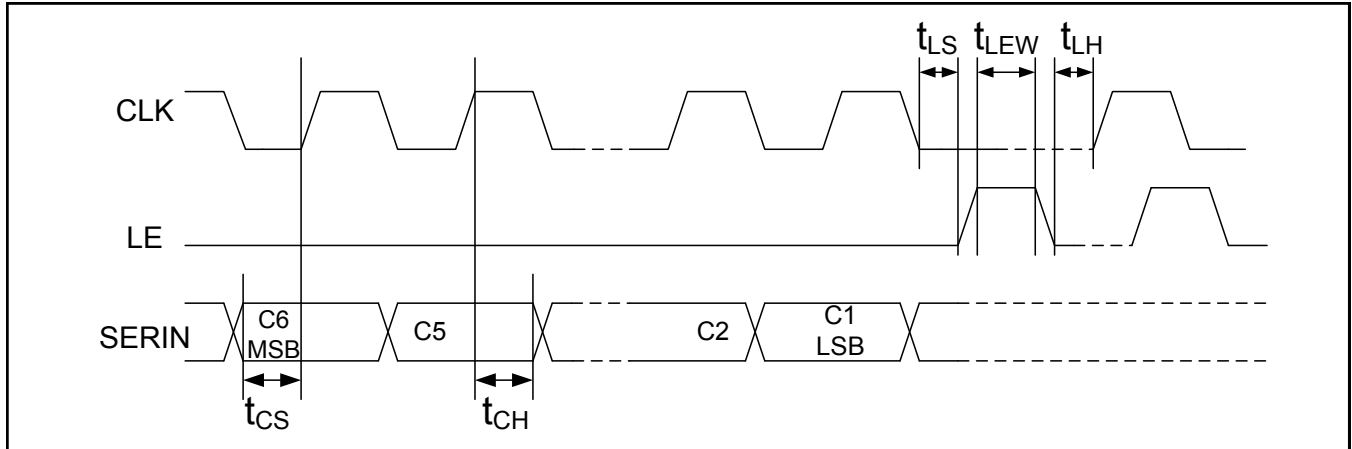
| INPUTS |    | OUTPUTS         |                 |        |        |
|--------|----|-----------------|-----------------|--------|--------|
| Enable | TR | A7              | B7              | L1, L2 | P1, P2 |
| 0      | 1  | GND             | V <sub>EE</sub> | Hi Z   | Hi Z   |
| 0      | 0  | V <sub>EE</sub> | GND             | Hi Z   | Hi Z   |
| 1      | 1  | GND             | V <sub>EE</sub> | Hi Z   | Low    |
| 1      | 0  | V <sub>EE</sub> | GND             | Low    | Hi Z   |

Where:

“Low” means that the NMOS FET is on (pulls the gate to approximately V<sub>EE</sub> + 0.2V).

“Hi Z” means that the open-drain NMOS FET is shut down and shows a high impedance.

## Serial Interface Timing Diagram



## Serial Interface Timing Characteristics

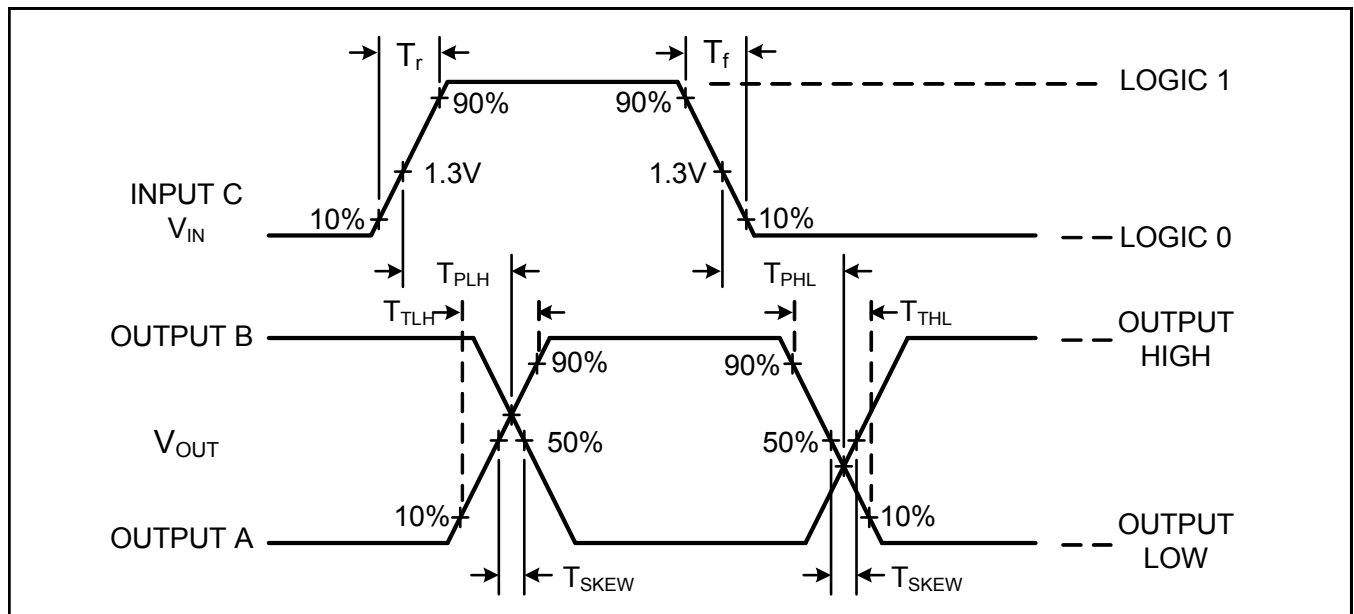
| Symbol    | Parameter                     | Unit | Typical performance |       |        |
|-----------|-------------------------------|------|---------------------|-------|--------|
|           |                               |      | -40°C               | +25°C | +125°C |
| $t_{CKH}$ | Min. Serial Clock HIGH Period | ns   | 50                  | 50    | 50     |
| $t_{CKL}$ | Min. Serial Clock LOW Time    | ns   | 50                  | 50    | 50     |
| $t_{CS}$  | Min. Control Set-up Time      | ns   | 20                  | 20    | 20     |
| $t_{CH}$  | Min. Control Hold Time        | ns   | 20                  | 20    | 20     |
| $t_{LS}$  | Min. LE Set-up Time           | ns   | 20                  | 20    | 20     |
| $t_{LEW}$ | Min. LE Pulse Width           | ns   | 20                  | 20    | 20     |
| $t_{LH}$  | Min. LE Hold Time             | ns   | 20                  | 20    | 20     |

## Parallel Interface Characteristics Over Guaranteed Operating Range<sup>5</sup>

| Symbol     | Parameter                             | Unit | Typical performance |       |        |
|------------|---------------------------------------|------|---------------------|-------|--------|
|            |                                       |      | -40°C               | +25°C | +125°C |
| $T_{PLH}$  | Propagation Delay                     | ns   | 22                  | 24    | 28     |
| $T_{PHL}$  | Propagation Delay                     | ns   | 22                  | 24    | 28     |
| $T_{TLH}$  | Output Transition Time (Rising Edge)  | ns   | 6                   | 7     | 8      |
| $T_{THL}$  | Output Transition Time (Falling Edge) | ns   | 4                   | 5     | 6      |
| $T_{skew}$ | Delay Skew                            | ns   | 1                   | 1     | 1      |

5.  $V_{CC} = 3.0V$ ,  $V_{EE} = -3.0V$ ,  $C_L = 2\text{ pF}$ , input LOGIC1 = 3V, LOGIC0 = 0V,  $T_{rise}$ ,  $T_{fall} = 6\text{ ns}$ .

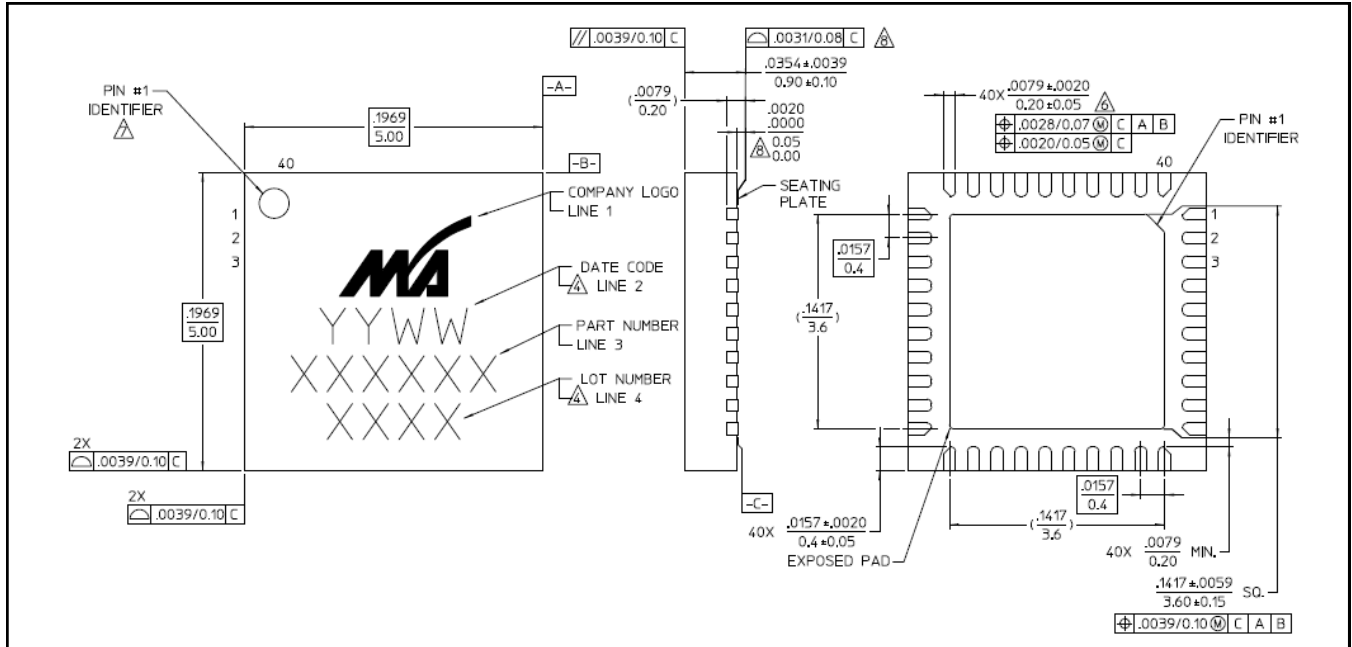
### Switching Waveforms



## Module Driver 6-bit Serial/Parallel, Transmit/Receive

Rev. V2

Lead-Free, 5mm QFN-40LD<sup>†</sup>



<sup>†</sup> Reference Application Note M538 for lead-free solder reflow recommendations.  
Plating is 100% matte tin over copper.  
Meets JEDEC moisture sensitivity level 3 requirements.

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