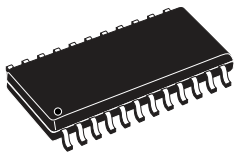
L5951

Triple output multifunction voltage regulator for car radio with IDR/class2 interface

Datasheet - production data



SO-24

Features

- 3 voltage regulators:
  - 3.3 V (100 mA) standby regulator
  - 5 V (100 mA) stand-by regulator
  - 7.8 V (100 mA)
- Out of regulation detection for 5 V standby regulator
- Wide operating supply voltage range from 4.5 V up to 26.5 V for transient 34 V
- Very low standby quiescent current (<150 µA)
- Input to output signal transfer function programmable
- LVS function
- TTL and CMOS compatible inputs
- Output current limitation
- Controlled output slope for low EMI
- Overtemperature shut-down
- Able to survive under loss of ground or battery
- ESD protected

Description

The L5951 is a monolithic triple regulator integrated with a SAE J1850 Integrated Driver / Receiver realized in advanced Multipower-BCD technology. It is intended to drive single wire J1850 communications, and offer microcontroller power and power management for automotive or industrial applications.

Table 1. Device summary

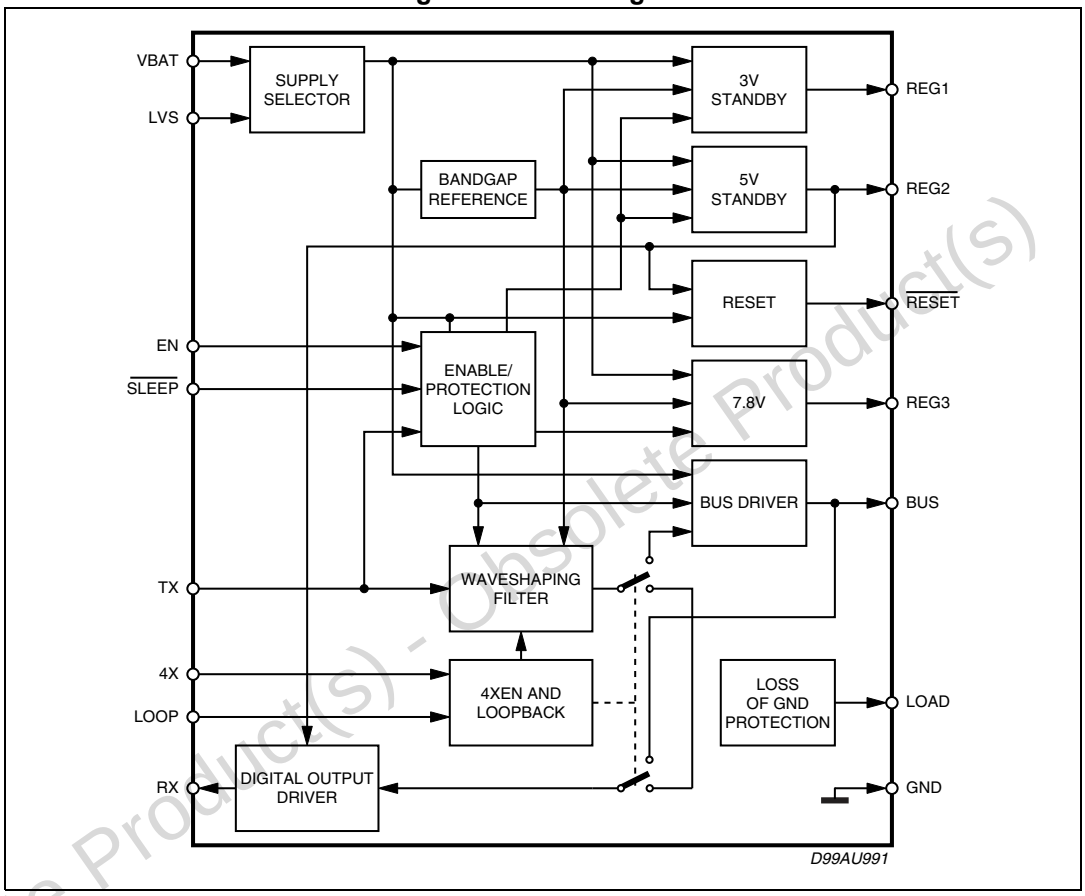
Order code	Package	Packing
L5951	SO-24	Tube

Contents

1 Block diagram and pins description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pins description

Figure 2. Pins connection (top of view)

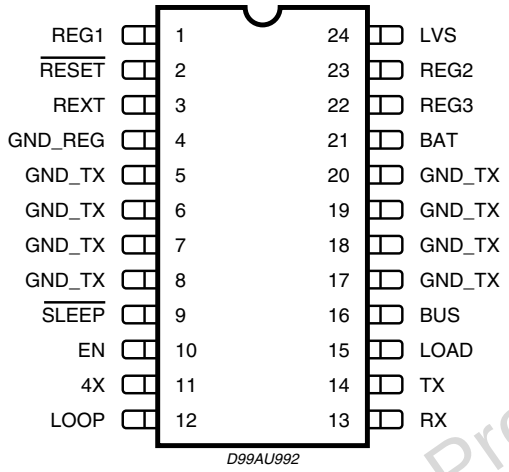


Table 2. Pins function

N.	Name	Function
1	REG1	Regulator #1
2	Reset (1)	Reset Output to µC
3	Rext	Waveshaping Resistor
4	GND_REG	Regulator Ground
,6,7,8,17,18,19,20	GND_TX	Transceiver Ground
9	Sleep(1)	Transceiver Enable Input
0	EN	Enable for Regulator #3
11	4X	4XBus mode (41.6K Baud)
12	LOOP	Loopback Enable
13	RX	Serial Data Output to mC
14	TX	Serial Data Input from mC
15	Load	External Pull Down to Gnd
16	Bus	Bus Output to Vehicle
21	Bat	Battery Supply
22	REG3	Regulator #3
23	REG2	Regulator #2
24	LVS	Low Voltage Supply

1. Denotes active low for sleep and reset.

2 Functional description

2.1 General features

The L5951 is an integrated circuit which provides a J1850 physical layer as well three voltage regulators. The L5951 was developed to provide the power and Class 2/IDR interface for a microcontroller.

2.2 REG1 output voltage

The REG1 regulator output is equal to 3.3V. The 3.3V regulator is non low drop out and can handle currents up to 100mA with short circuit limit of 280mA.

2.3 REG2 output voltage

The REG2 regulator output is equal to 5V and can handle currents up to 100mA with short circuit limit of 280mA. The output stage of the 5V regulator is low dropout.

2.4 REG3 output voltage

The REG3 regulator output is equal to 7.8 V and can handle currents up to 100mA with short circuit limit of 280 mA. The output stage of the 7.8 V regulator is low dropout. REG3 regulator is controlled by the EN (enable) pin of the IC. REG3 can be turned on and off by toggling the EN pin. A logic "1" on the EN pin enables REG3, while a logic "0" on the EN pin disables REG3. The maximum voltage when REG3 is off must be less than 0.2 V.

Sleep[a] **Input -** The Class 2 transmitter can be turned on and turned off by the Sleep* pin. Once the voltage level is above 2VDC, the transmitter is enabled. If the Sleep* pin drops below 0.8 VDC, and EN is "0" the transceiver goes into a low power mode. In low power mode, REG3 and the transceiver are disabled. The L5951 will still receive messages and send them to the microcontroller out of the RX pin.

LVS input - Reg1 and Reg2 are supplied by Vbat pin. The device could then dissipate a lot of power, causing thermal shutdown at high voltage. For this reason a secondary low voltage supply (LVS) can be used to reduce power dissipation.

Reset[a] **Output -** The L5951 has low voltage or no voltage circuitry that is a warning to the microcontroller. If REG2 drops 0.3 VDC below its normal operating voltage, the Reset[a] pin will go to a logic "0". Between the voltage levels of 4.65 VDC (min) and 5.10 VDC (max) on REG2, a reset will occur. There is a hysteresis of 50mV on the Reset[a] pin.

Low Input Voltage Operation - If battery voltage level drops below 7.0V, the outputs are to remain alive and ready for the return of normal voltage battery levels. The L5951 will be able to retrieve data off the BUS and send it to the microprocessor when the supply voltage is as low as 4.9 V. The regulators should stay the same voltage as the battery voltage down to 7.0 V minus operating headroom for the 7.8 V regulator. BUS $V_{OH,min}$ are not guaranteed over all conditions below VBAT = 9.0 V.

a. denotes active low

Waveshaping - Messages sent by the microcontroller to the transceiver are routed to a waveshaping circuit. The digital signal is rounded at the switching points in order to reduce EMI emissions. A second order function, I = C*dV/dt, is used to control the rise and fall times of the transmission. The rise and fall times are controlled by an external resistor Rext. The waveshaping circuit can be enabled and disabled by the 4X pin. A logic "1" will disable the waveshape circuit and a logic "0" will enable the waveshape circuit. In 4X mode, the speed of the BUS is increased by a factor of four. Any signal coming from the microcontroller and going to the BUS must be waveshaped. If loopback (LOOP) is enabled, the signal coming from the micro through the TX pin is routed to the RX pin back to the micro with or without it being waveshaped. A logic "1" enables loopback and a logic "0" disables loopback.

Nodes - The transmitter provides a wave-shaped 0 to 7.7 VDC waveform on the BUS output. It also receives waveforms and transmits a digital level signal back to a logic IC. The transmitter can drive up to 32 remote transceivers. These remote nodes may be at ground potentials that are ±2 VDC, with respect to the assembly. Under this condition, waveshaping will only be maintained during 3 of the 4 corners. The L5951 is a remote node on the Class 2/IDR Bus. Each remote transceiver has a 470 + 10% pF capacitor on its output for EMI suppression, as well as a 10.6 kΩ + 5% pull down resistor to ground. The main node has a 3.300 + 10% pF capacitor on its output for EMI suppression, as well as a 1.5 kΩ + 5% pull down resistor to ground. With more than 26 nodes there is no primary node, all nodes will have the 470 ±10% pF capacitor and the 10.6kΩ ±5% pull down resistor. No matter how many remote nodes are on the Class 2/IDR Bus, the RC of the Class 2/IDR Bus is maintained at approximately 5ms. The minimum and maximum load on the Class 2/IDR Bus is given below:

Table 3. Minimum and maximum load on the Class 2/IDR Bus

	Capacitance	Resistance to ground
Minimum Nodes	(3.33 · .9) + (.47 · .9) = 3.39 nF	(1.5 · 1.05) || (10.6 · 1.05) = 1.38 kΩ
Maximum Nodes	(3.3 · 1.1) + 25·(0.47 · 1.1) = 16.55 nF	(1.5 · 0.95) || (10.6 · 0.95) / 25 = 314Ω

2.5 Protection

The L5951 can survive under the following conditions: shorting the outputs to BAT and GND, loss of BAT, loss of IC GND, double battery(+26.5V), 4000V ESD, 34V load dump. L5951 will not handle a reverse battery condition. External components must be implemented for reverse battery protection.

Thermal Shutdown: thermal shutdown is broken down into two areas; V1 and V2 pouts, and the other is V3 output and the Class 2 Bus Driver. V1 and V2 outputs shutdown at 160°C and returns to normal operation at 130°C. The V3 output and Class 2 Bus Driver shutdown at 150°C and return to normal operation at 120°C.

Current Limiting: each voltage regulator will contain its own current protection, and the maximum allowable current for all three regulators is 280mA.

Short Circuit: If the outputs are short circuited, the IC will begin current limiting and eventually the thermal shutdown will kick in. Current limiting will not disable the outputs.

Overvoltage: The IC will not operate if the BAT voltage reaches 30V or above. V1 and V2 will not be shutdown, but all other outputs will not operate.

Loss of Ground & Loss of Battery Connection: in this conditions a very small leakage on BUS is generated.

2.6 Protocol description

The L5951 uses a Variable Pulse Width (VPW) modulated protocol. One frame consists of an entire message not containing more than 12 bytes. The first bit of each byte will be the most significant bit (MSB). A transmitted message begins with a SOF signal and ends with the EOF signal.

The data to be transmitted has to be in a specific format as follows:

idle, SOF, DATA, CRC, EOD, NB, IFR, EOF, IFS, idle

Definitions below:

idle:	Logic level low on communication bus
SOF:	Start of Frame
DATA:	Data Bytes
CRC:	Cyclic Redundancy Check Error Detection Byte
EOD:	End of DATA (only when IFR is used)
NB:	Normalization Bit
IFR:	In-Frame Response Byte(s)
EOF:	End of Frame
IFS:	Inter-Frame Separation
BRK:	Break (can occur on network at any time)

Idle - Logic level low on bus any time after IFS.

Start of Frame (SOF) - The SOF signals the receiver that a new frame is beginning. SOF signal is a logic level high pulse identified by a pulse width of about t = 200 µs.

DATA - Total number of bytes that can be transmitted (from SOF to EOF) is 12 bytes.

Cyclic Redundancy Check (CRC) - A method for determining if the message received is the same as the message transmitted. If an invalid CRC number is detected, then an error will be detected. The SOF signal is not used to determine the CRC. All bits in the CRC are initially "ones" to avoid confusion with a data stream that are all "zeros".

End of Data (EOD) - Used to signal the receiver about the end of data transmission. If there is a IRF signal, the sender of the frame will expect one or more bytes in the IFR following the EOD. If there is no IFR used, then the bus would stay in a logic level low state resulting in a EOF. EOD signal is recognized by a logic level low pulse for a duration of about 200 µs.

Normalization Bit (NB) - The sole reason for the NB is to define the start of the in-frame response. The first bit the IFR is passive, therefore it is necessary to have a signal that follows EOD. There are two forms to the NB. First of all, the NB is a logic level high pulse. The two forms are distinguished by their pulse widths. The first form has a pulse width of about 64 µs and indicates if the IFR contains a CRC or not. The second form has a longer pulse width of about 128 µs and also indicates if there is a CRC in the IFR or not. The manufacturer can manipulate the NB to any of the two methods.

In-Frame Response (IFR) - Response bytes are sent by the receiver of the transmission and start after the EOD. If the IFR stays at a logic level low for a period of time then the frame must be considered to be complete. IFR bytes can be used to send a signal back to the originator indicating the correct CRC number to confirm the correct message was sent.

End of Frame (EOF) - Indicates the end of a frame. Once the last byte is transmitted, the bus will be in a logic level low state for a period of time indicating the end of the frame. EOF signal is recognized by a low pulse for a width of about 280 µs.

Inter-Frame Separation (IFS) - IFS is used to synchronize the receivers at various nodes.

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	DC operating supply voltage	-0.6 to 26.5	V
V_{DIAG}	Diagnostic output voltage	-0.6 to 5.5	V
V_{IN}	Input control voltage (EN, $\overline{Sleep}$, 4X, Loop, TX)	-0.6 to 5.5	V
V_{OUT}	Output control voltage (Reset [1])	-0.3 to 5.5	V
V_S	Peak supply voltage t = 50ms	34	V
T_{op}	Operating temperature range	-40 to 85	°C
T_{stg}	Storage temperature range	-40 to 150	°C

1. Denotes active low.

3.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction-to-ambient [1]	50	°C/W

1. With 6cm^2 on board heat sink area.

3.3 Electrical characteristics

T_{amb} = 25 °C, V_{BAT} = 14.4 V unless otherwise specified. Standard Loads: I_{REG1} = 0.5 mA, I_{REG2} = 0.5 mA, I_{REG3} = 5 mA.

Table 6. Electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$I_{q,ST\text{-}BY}$	Standby quiescent current	EN, Sleep* = 0V, V_{BAT} = 14V, I_{REG2} = 50mA, I_{REG1} = 50mA EN, Sleep* = 0V, V_{BAT} = 14V, I_{REG2} = 500µA, I_{REG1} = 250mA		350 110		µA µA
	Maximum quiescent current - V_{BAT}	V_{BAT} = 14V, I_{REG1} = 100mA, I_{REG2} = 100mA, I_{REG3} = 100mA, I_{BUS} = 30mA LVS = 0V LVS = 10V		10 10.5		mA mA
	Maximum quiescent current - LVS	V_{BAT} = 14V, I_{REG1} = 100mA, I_{REG2} = 100mA, I_{REG3} = 100mA, I_{BUS} = 30mA LVS = 10V		750		µA

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	EN switch input current	V_{BAT} = 14V, EN ≥ 2 V V_{BAT} = 14V, EN ≥ 0.8 V		0 0		µA µA
$V_{ENL, ENH}$	EN input threshold voltage	V_{BAT} = 14V, VIL V_{BAT} = 14V, VIH	 2		0.8	V
$V_{RES, L}$	Reset(1) output low voltage	Set V_{BAT} so V_{REG2} drops 0.30 V	0	0.02	0.4	V
V_{RES}	Reset(1) output voltage threshold	Decrease V_{BAT}so V_{REG2} drops until Reset(1) drops		V_{REG2} - 0.20		V
$V_{RES, HYS}$	Reset threshold hysteresis			50		mV
3.3V/100mA DC characteristics for regulator output 1						
V_{REG1}	Output voltage	I_{REG1} =100mA	3.14	3.3	3.46	V
ΔV_{line}	Line regulation	7 V ≤ V_{BAT} ≤ 26 V (Measure ΔV_{REG1} Across V_{BAT} Range)		7	15	mV
ΔV_{load}	Load regulation	0.5mA ≤ I_{REG1} ≤ 100mA (Measure ΔV_{REG1} across V_{LOAD} range)		8	50	mV
$V_{DROPOUT}$	Dropout voltage (Measure V_{BAT} - V_{REG1} when V_{REG1} drops 0.1V)	I_{REG1} = 100mA I_{REG1} = 5mA		1 0.12	2.2 1.5	V V
I_{lim1}	Current limit			200		mA
SVR1	Reg1 supply voltage rejection	I_{REG1} = I_{REG2} = I_{REG3} = 50mA f = 20 to 20kHz V_{BAT} = 14Vdc, 1Vac,pp		45		dB
5V/100mA regulator output 2						
V_{REG2}	Output voltage	I_{REG2} =100mA	4.75	5	5.25	V
ΔV_{line}	Line regulation	7V ≤ V_{BAT} ≤ 26V (Measure ΔV_{REG2} across V_{BAT} range)		6	40	mV
ΔV_{load}	Load regulation	0.5mA ≤ I_{REG2} ≤ 100mA (Measure ΔV_{REG2} across V_{LOAD} range)		14	100	mV
$V_{DROPOUT}$	Dropout voltage (Measure V_{BAT} - V_{REG2} when V_{REG2} drops 0.1V)	I_{REG2} =100mA I_{REG2} =5mA		450 22		mV mV
I_{lim2}	Current limit			200		mA
SVR2	Reg2 supply voltage rejection	I_{REG1} = I_{REG2} = I_{REG3} = 50mA f = 20 to 20kHz V_{BAT} = 14Vdc, 1Vac,pp		45		dB

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
7.8V/100mA regulator output 3						
V_{REG3}	Output voltage	I_{REG3} =100mA - 8.8V ≤ V_{BAT} ≤ range	7.60	7.8	8	V
DV_{line}	Line regulation	8.8V ≤ V_{BAT} ≤ 26V (Measure ΔV_{REG3} across V_{BAT} range)			50	mV
DV_{load}	Load regulation	5mA ≤ I_{REG3} ≤ 100mA (Measure ΔV_{REG3} across V_{LOAD} range)			50	mV
$V_{DROPOUT}$	Dropout voltage (Measure V_{BAT} - V_{REG3} when V_{REG3} drops 0.1V)	I_{REG3} = 100mA I_{REG3} = 5mA		0.5 0.04		V V
I_{lim3}	Current limit			200		mA
SVR3	Reg3 supply voltage rejection	I_{REG1} = I_{REG2} = I_{REG3} = 50mA f = 20 to 20kHz V_{BAT} = 14Vdc, 1Vac,pp		45		dB
DC characteristics for class 2 transceiver (Standard loads: I_{REG1} = 0.5mA, I_{REG2} = 0.5mA, I_{REG3} = 5mA)						
BUS_{ih} BUS_{il}	BUS guaranteed Input voltages	Verify RX > 3 VDC Verify RX < 3 VDC	4.25	3.7	3.50	V V
BUS_{Hyst}	BUS hysteresis	BUS_{ltoh} - BUS_{hhtol}		0.15		V
BUSov	BUS output voltage	TX = 5 VDC, BUS = 257 to 1380Ω to gnd V_{BAT} - 8.2 to 16 VDC V_{BAT} - 6.0 to 8.2 VDC TX = 0V		7.2 5		V V
$I_{BUSshort}$	BUS short circuit current	TX = 5VDC BUS = -2 to 4.8VDC		170		mA
$I_{BUSleak}$	BUS leakage current	BUS = -2 to 0 VDC BUS = 0 to V_{BAT}		0 0		mA mA
$LOAD_{ON}$	Load output	I_{LOAD} = 6mA		0.045		V
$LOAD_{Dio}$	Load output (unpowered)	V_{BAT} = 0V, I_{LOAD} = 6mA		0.7		V
$I_{BUSloss}$ $I_{LOADloss}$	BUS & LOAD current during loss of assembly V_{BAT} or GND	I_{VBAT} = 0mA, BUS = -18 to 9VDC LOAD = -18 to 0 VDC		11 39		µA µA
TX_{VIL} TX_{VIH}	TX input voltage	Verify BUS < 3.875VDC Verify BUS > 3.875VDC	2		0.8	V V
I_{TXVIL} I_{TXVIH}	TX input current	TX = 5VDC TX = 0VDC		110 0		µA µA
4_{Trip1} 4_{Trip2}	4X input trip point voltages	Normal Mode 4X Mode		1.4		V

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{4Xvih} I_{4Xvil}	4X input current	4X = 5 VDC 4X = 0 VDC		0 0		µA µA
L_{Trip1} L_{Trip2}	LOOP input trip point voltages	Normal Mode Loopback Mode	2		0.8	V V
I_{Lvih} I_{Lvil}	LOOP input current	LOOP = 5VDC LOOP = 0VDC		0		µA
V_{RXhigh}	RX output voltage, high	BUS = 7V, I_{RX} = -200µA		4.85		V
V_{RXlow}	RX output voltage, low	BUS = 0V, I_{RX} = 1.6mA		0.2		V
I_{RX}	RX output current	RX = high (Short circuit protection limits)		5		mA
V_{IH} V_{IL}	Sleep(1) input voltage	TX = 5VDC Verify BUS > 3.725 Verify BUS < 4.025	2		 0.8	 V V
$I_{Sleepvih}$ $I_{Sleepvil}$	Sleep(1) input current	Sleep* = 5VDC Sleep* = 0VDC		0.2 0		µA µA
AC characteristics for class 2 transceiver (Standard loads: IREG1 = 0.5mA, IREG2 = 0.5mA, IREG3 = 5mA)						
BUS_{LTOH}	BUS voltage rise times	TX = 7.812Hz square wave See Figure 1 Min and max loaded BUS		 15		 µs
BUS_{HTOL}	BUS voltage fall times	TX = 7.812Hz square wave See Figure 1 Min and max loaded BUS		 14		 µs
t_{Wbus}	BUS pulse width distortion	TX = 7.812Hz square wave See Figure 2 Load BUS with 3.300pF and 1.38kΩ Measure @ 1.5V levels Measure @ 6.25V levels		 77 48		 µs µs
V1 V2	Spectral content limit (Measure spectral peak from 0.53MHz to 1.6MHz)	V_{BAT} = 9V to 16V, no ground offset, 0.53 ≤ f ≤ 1MHz. V_{BAT} = 9V to 16V, no ground offset, 1 ≤ f ≤ 1.67MHz.		100 80		µV µV
BUS_{DLY}	Propagation delay	Measure delay between TX trip point and RX trip point		16		µs
TX_{4XDLY} $TX_{NormDLY}$	TX to BUS delay	Measure from 2.5V on TX to 3.875V on BUS 4X mode Normal mode		 3.5 14.5		 µs µs

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$RX_{LTOHdly}$ $RX_{HTOLdly}$	RX output delay time	See Figure 4 Measured from BUS threshold voltage		1.5 1.9		µs µs
RX_{LTOH} RX_{HTOL}	RX output transition time	Load RX with 50pF to ground See Figure 5		170 70		ns ns
RX_{LTOH} RX_{HTOL}	RX output transition time during sleep state	Load RX with 50pF to ground See Figure 5, Sleep(1) = 0VDC		170 70		ns ns

1. Denotes active low.

3.4 BUS timing diagrams

Figure 3. BUS rise and fall times

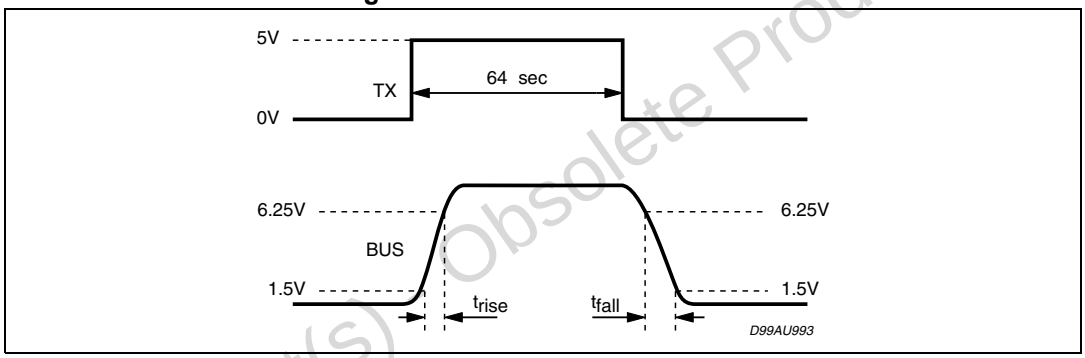


Figure 4. BUS pulse width distortion

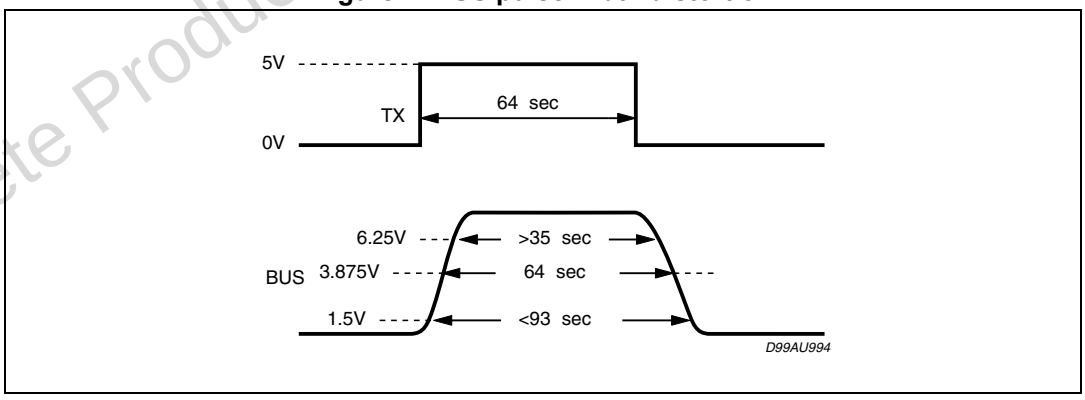


Figure 5. BUS output voltage

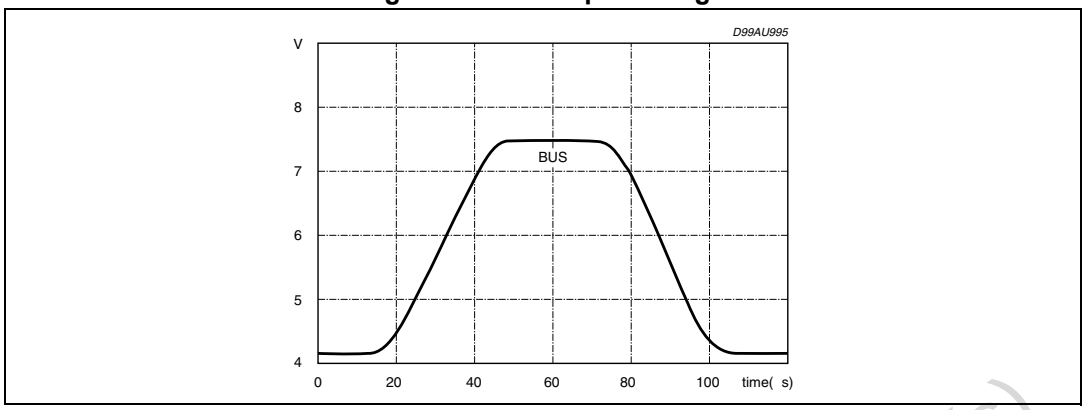
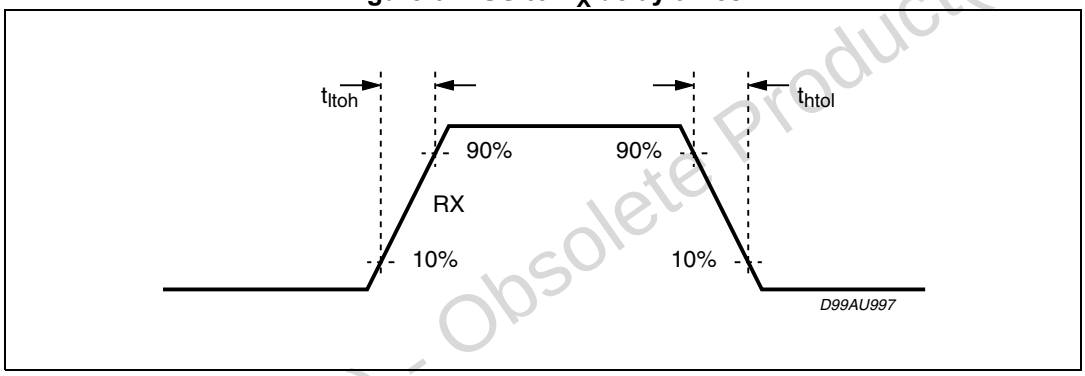


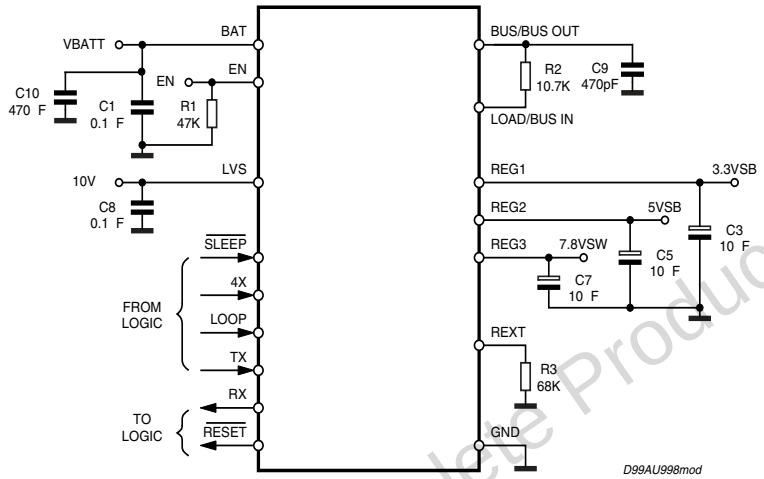
Figure 6. BUS to R_X delay times



4 Typical application circuit

4.1 Application circuit

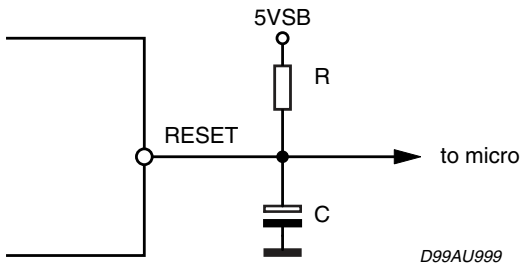
Figure 7. Application circuit



Note: ESR of output capacitors should be between 0.2Ω and 5.0Ω.

4.2 Typical reset circuit

Figure 8. Reset circuit



1) 10kΩ is the minimum resistance for R.
2) The value of C depends on timing needed

Table 7. External components parts list for standard application

Quantity	Application Description	Part Description	Note Number
5	C1, C8	CAP - 0.1µF, 25V	(1)
3	C3, C5, C7	CAP - Tant 10µF, 10V	(2)
1	R1	RES-47k, 1/16W 5%	(3)
1	R2	RES - 10.7k, 1/16W, 1%	(4)
1	R3	RES - 68k, 1/16W, 1%	(5)
1	C9	CAP - 25V, 470pF	(6)
1	C10	CAP - 50V, 470pF	(1)

Reasons for this component choice:

1. Noise suppression
2. Output compensation
3. Pull down resistor
4. Bus resistor
5. Bus slew rate control
6. Proper bus capacitance

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

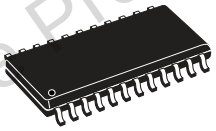
Figure 9. SO-24 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	15.20		15.60	0.598		0.614
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

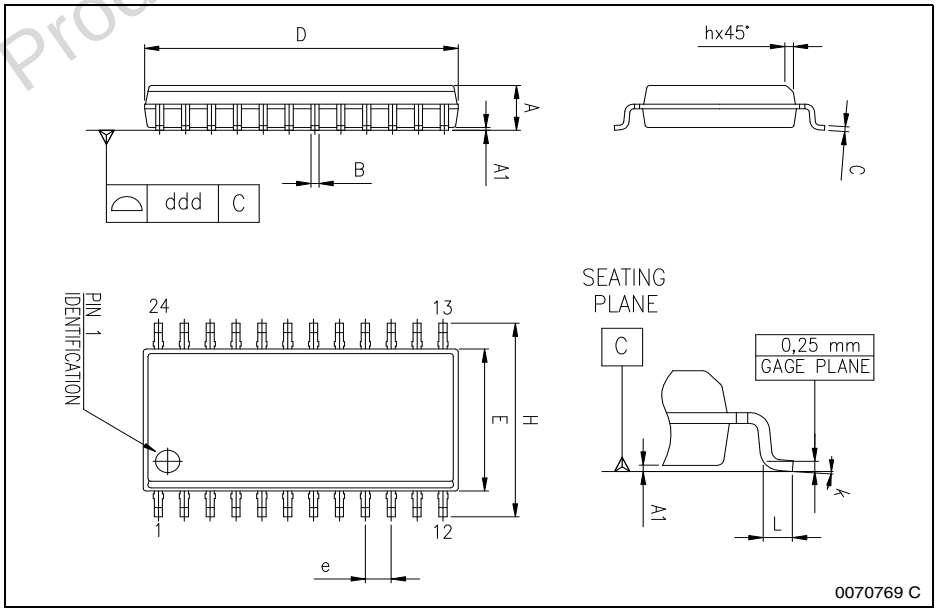
(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA

Weight: 0.60gr



SO24



6 Revision history

Table 8. Document revision history

Date	Revision	Changes
24-Jan-2001	1	Initial release.
23-Sep-2013	2	Updated disclaimer.

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