42 V System Power Supply with Ultra-low Power Window-type Watchdog Timer for Industrial Application

No. EY-409-200326

OVERVIEW

The R5115x is a system power supply IC with an ultra-low power window-type watchdog timer (VR + VD + WDT) that has an input voltage range of 3.5 V to 42 V. This is a high-reliability semiconductor device for industrial application (-Y) that has passed both the screening at high temperature and the reliability test with extended hours.

KEY BENEFITS

- Consists of a voltage regulator, a voltage detector and a watchdog timer that provides a system power supply, a power supply voltage monitoring and a system malfunction monitoring.
- Equipped with an auto monitoring stop (1) to cease the watchdog timer monitoring at light load.
- Outputs a reset signal from watchdog timer when a pulse signal period is too short or too long.

KEY SPECIFICATIONS

- Input Voltage Range (Absolute Maximum Rating): 3.5 V to 42.0 V (50.0 V)
- Supply Current: Typ. 8.5 µA
- Protections: Thermal Shutdown, Output Current Limiting, Short-circuit Current Limiting

Voltage Regulator (VR) Section

- Output Voltage Range: 3.3 V to 5.0 V
- Output Voltage Accuracy: ±1.6% (−40°C ≤ Ta ≤ 125°C)
- Output Current: 250 mA

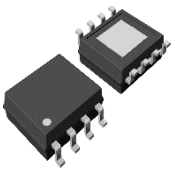
Voltage Detector (VD) Section

- Detection Voltage Threshold Range: 2.5 V to 4.8 V
- Detection Voltage Accuracy: ±1.6% (−40°C ≤ Ta ≤ 125°C)

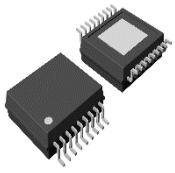
Watchdog Timer (WDT) Section

- Watchdog Timer Accuracy (tow): −17.8% to 21.7% (−40°C ≤ Ta ≤ 125°C)

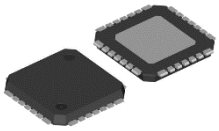
PACKAGES



HSOP-8E
5.2 x 6.2 x 1.6* mm
*maximum dimension

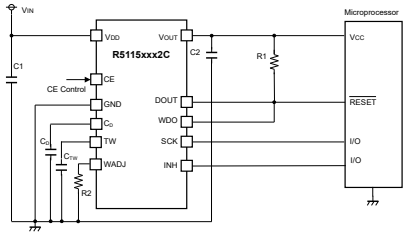


HSOP-18
5.2 x 6.2 x 1.6* mm
*maximum dimension



HQFN0808-28
8.8 x 8.8 x 0.95 mm

TYPICAL APPLICATION



C_{IN}, C_{OUT}: 0.1 µF, Ceramic capacitor
C_{TW}: Capacitor for setting watchdog timer
C_D: Capacitor for setting reset delay time

SELECTION GUIDE

Product Name	Package	Quantity per Reel
R5115Sxx1∗-E2-YE	HSOP-8E	1,000 pcs
R5115Sxx2∗-E2-YE	HSOP-18	1,000 pcs
R5115Lxx2∗-TR-YE	HQFN0808-28	2,000 pcs

xx: Set output voltage (V_{SET}) and set detection voltage ($-V_{DSET}$) options. Assign a code starting from 01 to designate a desired combination of V_{SET} and $-V_{DSET}$.

∗: Other functional options

∗	Package	WADJ	WDO Pin	RESETB/DOUT Pin
A	HSOP-8E	Internally fixed	No	RESETB
B	HSOP-8E	No	No	RESETB
C	HSOP-18 HQFN0808-28	Adjustable	Yes	DOUT

APPLICATIONS

- Factory Automation Equipment, Smart meters
- Surveillance Camera, Vending Machines

(1) R5115Sxx1A, R5115xxx2C only

SELECTION GUIDE

A set detection voltage, a package type, a WADJ function, a WDO pin and a RESETB/DOUT pin are user-selectable options.

Selection Guide

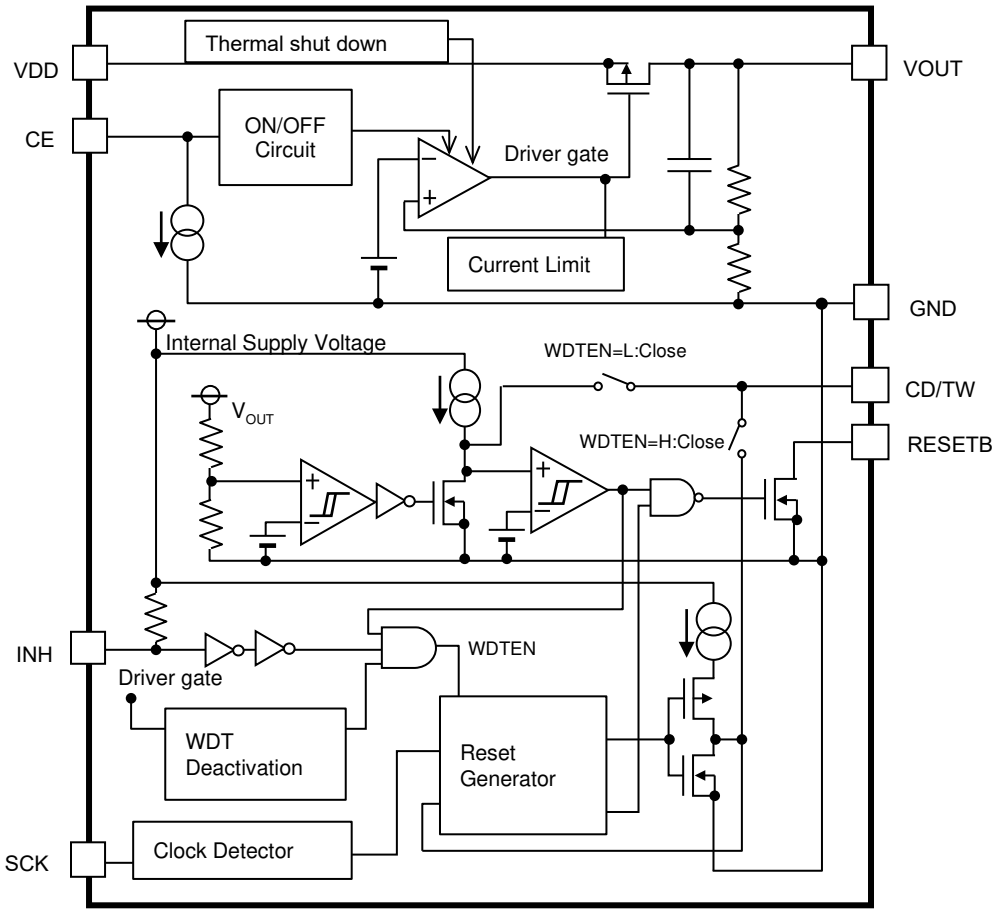
Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5115Sxx1∗-E2-YE	HSOP-8E	1,000 pcs	Yes	Yes
R5115Sxx2∗-E2-YE	HSOP-18	1,000 pcs	Yes	Yes
R5115Lxx2∗-TR-YE	HQFN0808-28	2,000 pcs	Yes	Yes

xx: Set output voltage (V_{SET}) and set detection voltage ($-V_{DSET}$) options
Assign a code starting from 01 to designate a desired combination of V_{SET} and $-V_{DSET}$.

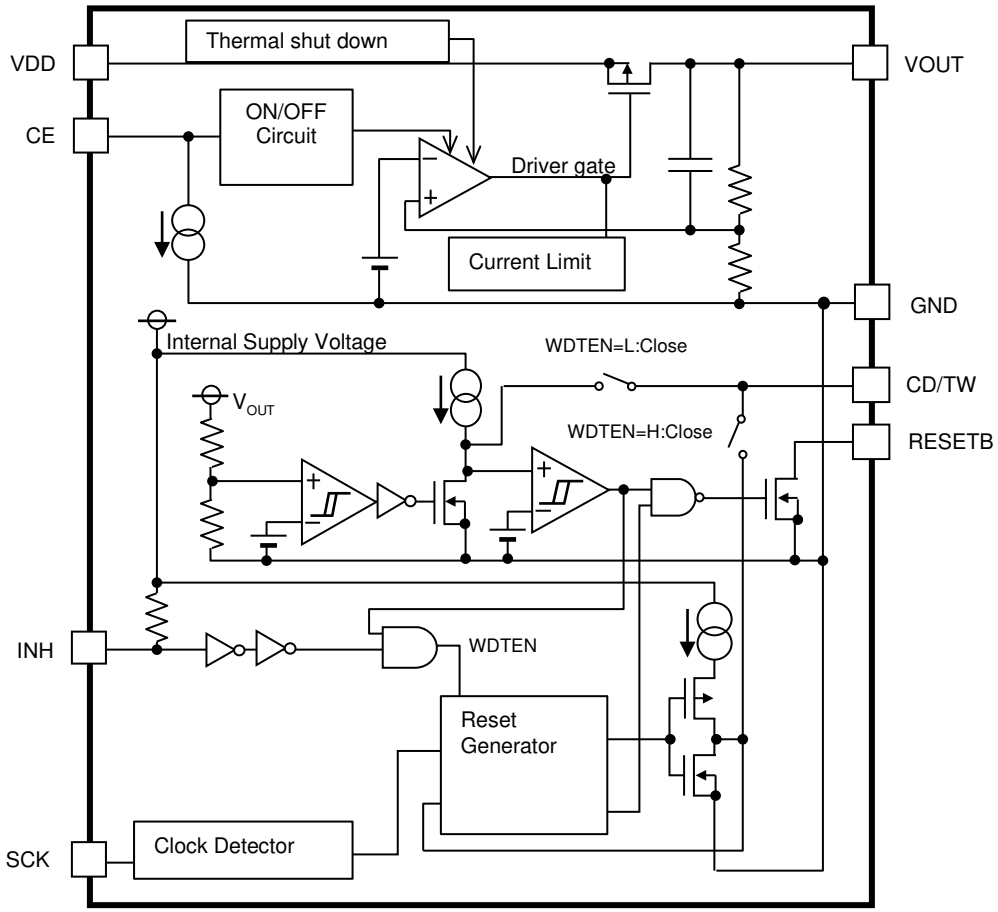
∗: Other functional options

∗	Package	WDT Type	WADJ Function	WDO Pin	RESETB/DOUT Pin
A	HSOP-8E	Window	Internally Fixed	No	RESETB
B	HSOP-8E	Window	No	No	RESETB
C	HSOP-18 HQFN0808-28	Window	Adjustable	Yes	DOUT

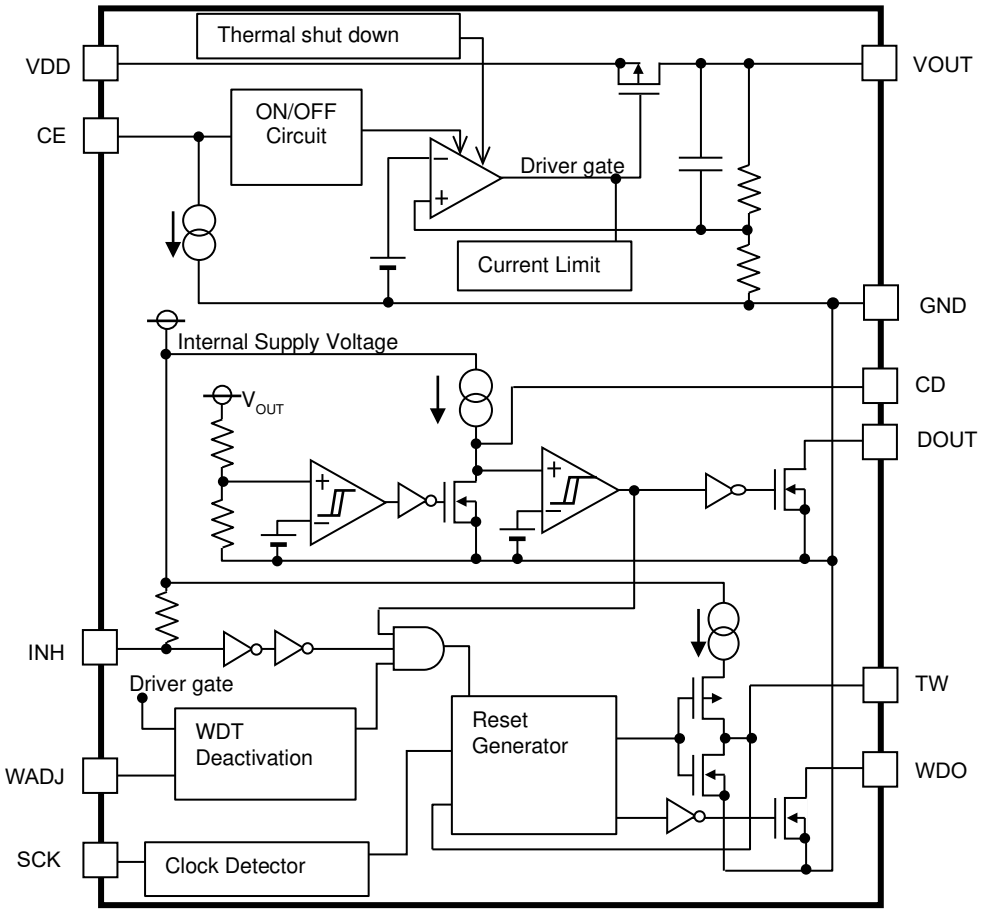
BLOCK DIAGRAMS



R5115Sxx1A Block Diagram

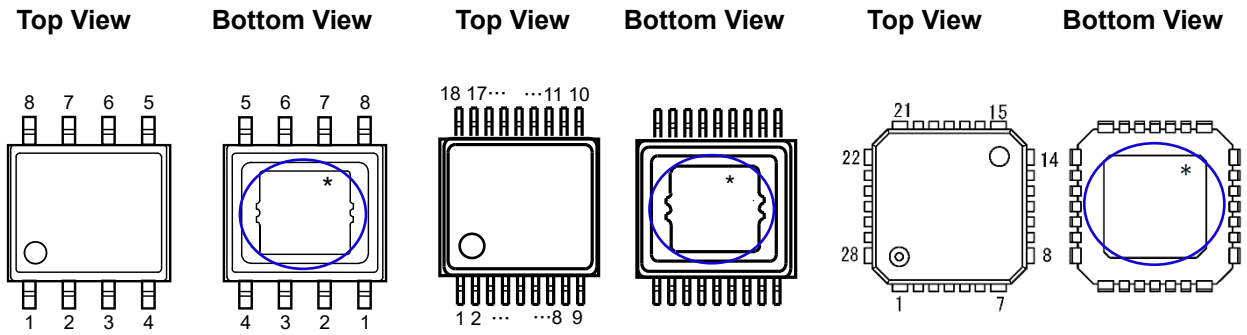


R5115Sxx1B Block Diagram



R5115xxx2C Block Diagram

PIN DESCRIPTION



HSOP-8E Pin Configuration **HSOP-18 Pin Configuration** **HQFN0808-28 Pin Configuration**

* The tab on the bottom of the package shown by blue circle is a substrate potential (GND). It is recommended that this tab be connected to the ground plane on the board but it is possible to leave the tab floating.

HSOP-8E Pin Description, R5115Sxx1A/R5115Sxx1B

Pin No.	Pin Name	Description
1	VDD	Power Supply Pin
2	CD/TW	Watchdog Timer Monitoring Time Setting Pin/ Voltage Detector Reset Delay Time (Power-on Reset Time) Setting Pin
3	CE	Chip Enable Pin, Active-high
4	GND	Ground Pin
5	INH	Inhibit Pin, Active-low
6	SCK	Watchdog Timer Pulse Inputting Pin
7	RESETB(1)	Reset Output Pin, Active-low, Nch Open Drain Output
8	VOUT	Voltage Regulator Output Pin

(1) The RESET pin voltage should be pulled up to the appropriate level using an external resistor.

HSOP-18 Pin Description, R5115Sxx2C

Pin No.	Pin Name	Description
1	VDD	Power Supply Pin
2	NC	No Connection
3	CD	Voltage Detector Reset Delay Time (Power-on Reset Time) Setting Pin
4	NC	No Connection
5	TW	Watchdog Timer Monitoring Time Setting Pin
6	NC	No Connection
7	CE	Chip Enable Pin, Active-high
8	NC	No Connection
9	GND	Ground Pin
10	WADJ	Watchdog Timer Operating Threshold Pin
11	INH	Inhibit Pin, Active-low
12	NC	No Connection
13	SCK	Watchdog Timer Pulse Input Pin
14	NC	No Connection
15	WDO(1)	Watchdog Timer Output Pin, Nch Open Drain Output
16	DOUT(2)	RESET Output Pin, Active-low, Nch Open Drain Output
17	NC	No Connection
18	VOUT	Voltage Regulator Output Pin

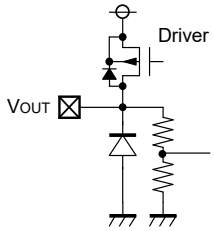
(1) The WDO pin voltage should be pulled up to the appropriate level using an external resistor.
(2) The DOUT pin voltage should be pulled up to the appropriate level using an external resistor.

HQFN0808-28 Pin Description, R5115Lxx2C

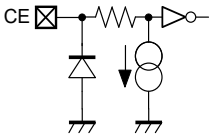
Pin No.	Pin Name	Description
1	GND	Ground Pin
2	CD	Voltage Detector Reset Delay Time (Power-on Reset Time) Setting Pin
3	TW	Watchdog Timer Monitoring Time Setting Pin
4	NC	No Connection
5	CE	Chip Enable Pin, Active-high
6	NC	No Connection
7	GND	Ground Pin
8	GND	Ground Pin
9	GND	Ground Pin
10	NC	No Connection
11	WADJ	Watchdog Timer Operating Threshold Pin
12	INH	Inhibit Pin, Active-low
13	NC	No Connection
14	GND	Ground Pin
15	GND	Ground Pin
16	SCK	Watchdog Timer Pulse Input Pin
17	NC	No Connection
18	WDO(1)	Watchdog Timer Output Pin, Nch Open Drain Output
19	DOUT(2)	RESET Output Pin, Active-low, Nch Open Drain Output
20	NC	No Connection
21	GND	Ground Pin
22	GND	Ground Pin
23	NC	No Connection
24	VOUT	Voltage Regulator Output Pin
25	NC	No Connection
26	VDD	Power Supply Pin
27	NC	No Connection
28	GND	Ground Pin

(1) The WDO pin voltage should be pulled up to the appropriate level using an external resistor.
(2) The DOUT pin voltage should be pulled up to the appropriate level using an external resistor.

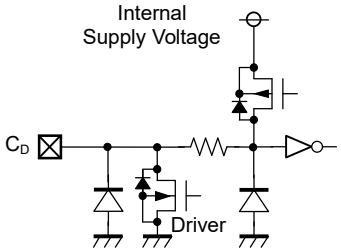
Equivalent Circuits of Individual Pins



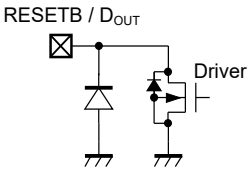
Equivalent Circuit for VOUT Pin



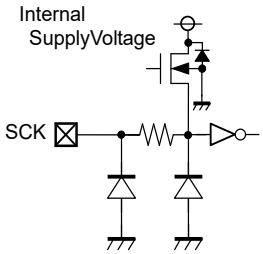
Equivalent Circuit for CE Pin



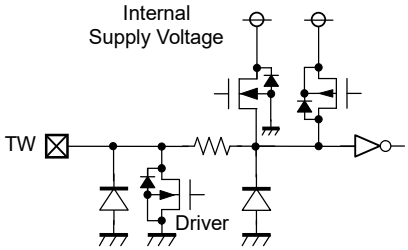
Equivalent Circuit for CD Pin



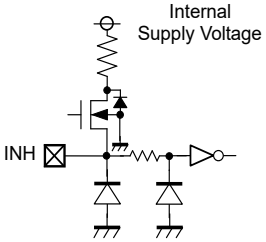
Equivalent Circuit for RESETB Pin (R5115Sxx1x)/
Equivalent Circuit for DOUT Pin (R5115xxx2C)



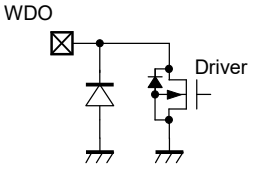
Equivalent Circuit for SCK Pin



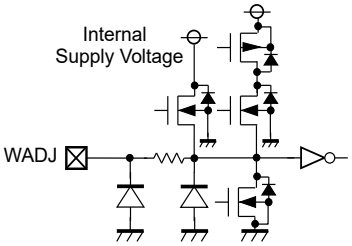
Equivalent Circuit for TW Pin



Equivalent Circuit for INH Pin



Equivalent Circuit for WDO Pin (R5115xxx2C)



Equivalent Circuit for WADJ Pin (R5115xxx2C)

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{IN}	Input Voltage	−0.3 to 50	V
	Peak Voltage(1)	60	V
V_{CE}	CE Pin Input Voltage	−0.3 to 50	V
V_{OUT}	VOUT Pin Output Voltage	−0.3 to V_{IN} +0.3 ≤ 50	V
V_{CD}	CD Pin Output Voltage	−0.3 to 7.0	V
V_{TW}	TW Pin Output Voltage	−0.3 to 7.0	V
V_{RESETB}	RESETB Pin Output Voltage	−0.3 to 7.0	V
V_{DOUT}	DOUT Pin Output Voltage	−0.3 to 7.0	V
V_{WDO}	WDO Pin Output Voltage	−0.3 to 7.0	V
V_{SCK}	SCK Pin Input Voltage	−0.3 to 7.0	V
V_{INH}	INH Pin Input Voltage	−0.3 to 7.0	V
V_{WADJ}	WADJ Pin Output Voltage	−0.3 to 7.0	V
I_{RESETB}	RESETB Pin Current	16	mA
I_{DOUT}	DOUT Pin Current	16	mA
I_{WDO}	WDO Pin Current	16	mA
P_D	Power Dissipation	Refer to Appendix *"Power Dissipation"*	
Tj	Junction Temperature Range	−40 to 150	°C
Tstg	Storage Temperature Range	−55 to 150	°C

ABSOLUTE MAXIMUM RATINGS
Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

(1) Application time is 200 ms or less.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{IN}	Input Voltage	3.5 to 42.0	V
V_{CE}	CE Pin Input Voltage	0 to 42.0	V
V_{SCK}	SCK Pin Input Voltage	0 to 5.5	V
V_{INH}	INH Pin Input Voltage	0 to 5.5	V
Ta	Operating Temperature Range	−40 to 125	°C

RECOMMENDED OPERATING CONDITIONS
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

C_{IN} = C_{OUT} = 0.1µF, V_{IN} = 14 V, unless othrewise noted.

The specifications surrounded by [ ] are guaranteed by design engineering at −40°C ≤ Ta ≤ 125°C.

R5115xxxxx-YE Electrical Characteristics **(Ta = 25°C)**

Symbol	Parameter	Test Conditions/Comments	Min.	Typ.	Max.	Unit
I_{SS}	Supply Current	I_{OUT} = 0 mA R5115Sxx1A/ R5115xxx2C		8.5	[18]	µA
		I_{OUT} = 0 mA R5115Sxx1B		13.5	[23]	µA
Istandby	Standby Current	V_{IN} = 42 V, V_{CE} = 0 V		0.2	1.0	µA
I_{PD}	CE Pull-down Constant Current	V_{CE} = 42 V		0.2	[0.6]	µA
V_{CEH}	CE Input Voltage, High		[2.2]		[42]	V
V_{CEL}	CE Input Voltage, Low				[1.0]	V

VR Section **(Ta = 25°C)**

Symbol	Parameter	Test Conditions/Comments		Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	I_{OUT} = 1 mA	Ta = 25°C	[×0.994]		×1.006	V
			−40°C ≤ Ta ≤ 125°C	[×0.984]		[×1.016]	V
ΔV_{OUT}/ ΔI_{OUT}	Load Regulation	V_{IN} = V_{SET} + 3.0 V 1 mA ≤ I_{OUT} ≤ 250 mA		[-20]	0	[50]	mV
V_{DIF}	Dropout Voltage	I_{OUT} = 250 mA	V_{SET} = 3.3		1.0	[2.0]	V
			V_{SET} = 5.0		0.80	[1.5]	V
ΔV_{OUT}/ ΔV_{IN}	Line Regulation	3.5 V ≤ V_{SET} + 0.5 V ≤ V_{IN} ≤ 42 V I_{OUT} = 1 mA			0.01	[0.02]	%/V
I_{LIM}	Output Current Limit	V_{IN} = V_{SET} + 3.0 V		[320]	440	[530]	mA
I_{SC}	Short-circuit Current Limit	V_{IN} = 5 V, V_{OUT} = 0 V		[70]	95	[135]	mA
T_{TSD}	Thermal Shutdown Temperature Threshold, rising	Junction Temperature		[150]	170		°C
T_{TSR}	Thermal Shutdown Temperature Threshold, falling	Junction Temperature		[125]	140		°C

C_{IN} = C_{OUT} = 0.1µF, V_{IN} = 14 V, unless othrewise noted.

The specifications surrounded by [ ] are guaranteed by design engineering at −40°C ≤ Ta ≤ 125°C.

R5115xxxxx-YE Electrical Characteristics (Contimued)

VD Section **(Ta = 25°C)**

Symbol	Parameter	Test Conditions/Comments		Min.	Typ.	Max.	Unit
-V_{DET}	Detection Voltage	V_{DD} = V_{OUT} (V_{OUT} Detection)	Ta = 25°C	x0.994		x1.006	V
			−40°C ≤ Ta ≤ 125°C	x0.984		x1.016	
V_{HYS}	Detection Threshold Hysteresis			−V_{DSET} ×0.015	−V_{DSET} ×0.02	−V_{DSET} ×0.025	V
t_{RESET}	Reset Delay Time (Power-on Reset)	C_D = 0.22 µF		184	220	253	ms
V_{RESETB}	RESETB Pull-up Voltage	R5115Sxx1A / R5115Sxx1B				5.5	V
V_{DOUT}	DOUT Pull-up Voltage	R5115xxx2C				5.5	V
$I_{OUTRSTB}$	Nch Driver Output Current (RESETB Output Pin)	R5115Sxx1A / R5115Sxx1B V_{IN} = 3.5 V, V_{RESETB} = 0.1 V		0.3	0.6		mA
$I_{LEAKRSTB}$	Nch Driver Leakage Current (RESETB Output Pin)	R5115Sxx1A / R5115Sxx1B V_{RESETB} = 5.5 V				0.3	µA
$I_{OUTDOUT}$	Nch Driver Output Current (DOUT Output Pin)	R5115xxx2C V_{IN} = 3.5 V, V_{DOUT} = 0.1 V		0.3	0.6		mA
$I_{LEAKDOUT}$	Nch Driver Leakage Current (DOUT Output Pin)	R5115xxx2C V_{DOUT} = 5.5 V				0.3	µA
R_{LCD}	CD Auto-discharge (Nch Tr. On-resistance)	V_{CE} = 0 V, V_{CD} = 0.1 V			7.5	20	kΩ

C_{IN} = C_{OUT} = 0.1µF, V_{IN} = 14 V, unless othrewise noted.

The specifications surrounded by [ ] are guaranteed by design engineering at −40°C ≤ Ta ≤ 125°C.

R5115xxxxx-YE Electrical Characteristics (Contimued)

WDT Section **(Ta = 25°C)**

Symbol	Parameter	Test Conditions/Comments	Min.	Typ.	Max.	Unit
t_{OW}	Open Window Time	C_{TW} = 10 nF	14.8	18.0	21.9	ms
t_{CW}	Closed Window Time	C_{TW} = 10 nF	3.8	4.5	5.3	ms
t_{OWL}	Long Open Window Time	C_{TW} = 10 nF	37	80	150	ms
t_{IGN}	Pulse Ignoring Time	C_{TW} = 10 nF	14.0	18.0	22.9	ms
t_{WR}	Reset Time	C_{TW} = 10 nF	7.2	9.0	10.7	ms
V_{SCKH}	SCK Input, High		1.5		5.5	V
V_{SCKL}	SCK Input, Low		0		0.65	V
V_{INHH}	INH Input, High		1.5		5.5	V
V_{INHL}	INH Input, Low		0		0.5	V
I_{INH}	INH Pull-up Current	V_{INH} = 0 V	4.0	8.0	11.5	µA
$I_{OWDTACT}$	WDT Activating Threshold Current	R5115Sxx1A		1.2	2.2	mA
$I_{OWDTDEACT}$	WDT Deactivating Threshold Current	R5115Sxx1A	0.6	1.0		mA
$\frac{I_{OUT}}{I_{WADJ}}(1)$	WADJ Pin Current Ratio (WDT is not active.)	R5115xxx2C V_{WADJ} = 0 V, I_{OUT} = 10 mA	1000	1600	3200	-
$\frac{I_{OUT}}{I_{WADJ}}(2)$	WADJ Pin Current Ratio (WDT is active.)	R5115xxx2C V_{WADJ}=1.0 V, I_{OUT} = 10 mA	800	1200	2400	-
V_{WADJ_TH}	WADJ Pin Threshold Voltage	R5115xxx2C	0.6	0.7	0.8	V
t_{SCKWH}	SCK Minimum Input Pulse Width, High	V_{SCKL} = 0.5, V_{SCKH} = 1.6	500			ns
t_{SCKWL}	SCK Minimum Input Pulse Width, Low	V_{SCKL} = 0.5, V_{SCKH} = 1.6	1500			ns
V_{WDO}	WDO Pull-up Voltage				5.5	V
I_{OUTWDO}	Nch Driver Output Current (WDO Output Pin)	R5115xxx2C V_{IN} = 3.5 V, V_{WDO} = 0.1 V	0.7	1.5		mA
$I_{LEAKWDO}$	Nch Driver Leakage Current (WDO Output Pin)	R5115xxx2C V_{WDO} = 5.5 V			0.3	µA
R_{LTW}	C_{TW} Auto-discharge (Nch Tr. On-resistance)	V_{CE} = 0 V, V_{TW} = 0.1 V		7.5	20	kΩ

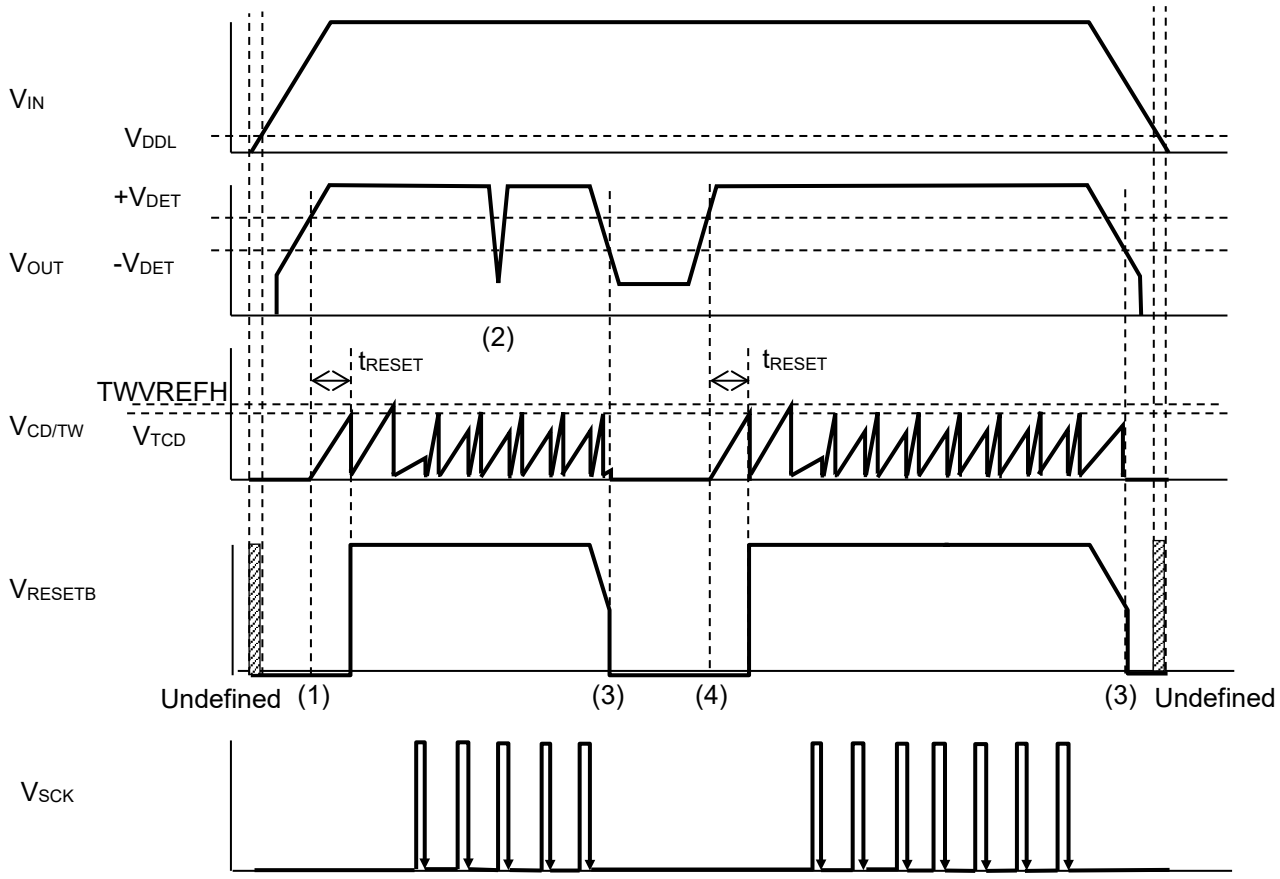
Product-specific Electrical Characteristics: Voltage Regulator Section

Product Name	VR Section					
	V_{OUT}					
	Ta = 25°C			−40 ≤ Ta ≤ 125°C		
	Min	Typ.	Max.	Min.	Typ.	Max.
R5115x01xx	4.9700	5.000	5.0300	4.9200	5.000	5.0800
R5115x02xx	4.9700	5.000	5.0300	4.9200	5.000	5.0800
R5115x03xx	4.9700	5.000	5.0300	4.9200	5.000	5.0800
R5115x04xx	4.9700	5.000	5.0300	4.9200	5.000	5.0800
R5115x05xx	3.2802	3.300	3.3198	3.2472	3.300	3.3528
R5115x06xx	3.2802	3.300	3.3198	3.2472	3.300	3.3528
R5115x07xx	3.2802	3.300	3.3198	3.2472	3.300	3.3528
R5115x08xx	4.9700	5.000	5.0300	4.9200	5.000	5.0800
R5115x09xx	4.9700	5.000	5.0300	4.9200	5.000	5.0800
R5115x10xx	4.9700	5.000	5.0300	4.9200	5.000	5.0800
R5115x11xx	4.9700	5.000	5.0300	4.9200	5.000	5.0800
R5115x12xx	4.9700	5.000	5.0300	4.9200	5.000	5.0800

Product-specific Electrical Characteristics: Voltage Detector Section

Product Name	VD Section								
	$-V_{DET}$						V_{HYS}		
	Ta = 25°C			−40 ≤ Ta ≤ 125°C					
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
R5115x01xx	4.5724	4.600	4.6276	4.5264	4.600	4.6736	0.0690	0.0920	0.1150
R5115x02xx	3.2802	3.300	3.3198	3.2472	3.300	3.3528	0.0495	0.0660	0.0825
R5115x03xx	3.9760	4.000	4.0240	3.9360	4.000	4.0640	0.0600	0.0800	0.1000
R5115x04xx	4.4730	4.500	4.5270	4.4280	4.500	4.5720	0.0675	0.0900	0.1125
R5115x05xx	2.9820	3.000	3.0180	2.9520	3.000	3.0480	0.0450	0.0600	0.0750
R5115x06xx	2.8826	2.900	2.9174	2.8536	2.900	2.9464	0.0435	0.0580	0.0725
R5115x07xx	2.6838	2.700	2.7162	2.6568	2.700	2.7432	0.0405	0.0540	0.0675
R5115x08xx	4.3736	4.400	4.4264	4.3296	4.400	4.4704	0.0660	0.0880	0.1100
R5115x09xx	4.0754	4.100	4.1246	4.0344	4.100	4.1656	0.0615	0.0820	0.1025
R5115x10xx	4.1748	4.200	4.2252	4.1328	4.200	4.2672	0.0630	0.0840	0.1050
R5115x11xx	2.4850	2.500	2.5150	2.4600	2.500	2.5400	0.0375	0.0500	0.0625
R5115x12xx	2.7832	2.800	2.8168	2.7552	2.800	2.8448	0.0420	0.0560	0.0700

THEORY OF OPERATION



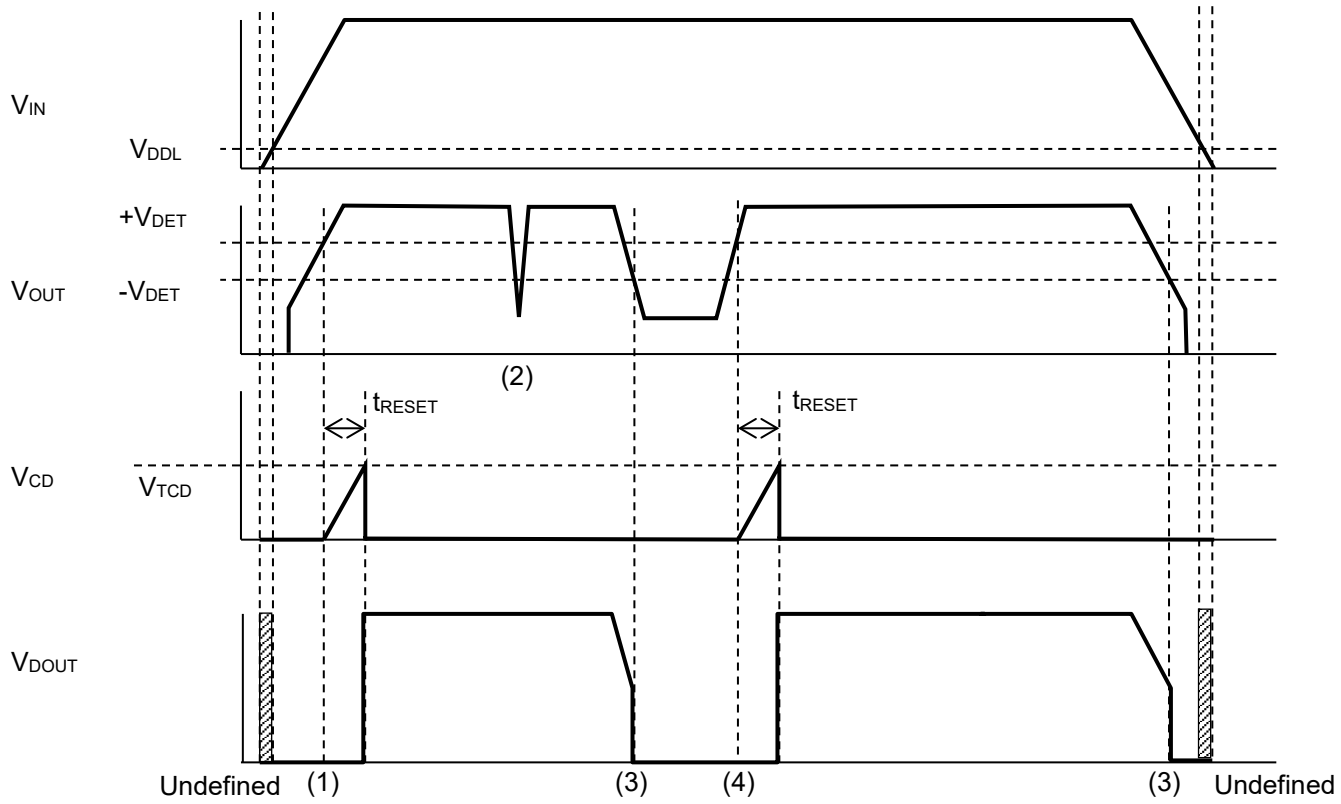
R5115Sxx1A/ R5115Sxx1B VD Timing Chart

(1) When the output voltage (V_{OUT}) of a voltage regulator (VR) becomes more than the reset voltage ($+V_{DET}$), the RESETB pin voltage (V_{RESETB}) becomes high after the reset delay time (t_{RESET}). During t_{RESET}, the CD/TW pin serves as a rest delay time setting pin. When V_{RESETB} becomes high, the CD/TW pin serves as a watchdog timer setting pin.

(2) When V_{OUT} becomes lower than the detection voltage ($-V_{DET}$) and when that period is shorter than the delay time (t_{DELAY}), Typ. 30 µs or lower, V_{RESETB} remains high and does not go into the detecting state.

(3) When V_{OUT} becomes lower than $-V_{DET}$, V_{RESETB} becomes low after a 30-µs (Typ.) t_{DELAY}, and the voltage detector (VD) goes into the detecting state.

(4) When V_{OUT} becomes higher than $+V_{DET}$, V_{RESETB} becomes high after t_{RESET}. (V_{TCD} = Typ.1 V)



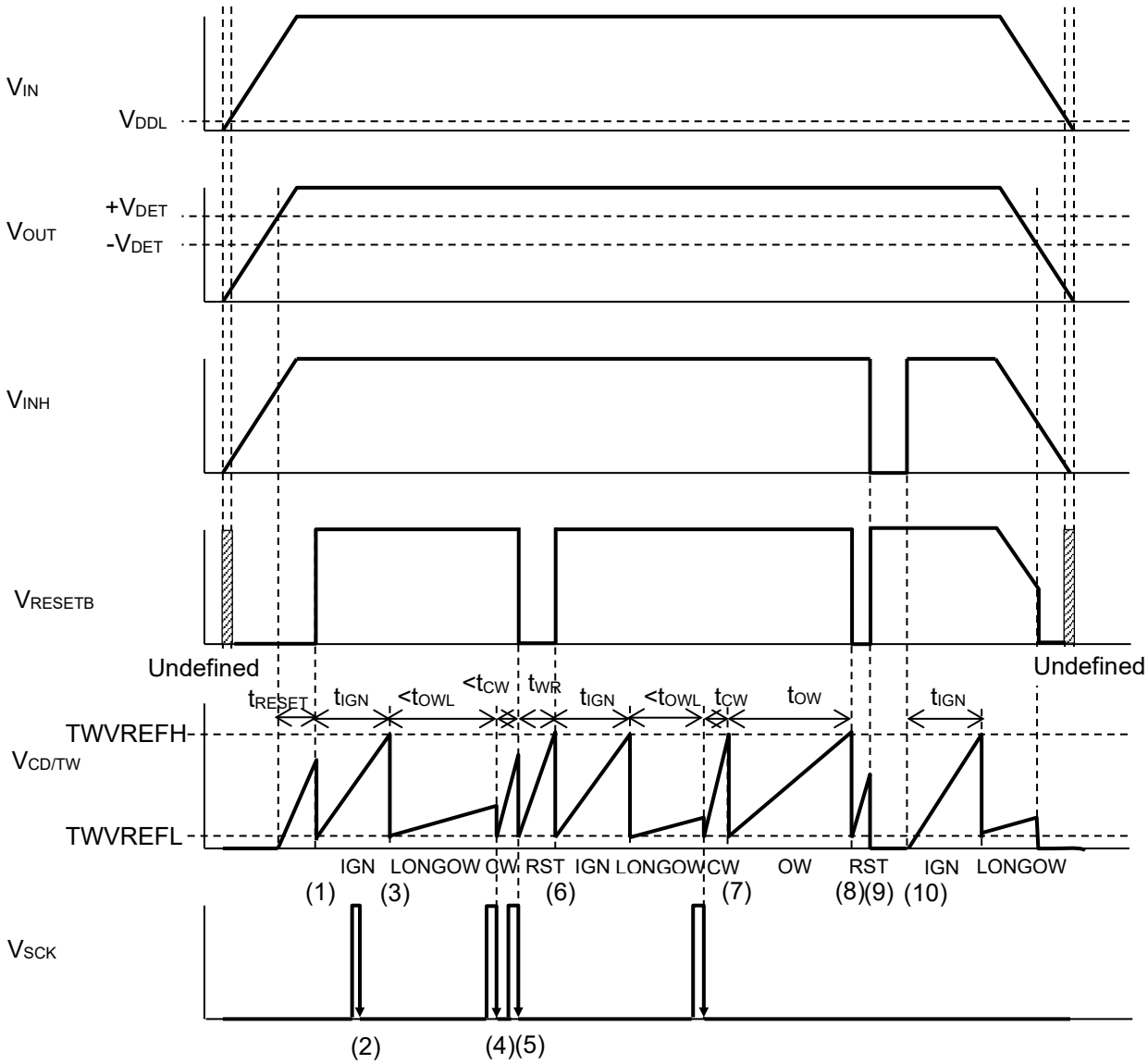
R5115xxx2C VD Timing Chart

(1) When the output voltage (V_{OUT}) of a voltage regulator (VR) becomes higher than the reset voltage ($+V_{DET}$), the DOUT pin voltage (V_{DOUT}) becomes high after the reset delay time (t_{RESET}).

(2) When V_{OUT} becomes lower than the detection voltage ($-V_{DET}$) and when that period is shorter than the delay time (t_{DELAY}), Typ. 30 µs or lower, V_{DOUT} remains high and does not go into the detecting state.

(3) When V_{OUT} becomes lower than $-V_{DET}$, V_{DOUT} becomes low after a 30-µs (Typ.) t_{DELAY}, and the voltage detector (VD) goes into the detecting state.

(4) When V_{OUT} becomes higher than $+V_{DET}$, V_{DOUT} becomes high after t_{RESET}. (V_{TCD} = Typ.1 V)



R5115Sxx1A/R5115Sxx1B WDT Timing Chart, Window Type

(1) When the output voltage (V_{OUT}) of a voltage regulator (VR) becomes higher than the reset voltage ($+V_{DET}$), the RESETB pin voltage (V_{RESETB}) becomes high after the reset delay time (t_{RESET}), and the watchdog timer (WDT) starts monitoring a pulse. After that, the CD/TW pin voltage ($V_{CD/TW}$) repeats charge and discharge. As a result, a sawtooth wave is generated. The WDT has four states: Ignoring, Reset, Open Window and Closed Window. In each state, the CD/TW pin is charged from 0 V or TWVREFL (Typ. 0.08 V).

(2) After WDT starts, WDT is in an ignoring state until $V_{CD/TW}$ is charged up to TWVREFH (Typ. 2V). So, a pulse to the SCK pin is ignored during the ignoring state.

(3) When $V_{CD/TW}$ is charged up to TWVREFH during the ignoring state, the CD/TW pin starts discharging and WDT goes into a long open window state. While this long open window state works as an open window state, it is four times longer than the normal open window state.

(4) When a pulse is sent to the SCK pin before $V_{CD/TW}$ reaches TWVREFH during the open window state, the CD/TW pin starts discharging and WDT goes into a closed window state.

(5) When a pulse is sent to the SCK pin before $V_{CD/TW}$ reaches TWVREFH during the closed window state, the CD/TW pin starts discharging and WDT goes into a reset state. During the reset state, V_{RESETB} becomes low.

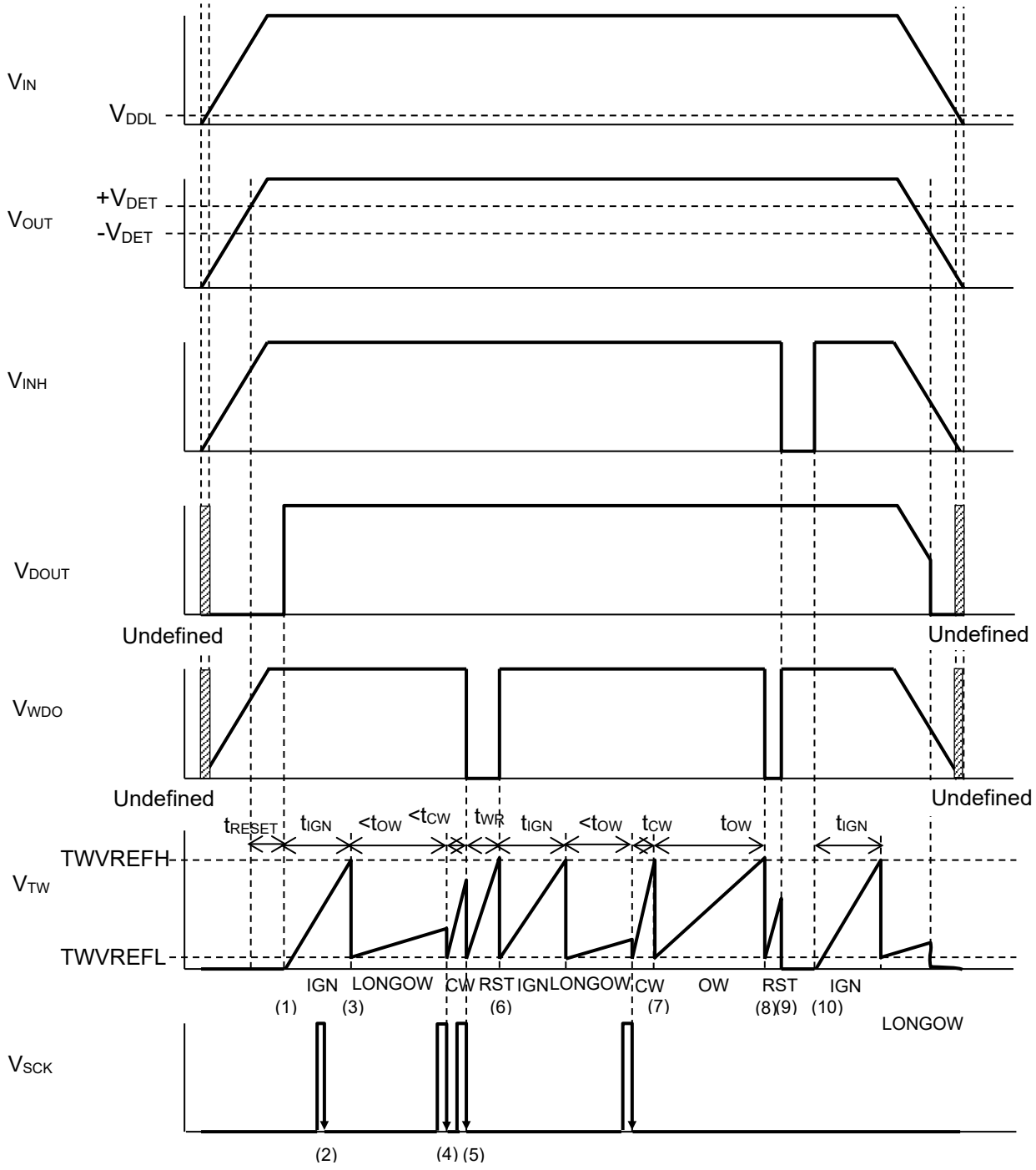
(6) When $V_{CD/TW}$ reaches TWVREFH during the reset state, the CD/TW pin starts discharging and WDT goes into an ignoring state.

(7) When a pulse is not sent to the SCK pin before $V_{CD/TW}$ reaches TWVREFH during a closed window state, the CD/TW pin starts discharging and WDT goes into an open window state.

(8) When a pulse is not sent to the SCK pin before $V_{CD/TW}$ reaches TWVREFH during the open window state, the CD/TW pin starts discharging and WDT goes into a reset state.

(9) When the INH pin voltage (V_{INH}) is set to low, WDT stops monitoring. So, the voltage detector (VD) determines whether V_{RESETB} is set to high/low, or $V_{CD/TW}$ is charged/discharged.

(10) When V_{INH} is changed from low to high, WDT goes into the ignoring state and restarts monitoring a pulse.



R5115xxx2C WDT Timing Chart, Window Type

(1) When the output voltage (V_{OUT}) of a voltage regulator (VR) becomes higher than the reset voltage ($+V_{DET}$), the DOUT pin voltage (V_{DOUT}) becomes high after the reset delay time (t_{RESET}), and the watchdog timer (WDT) starts monitoring a pulse. After that, the TW pin voltage (V_{TW}) repeats charge and discharge. As a result, a sawtooth wave is generated. WDT has four states: Ignoring, Reset, Open Window and Closed Window. In each state, the TW pin is charged from 0 V or TWVREFL (Typ.0.08 V).

(2) After WDT starts, WDT is in an ignoring state until V_{TW} is charged up to TWVREFH. So, a pulse to the SCK pin is ignored during the ignoring state.

(3) When V_{TW} is charged up to TWVREFH during the ignoring state, the TW pin starts discharging and WDT goes into a long open window state. While this long open window state works as an open window state, it is four times longer than the normal open window state.

(4) When a pulse is sent to the SCK pin before V_{TW} reaches TWVREFH during the open window state, the TW pin starts discharging and WDT goes into a closed window state.

(5) When a pulse is sent to the SCK pin before V_{TW} reaches TWVREFH during the close window state, the TW pin starts discharging and WDT goes into a reset state. During the reset state, V_{DOUT} becomes low.

(6) When V_{TW} reaches TWVREFH during the reset state, the TW pin starts discharging and WDT goes into an ignoring state.

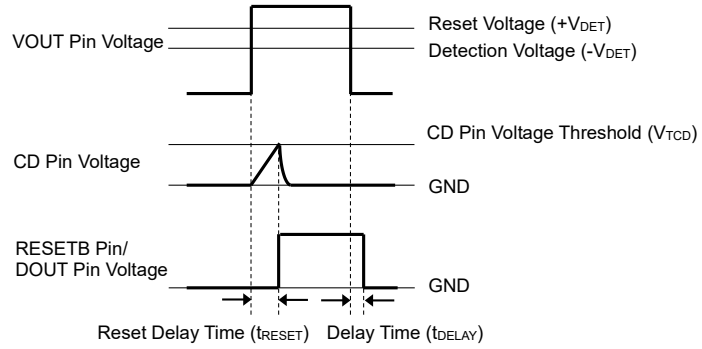
(7) When a pulse is not sent to the SCK pin before V_{TW} reaches TWVREFH during a closed window state, the TW pin starts discharging and WDT goes into an open window state

(8) When a pulse is not sent to the SCK pin before V_{TW} reaches TWVREFH during the open window state, the TW pin starts discharging and WDT goes into a reset state

(9) When the INH pin voltage (V_{INH}) is set to low, WDT stops monitoring. Then, the WDO pin voltage (V_{WDO}) is fixed to high and V_{TW} is fixed to low.

(10) When V_{INH} is changed from low to high, WDT goes into the ignoring state and restarts monitoring a pulse.

Delay Operation and Reset Delay Time



RESETB Pin: R5115Sxx1A/ R5115Sxx1B
DOUT Pin: R5115xxx2C

Delay Time Operation Timing Chart

When the VOUT pin voltage (V_{OUT}) becomes higher than the reset voltage ($+V_{DET}$), the CD pin voltage (V_{CD}) increases as the external capacitor starts charging. The RESETB pin voltage (V_{RESETB})/ the DOUT pin voltage (V_{DOUT}) remains low until V_{CD} reaches the CD pin voltage threshold (V_{TCD}). When V_{CD} becomes higher than V_{TCD}, V_{RESETB} or V_{DOUT} changes from low to high. The reset delay time (t_{RESET}) starts when the V_{OUT} becomes higher than $+V_{DET}$ and ends when V_{DOUT}/V_{RESETB} changes from low to high. When V_{DOUT}/V_{RESETB} changes from low to high, the electrical charge charged in the external capacitor starts discharging. The delay time (t_{DELAY}) starts when V_{OUT} becomes lower than the detection voltage ($-V_{DET}$) and ends when V_{DOUT}/V_{RESETB} changes from high to low. It is not dependent on the capacitance of the external capacitor.

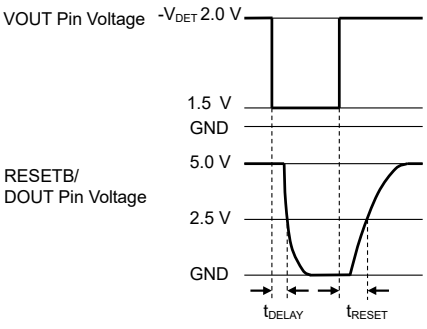
Method of Calculating the Reset Delay Time

The reset delay time (t_{RESET}) can be calculated by the following equation using an external capacitance (C_D):

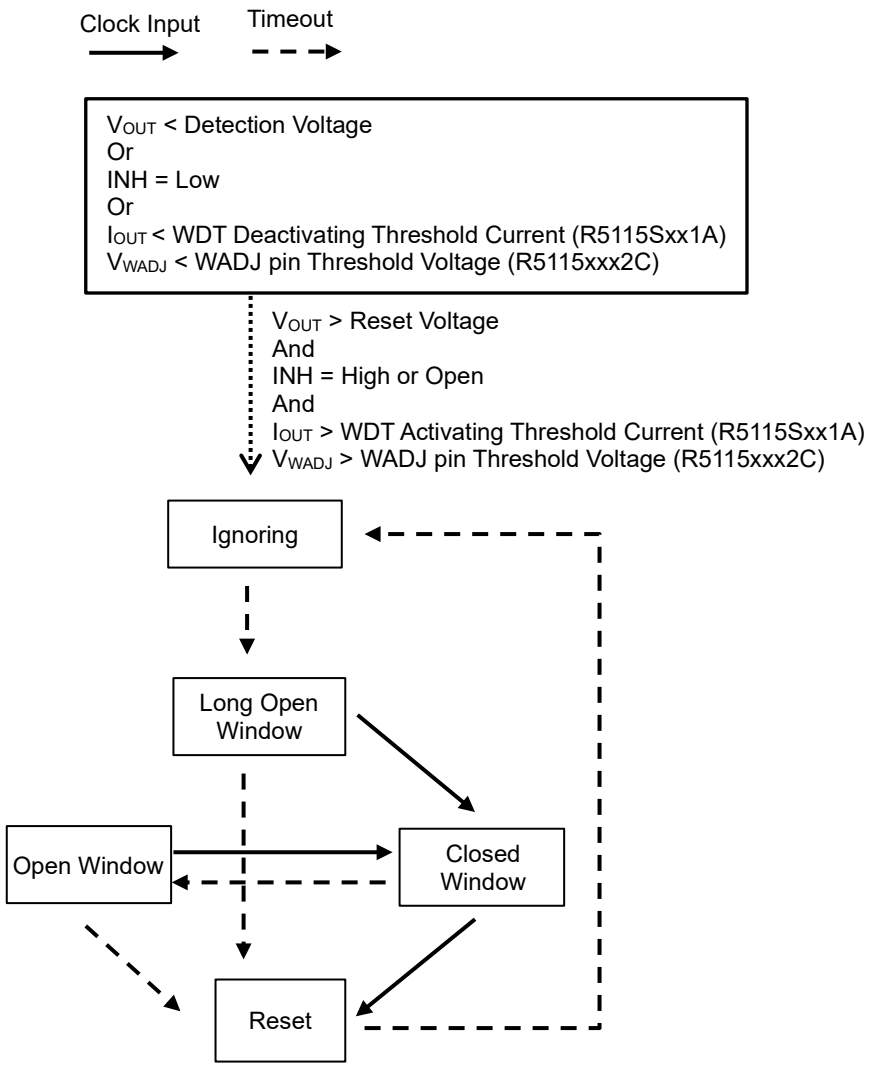
t_{RESET} (s) = 1.0 x C_D (F) / (1.0 x 10^{-6})

To make the VOUT/ SENSE pin voltage rises slower than 0.1 V/s, place a 100-pF or more capacitor (C_D).

t_{RESET} starts when the RESETB/DOUT pin is pulled up to 5 V using a 100-kΩ resistor, and a 1.5-V to ($-V_{DET}$) + 2.0-V pulse voltage is applied to the VOUT pin. It ends when V_{OUT} reaches 2.5 V.



Watchdog Timer State Transition Diagram



Watchdog Timer Setting

A watchdog timer (t_{OW}, t_{CW}, t_{OWL}, t_{IGN}, t_{WR}) can be set by using a capacitor connected to the TW pin. The relationship between capacitance and time are described as below:

t_{OW} (s) = 1.8 x C(F) / (1.0 x 10^{-6})

t_{CW} (s) = 1.8 x C(F) / (4.0 x 10^{-6})

t_{OWL} (s) = 1.8 x C(F) / (0.225 x 10^{-6})

t_{IGN} (s) = 1.8 x C(F) / (1.0 x 10^{-6})

t_{WR} (s) = 1.8 x C(F) / (2.0 x 10^{-6})

Allowable SCK Pulse Period

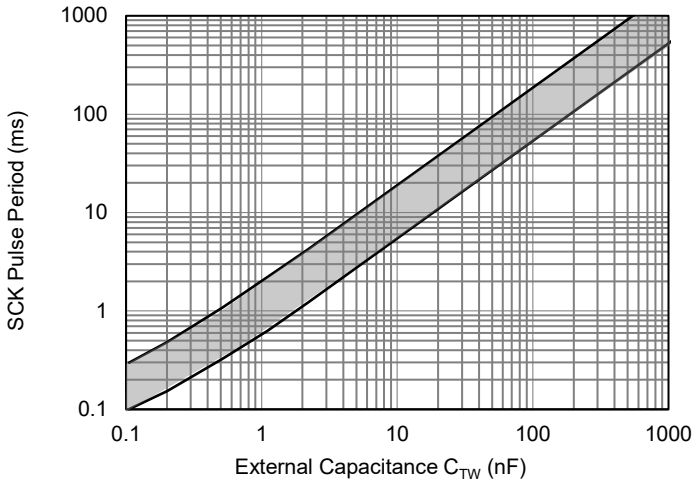
To prevent WDT of the R5115x from going into a reset state, the pulse period inputted to the SCK pin has to meet the following condition.

t_{CW} max < SCK Pulse Period < (t_{CW} + t_{OW}) min

The closed window time (t_{CW}) and the open window time (t_{OW}) in Electrical Characteristics may vary, and also the capacitor connected to the TW pin (C_{TW}) or the CD/TW pin (C_D/C_{TW}) may cause variations in t_{CW} or t_{OW}. Those variations are considered in the calculations below.

Min. SCK Pulse Period (s) = 0.53 x Max. C_{TW} (F) x 10^6
Max. SCK Pulse Period (s) = 1.86 x Min. C_{TW} (F) x 10^6

The graph below shows the relationship between the SCK pulse period and the external capacitance of C_{TW}. The pulse period inputted to the SCK pin has to be fit within the grayed-out area according to the capacitance of C_{TW}.

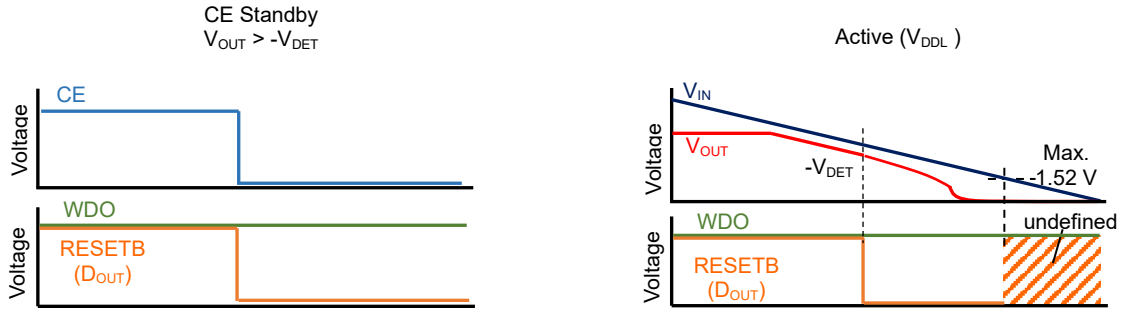


Standby Function

When the CE pin voltage (V_{CE}) is low, the R5115x goes into the standby mode. During the standby mode, the voltage regulator (VR) stops the output, the watchdog timer (WDT) stops the pulse monitoring and the voltage detector (VD) stops the voltage monitoring.
When V_{CE} is low, the outputs of WDT and VD will be as follows regardless of the output voltage (V_{OUT}).

R5115Sxx1A/ R5115Sxx1B: The RESETB pin voltage (V_{RESETB}) is fixed to low.
R5115xxx2C: The DOUT pin voltage (V_{DOUT}) is low and the WDO pin voltage (V_{WDO}) is fixed to the pull-up voltage.

When the input voltage (V_{IN}) is less than 1.52 V with 5-V pull-up voltage and 100-kΩ pull-up resistance, V_{RESETB}/ V_{DOUT} becomes indefinite, which means 0.1 V or more.



Voltage Regulator Voltage Setting

The voltage detector (VD) detects the output voltage drop of the voltage regulator (VR). If the VD reset voltage ($+V_{DET}$) is set to higher than the VR output voltage (V_{OUT}), VD continuously sends a reset signal even if VR output voltage (V_{OUT}) returns to the normal after detecting the output voltage drop of VR. To prevent this, the following conditions have to be met.

(VR Set Output Voltage) x 0.985 − 30 mV > (VD Set Detection Voltage) x 1.018 x 1.030

When using a device that is not meeting the above conditions, careful consideration must be given to the system operation before use.

Inhibit Function

When the INH pin voltage (V_{INH}) is low, the watchdog timer (WDT) stops monitoring a pulse. The WDO pin voltage (V_{WDO}) is fixed to high. The INH pin voltage (V_{INH}) is internally pulled up with a 400-kΩ (Typ.) resistor.

WADJ Function

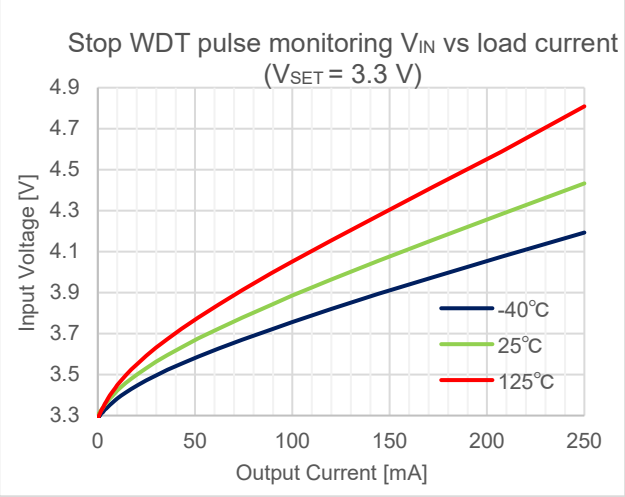
The R5115Sxx1A/ R5115xxx2C stops monitoring a pulse when the VR load current, which is a current flowing from the VOUT pin, is small. V_{WDO} is fixed to high. With the R5115Sxx1A, WDT stops monitoring a pulse when the load current is 1.0 mA (Typ.). With the R5115xxx2C, the load current can be set by using a resistor (R2) connected to the WADJ pin. The relationships between the resistance (R2) and the load current for deactivating the pulse monitoring of WDT ($I_{OWDTDEACT}$), and the resistance (R2) and the load current for activating the pulse monitoring of WDT ($I_{OWDTACT}$) are described as below.

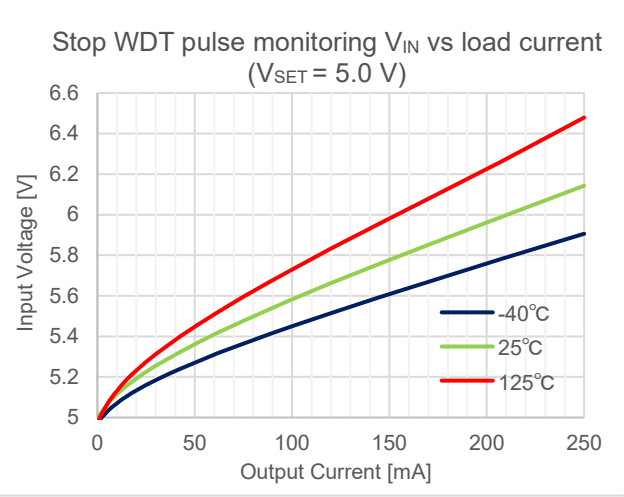
$I_{OWDTACT} = V_{WADJ\_TH} * \frac{I_{OUT}}{I_{WADJ}}(1) / R2$

$I_{OWDTDEACT} = V_{WADJ\_TH} * \frac{I_{OUT}}{I_{WADJ}}(2) / R2$

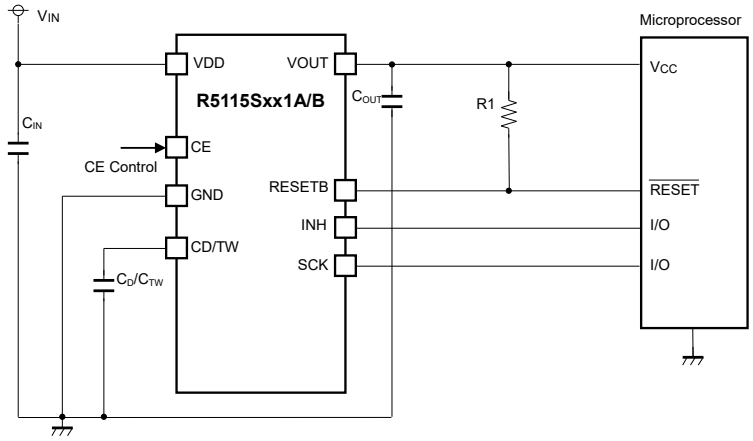
With the R5115Sxx1B, WDT monitors a pulse even when VR is in no-load state.

It is noted that WDT stops its operation regardless of load current of VR in the range of V_{IN} where the stable operation is not ensured owing to low V_{OUT}; Dropout Voltage (V_{DIF}): V_{IN} - V_{OUT} is ＜ 1.2 V (V_{SET} = 3.3 V, I_{OUT} = 100 mA). The output voltage from RESETB pin of R5115Sxx1A depends on only VD and WDO pin of R5115xxx2C is hold as “High.”

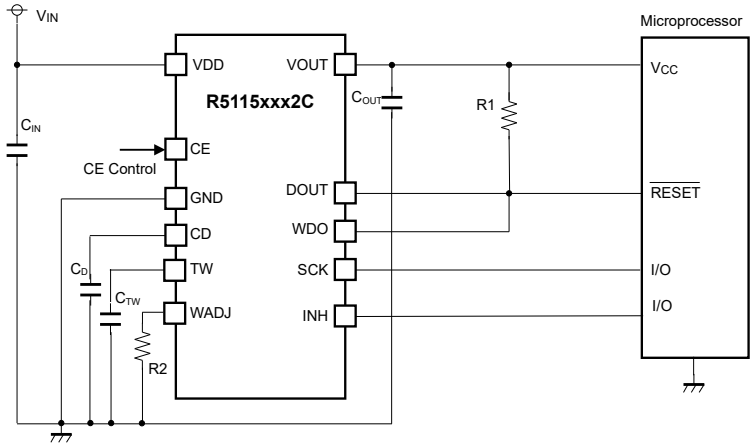




APPLICATION INFORMATION



R5115Sxx1A/B Typical Application Circuit



R5115xxx2C Typical Application Circuit

External Components

Symbol	Description
C_{IN}	0.1 µF, Ceramic Capacitor
C_{OUT}	0.1 µF, Ceramic Capacitor
C_{TW}	Capacitor for setting a WDT Refer to WDT Setting at Theory of Operation.
C_D	Capacitor for setting reset delay time Refer to Delay Operation and Reset Delay Time at *THEORY OF OPERATION*.
R1	Set the value for R1 considering the output current when the Nch is on and the leakage current when the Nch is off described in the Electrical Characteristics.
R2	Set the value for R2 considering the WADJ pin current ration and the WADJ pin threshold voltage described in the Electrical Characteristics.

TECHNICAL NOTES

The performance of a power source circuit using this device is highly dependent on a peripheral circuit. A peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, please be fully aware of the following points.

Phase Compensation

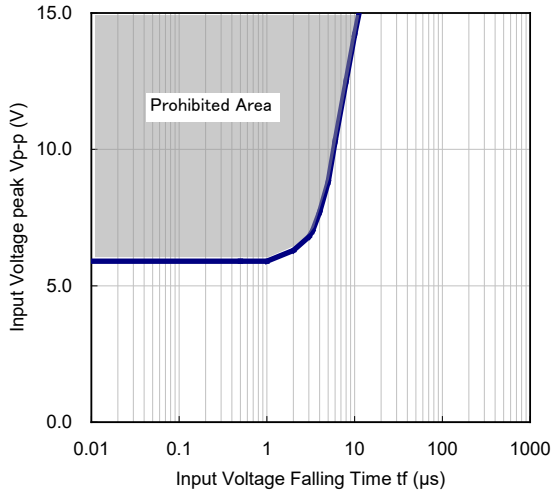
A phase compensation is provided to secure stable operation even when the load current is varied. For this purpose, use a 0.1-µF or more output capacitor (C_{OUT}) with good frequency characteristics and proper ESR (Equivalent Series Resistance). In case of using a tantalum type capacitor with a large ESR, the output might become unstable. Evaluate your circuit including consideration of frequency characteristics. Connect a 0.1-µF or more input capacitor (C_{IN}) between the VDD and GND pins with shortest-distance wiring.

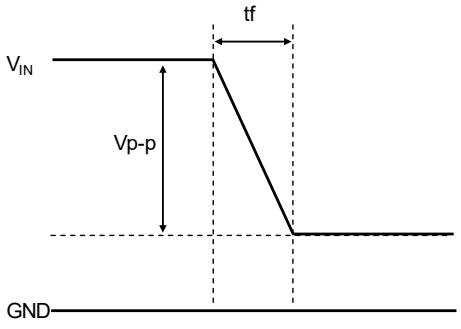
PCB Layout

Ensure that the VDD and GND lines are sufficiently robust. If their impedances are too high, noise pickup or unstable operation may result. Connect a 1.0 µF or more input capacitor (C_{IN}) between the VDD and GND pins with shortest-distance wiring. Also, connect an output capacitor (C_{OUT}) between the VOUT and GND pins with shortest-distance wiring.

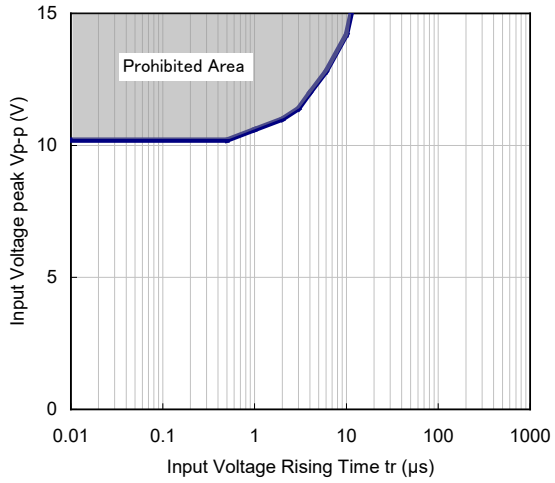
Input Voltage Fluctuation Prohibited Area

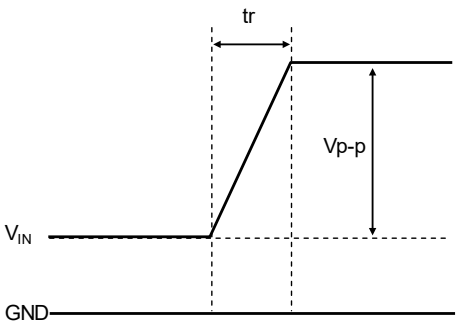
The input voltage fluctuation in the following area may cause false detection or false detection release, so should not be allowed.





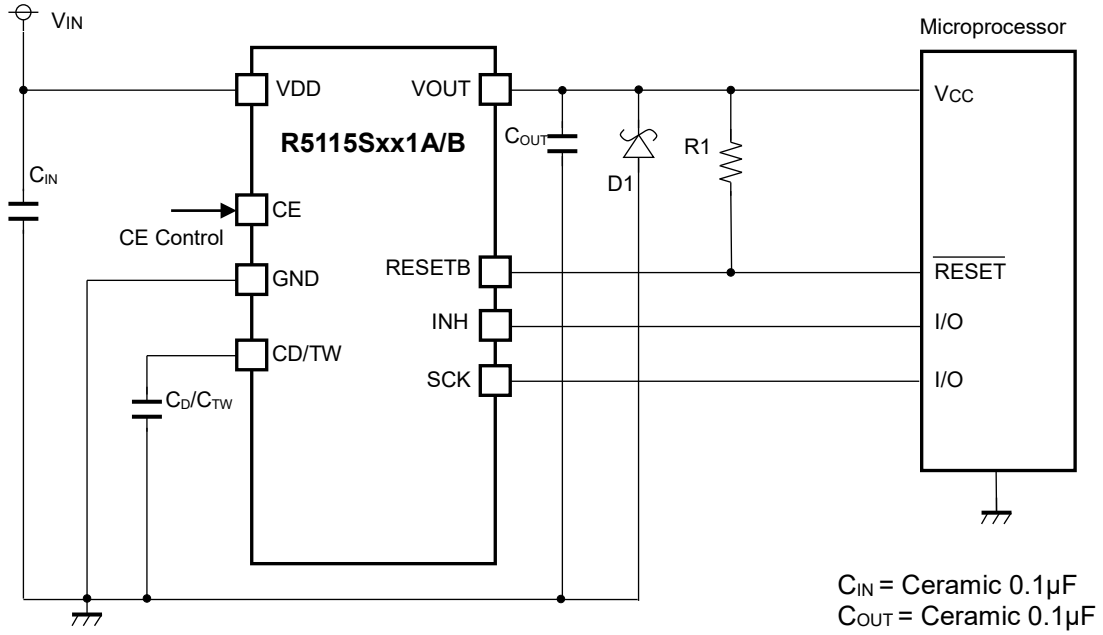
Input Voltage Falling Fluctuation Prohibited Area





Input Voltage Rising Fluctuation Prohibited Area

Typical Application Circuit with IC Chip Breakdown Prevention



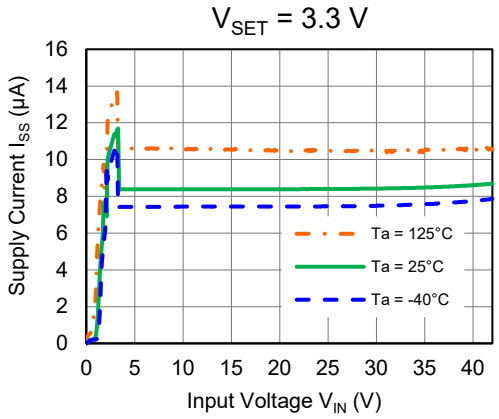
R5115Sxx1A/B Typical Application Circuit with IC Chip Breakdown Prevention

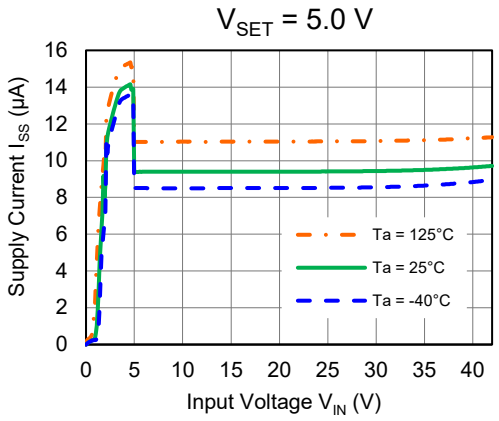
When a sudden surge of electrical current travels along the VOUT pin and GND due to a short-circuit, electrical resonance of a circuit involving an output capacitor (C_{OUT}) and a short circuit inductor generates a negative voltage and may damage the device or the load devices. Connecting a schottky diode (D1) between the VOUT pin and GND has the effect of preventing damage to them.

TYPICAL CHARACTERISTICS

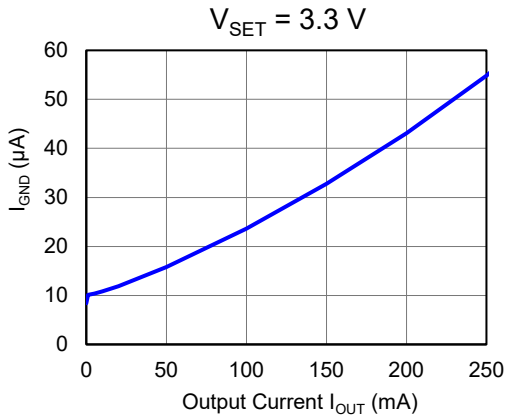
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

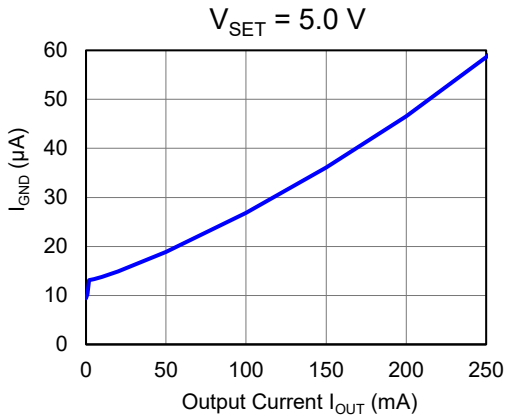
1) Supply Current vs. Input Voltage



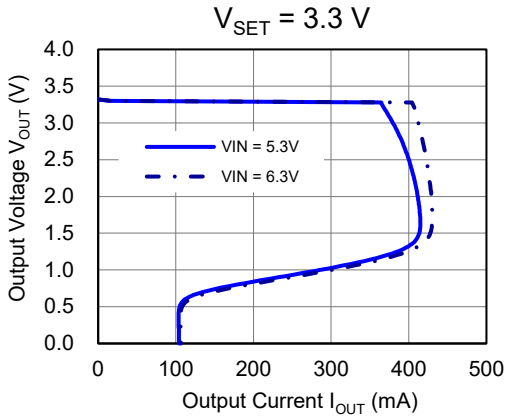


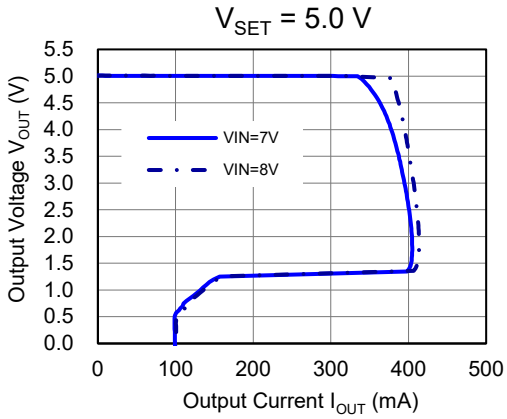
2) GND Pin Current vs. Output Current (Ta = 25°C)



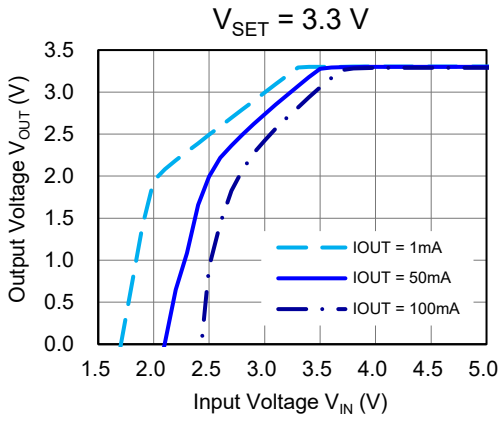


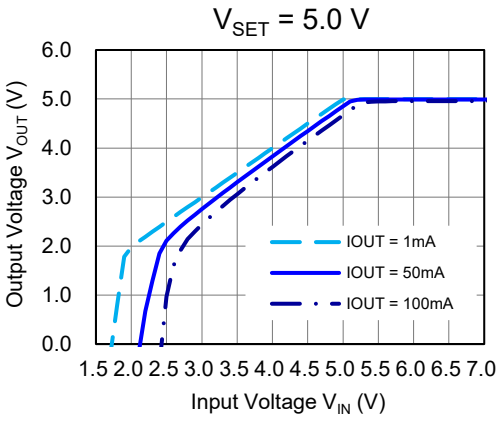
3) Output Voltage vs. Output Current (Ta = 25°C)



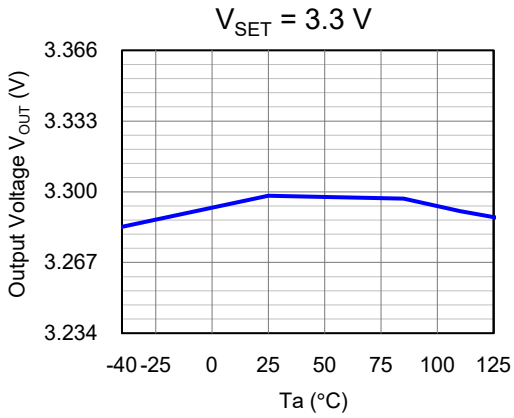


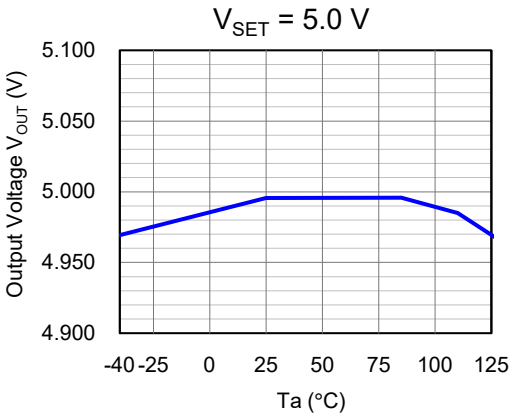
4) Output Voltage vs. Input Voltage (Ta = 25°C)



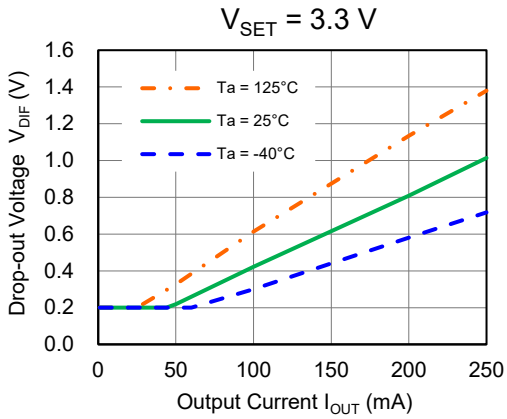


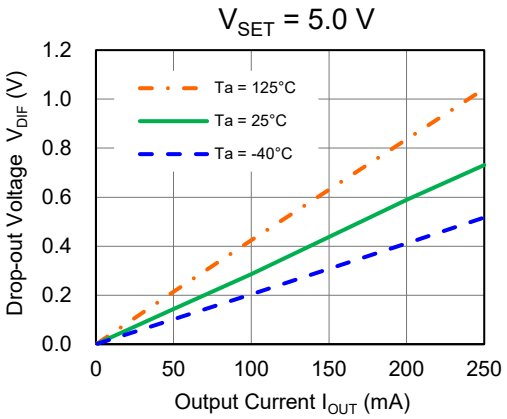
5) Output Voltage vs. Ambient Temperature (V_{IN} = 14 V, I_{OUT} = 1 mA)



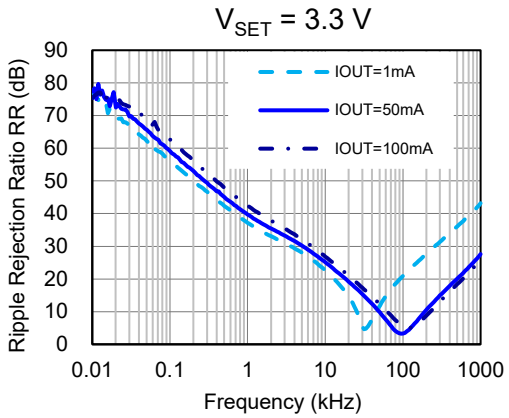


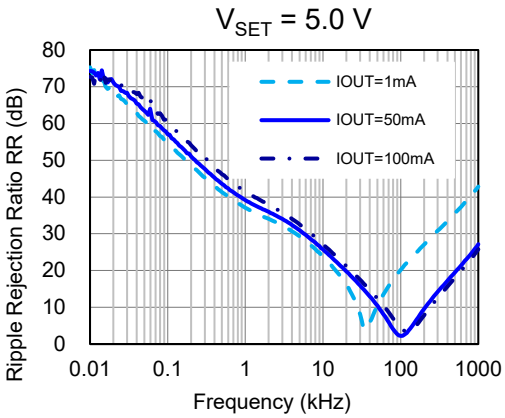
6) Dropout Voltage vs. Output Current



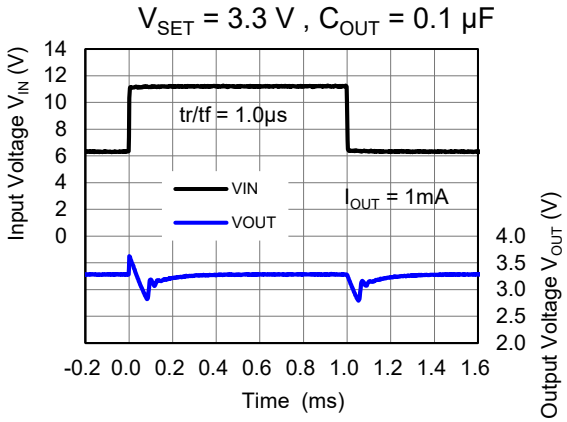


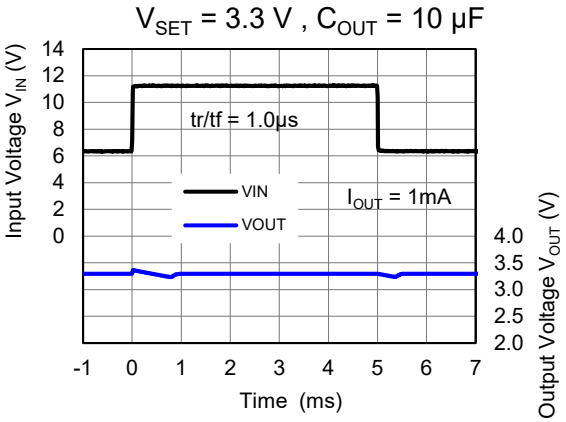
7) Ripple Rejection vs. Frequency (Ta = 25°C, Ripple = 0.2 Vpp)

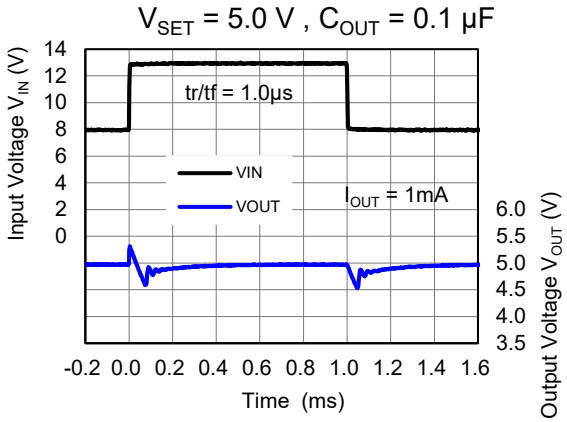


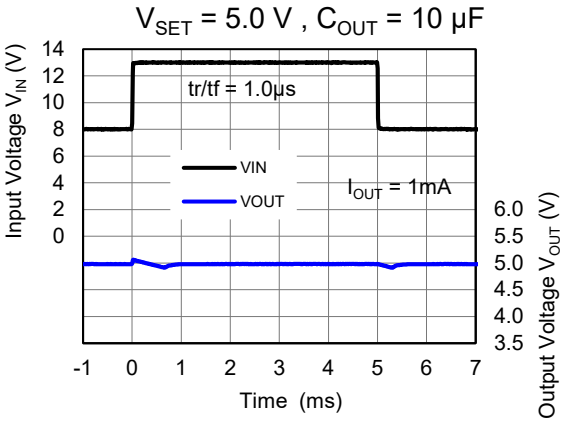


8) Input Transient Response (Ta = 25°C)

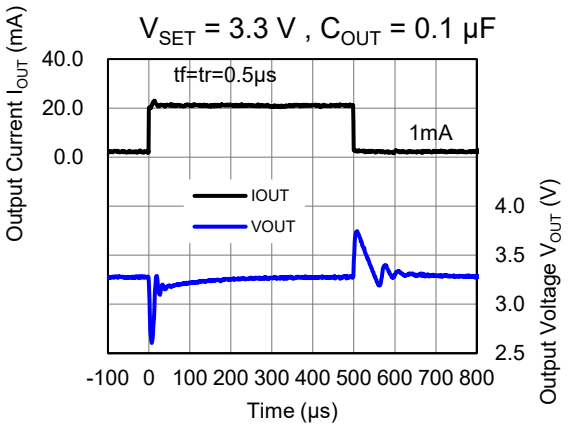


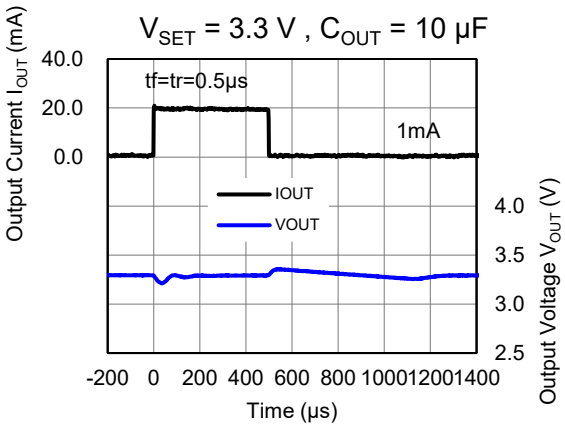


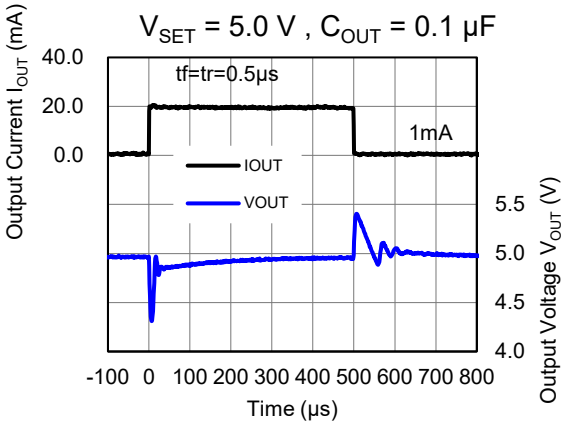


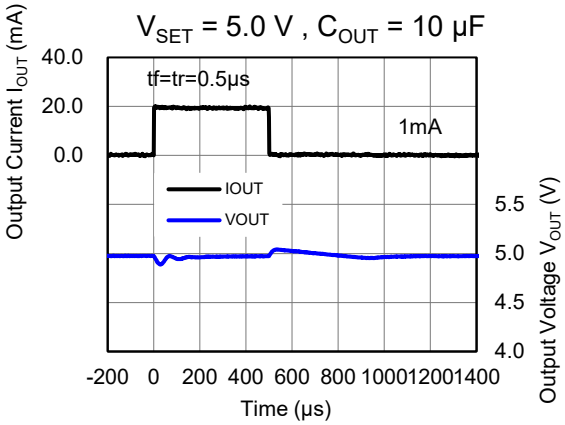


9) Load Transient Response (Ta = 25°C)

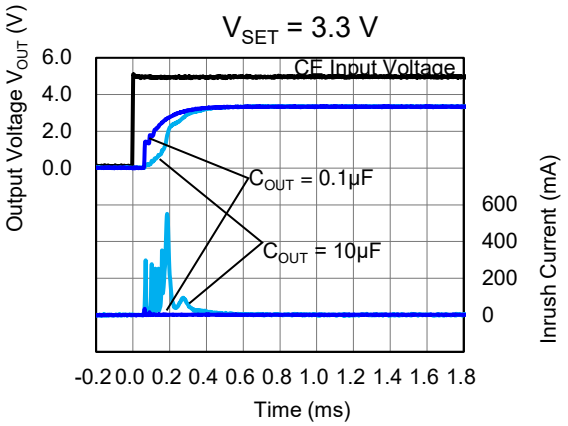


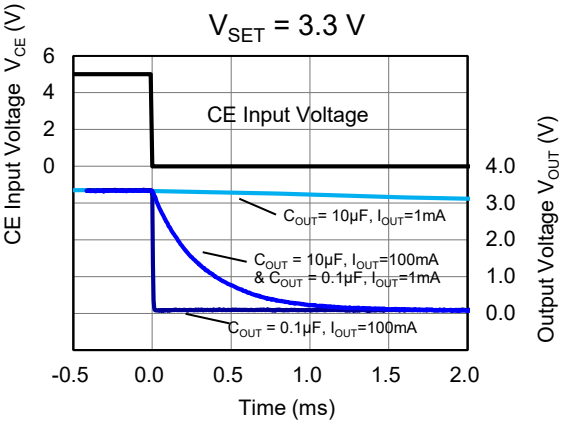


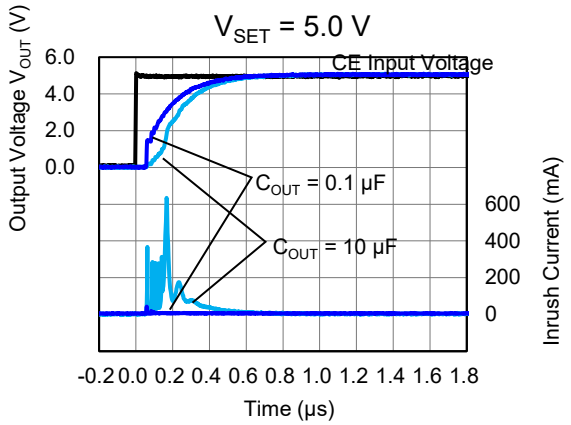


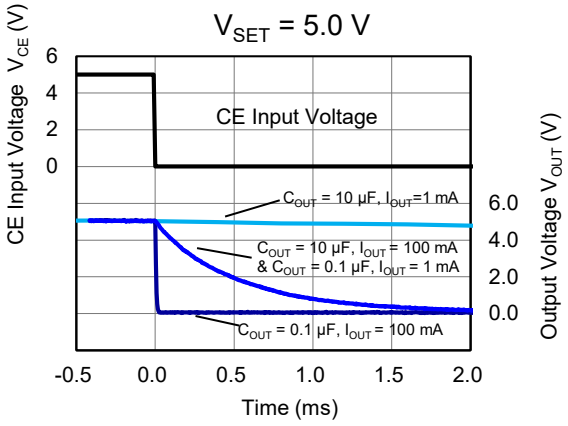


10) CE Transient Response (Ta = 25°C, V_{IN} = 14 V, I_{OUT} = 1 mA, C_{OUT} = 0.1 µF/10 µF)

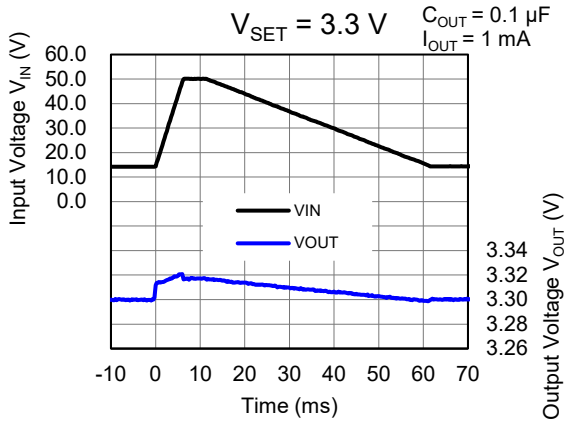


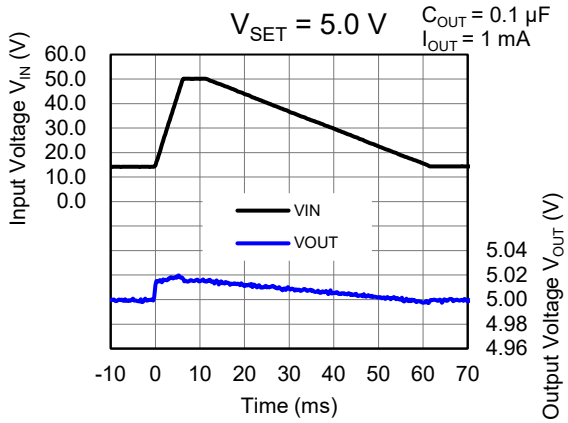




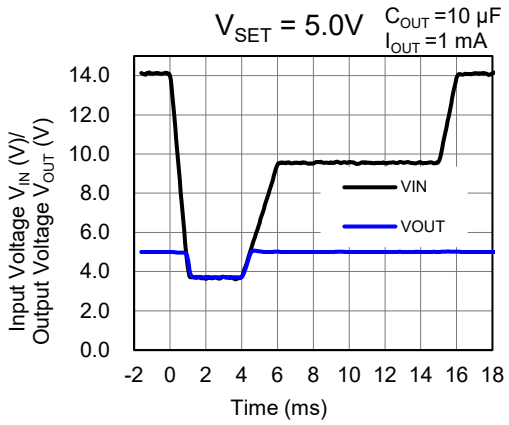


11) Load Dump (Ta = 25°C)

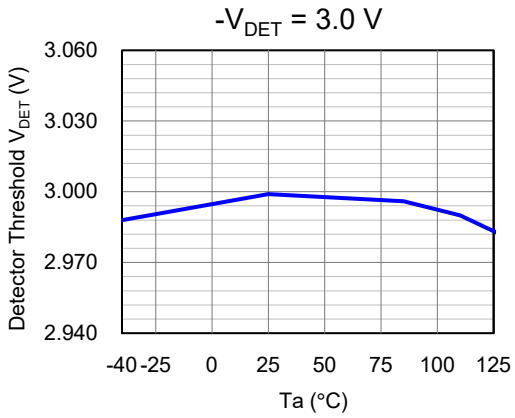


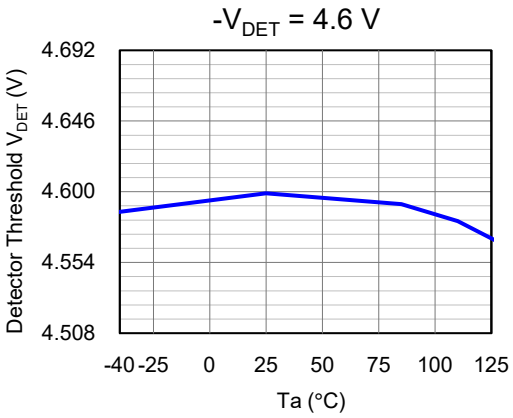


12) Cranking (Ta = 25°C)

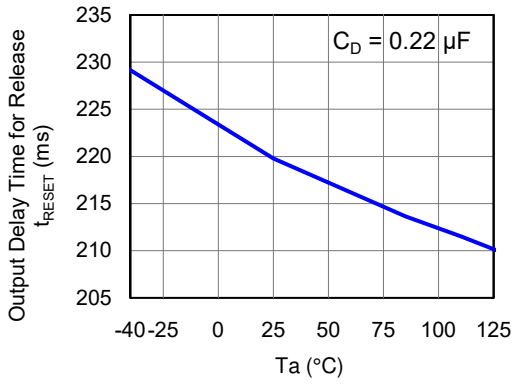


13) Detection Voltage vs. Ambient Temperature

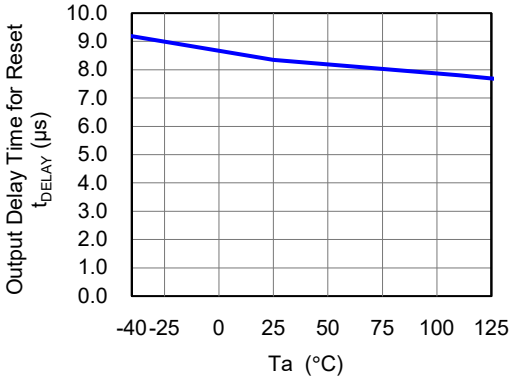




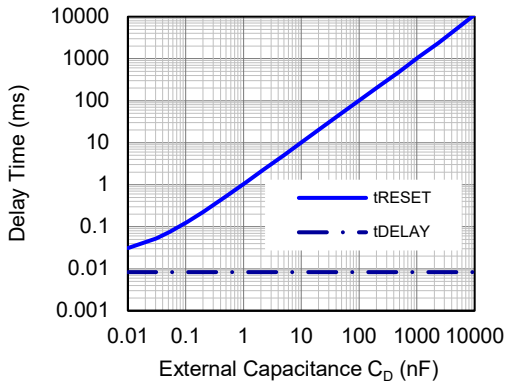
14) Release Delay Time vs. Ambient Temperature



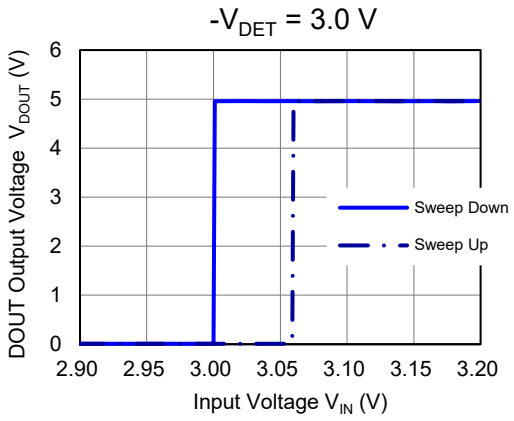
15) Detection Delay Time vs. Ambient Temperature

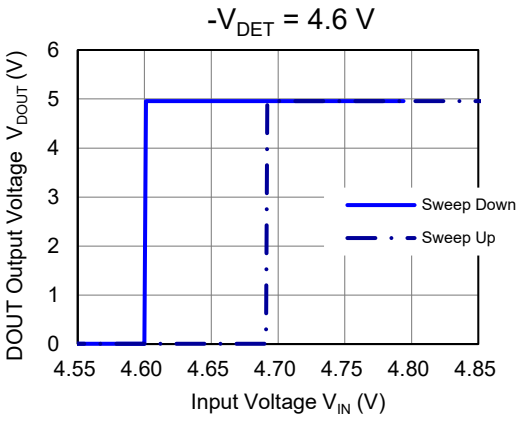


16) Release Delay and Detection Delay Time vs. CD Pin External Capacitance

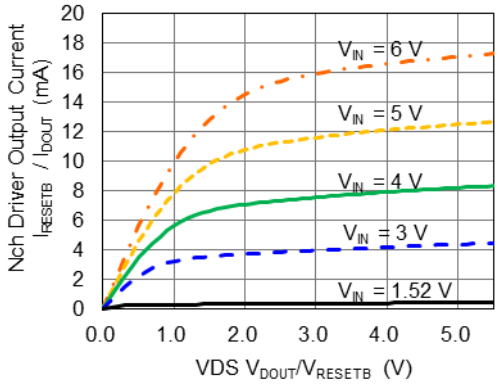


17) DOUT Pin Voltage vs. Input Voltage (DOUT pulled-up to 5 V with 100 kΩ)

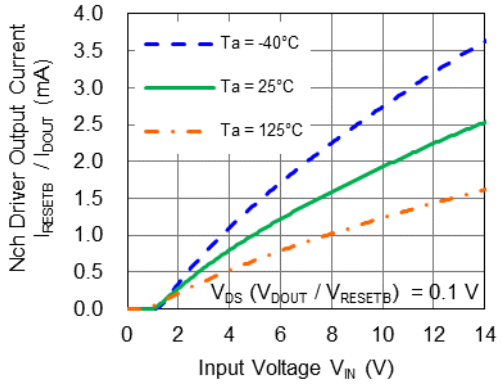




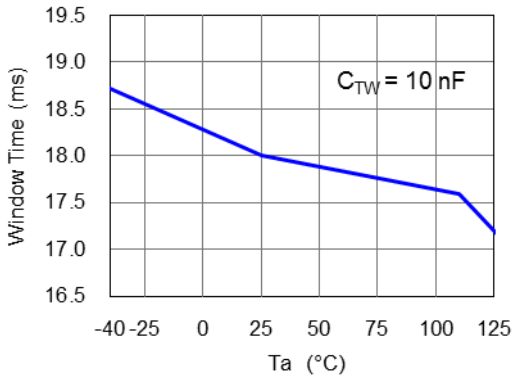
18) RESETB/DOUT Driver Output Current vs. V_{DS}



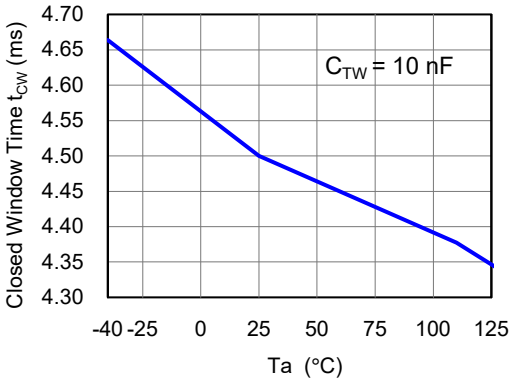
19) RESETB/DOUT Driver Output Current vs. Input Voltage



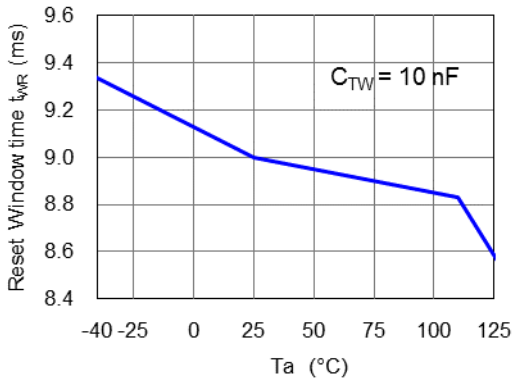
20) Open Window Time/Pulse Ignoring Time vs. Ambient Temperature



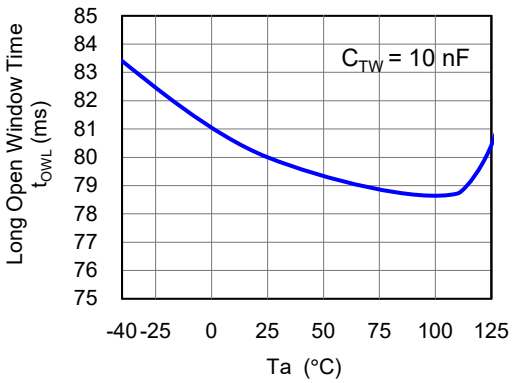
21) Closed Window Time vs. Ambient Temperature



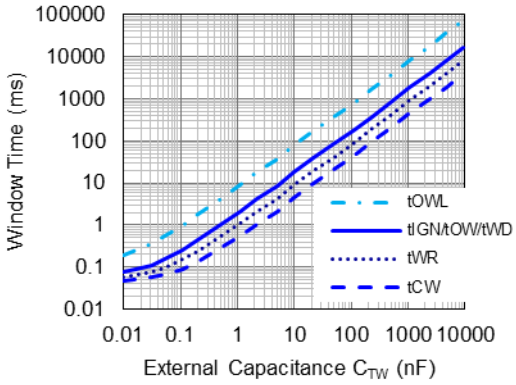
22) Reset Time vs. Ambient Temperature



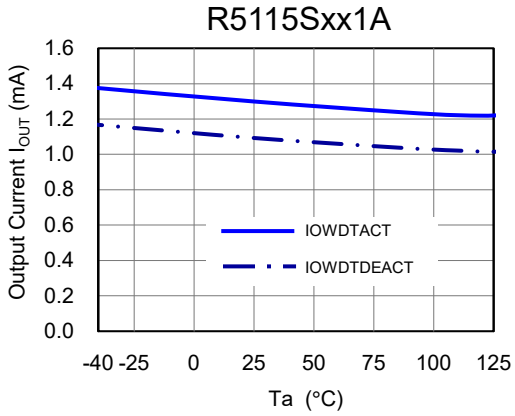
23) Long Open Window Time vs. Ambient Temperature



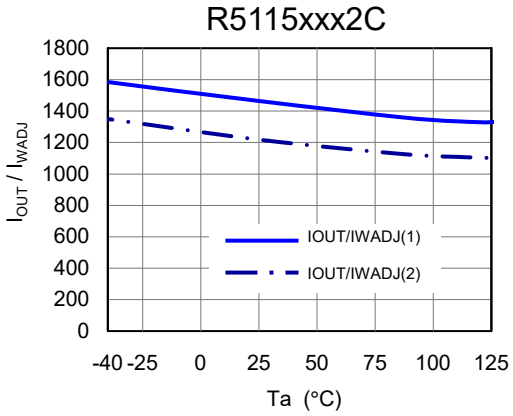
24) WDT t_{WD} / t_{OW} / t_{CW} / t_{IGN} / t_{OWL} / t_{RST} vs. TW Pin External Capacitance



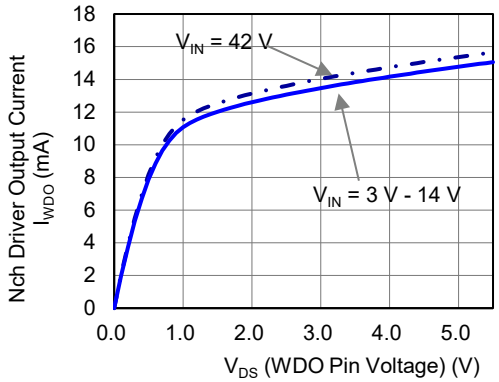
25) WDT Monitoring Threshold Load Current vs. Ambient Temperature



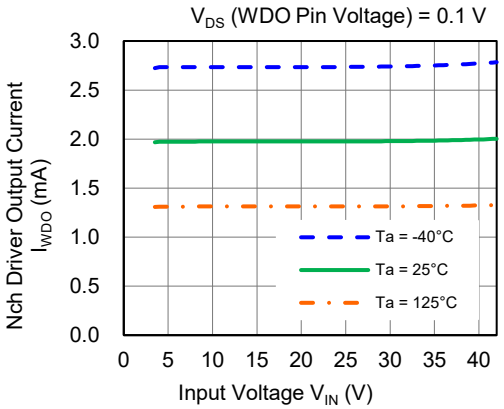
26) WADJ Pin Current Ratio vs. Ambient Temperature



27) WDO Driver Output Current vs. V_{DS}



28) WDO Driver Output Current vs. Input Voltage



Ver. B

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

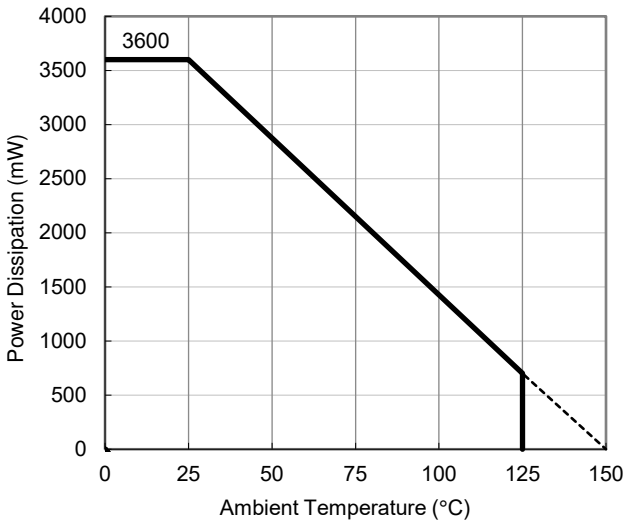
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 21 pcs

Measurement Result (Ta = 25°C, Tjmax = 150°C)

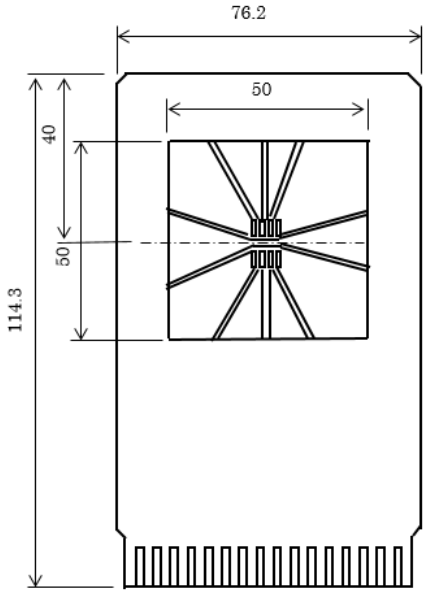
Item	Measurement Result
Power Dissipation	3600 mW
Thermal Resistance (θja)	θja = 34.5°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 10°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter

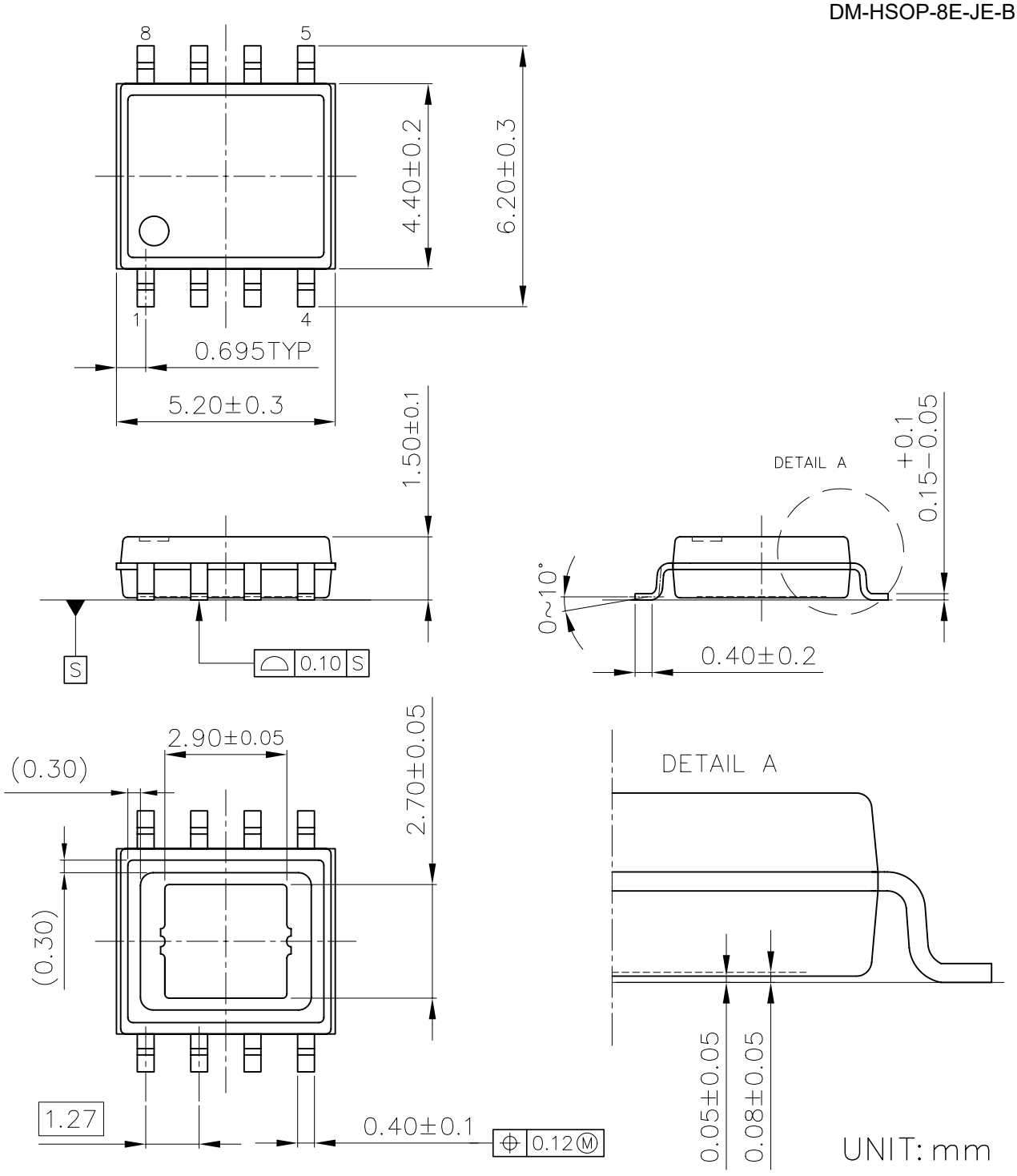


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

DM-HSOP-8E-JE-B



HSOP-8E Package Dimensions

Ver. B

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

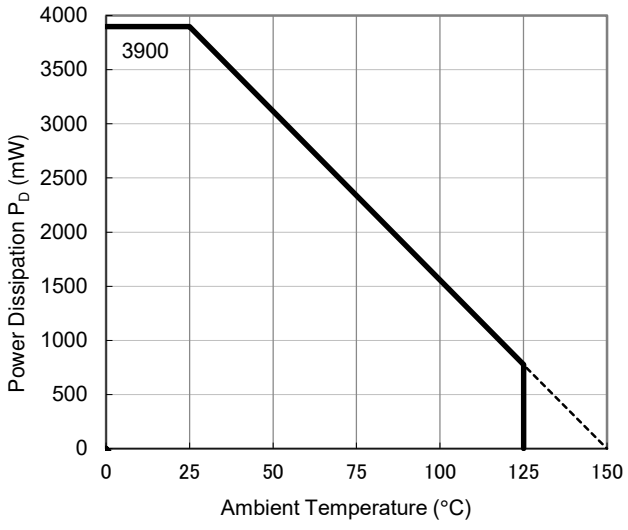
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 21 pcs

Measurement Result (Ta = 25°C, Tjmax = 150°C)

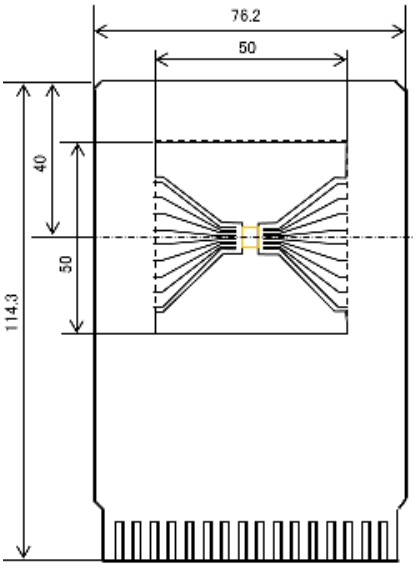
Item	Measurement Result
Power Dissipation	3900 mW
Thermal Resistance (θja)	θja = 32°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 8°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter

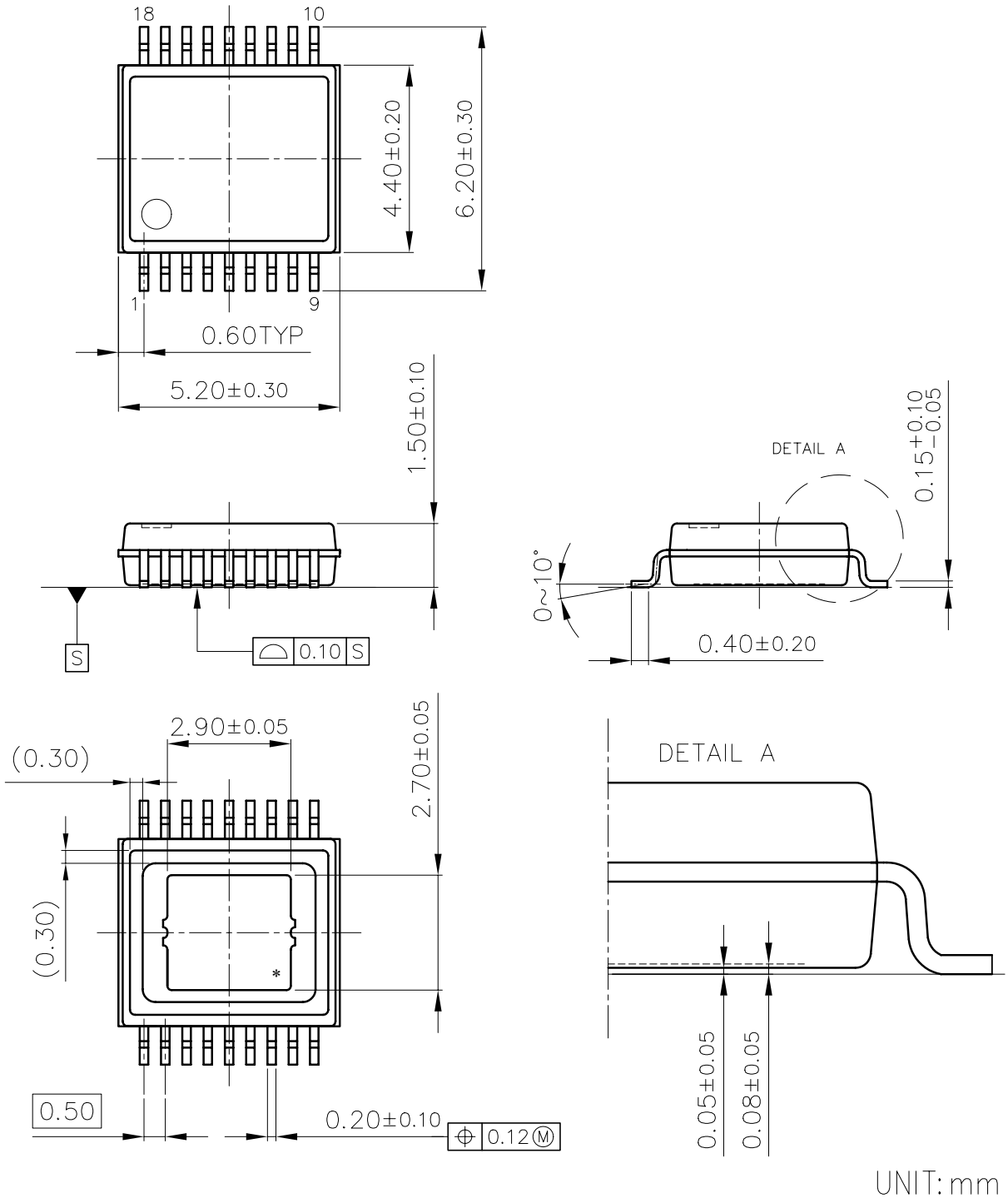


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

DM-HSOP-18-JE-B



HSOP-18 Package Dimensions

PD-HQFN0808-28-(125150)-JE-A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

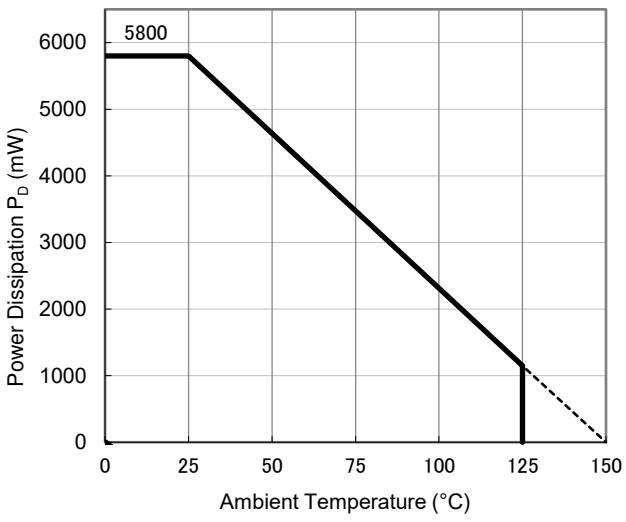
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 72 pcs

Measurement Result (Ta = 25°C, Tjmax = 150°C)

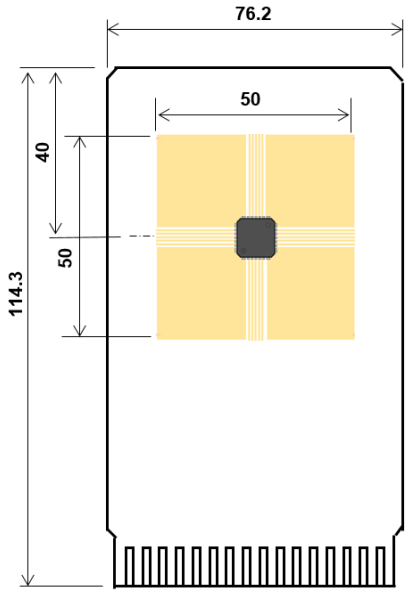
Item	Measurement Result
Power Dissipation	5800 mW
Thermal Resistance (θja)	θja = 21.5°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 5°C/W

θja: Junction-to–ambient thermal resistance.

ψjt: Junction–to-top of package thermal characterization parameter

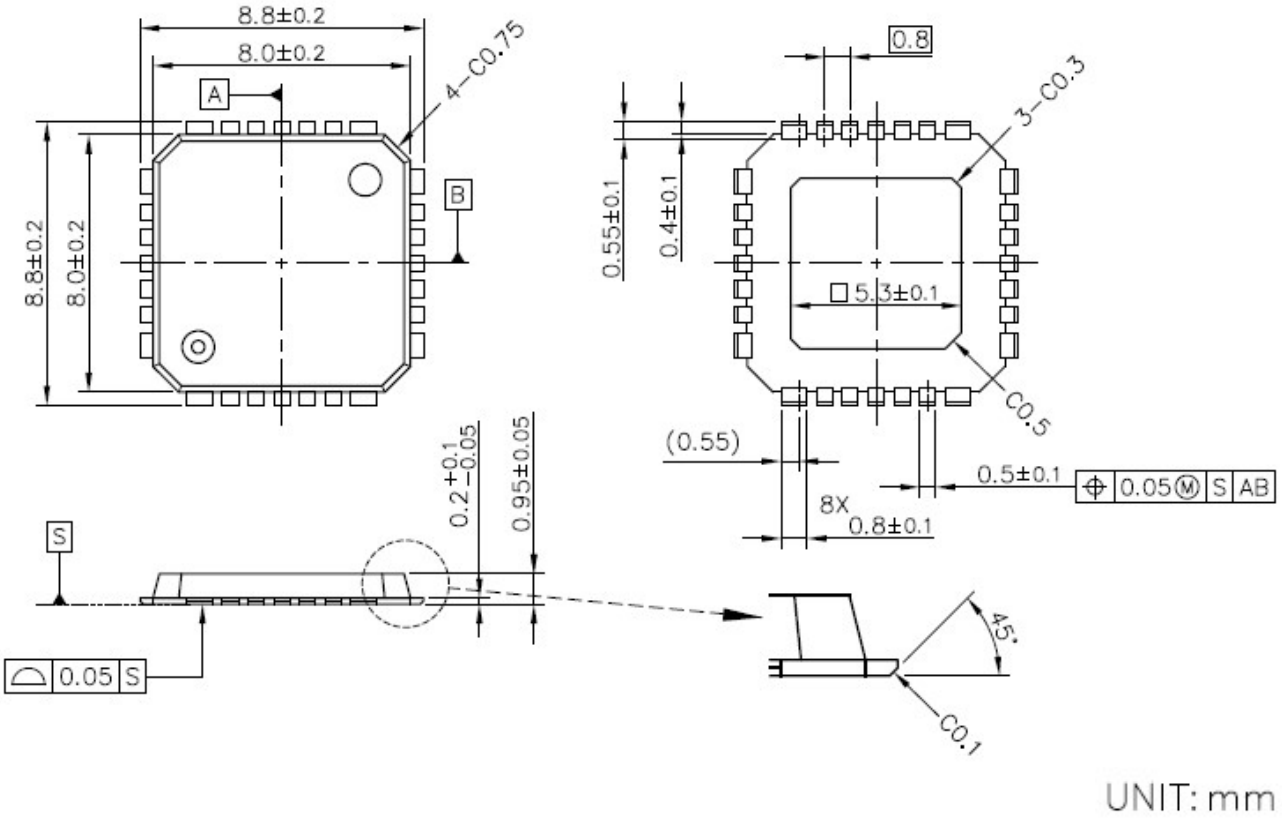


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

DM-HQFN0808-28-JE-A



HQFN0808-28 Package Dimensions

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