Description

The P9225-R is a high-efficiency wireless power receiver (Rx) capable of operating in both WPC and PMA protocols. Using magnetic inductive charging technology, the receiver converts an AC power signal from a resonant tank into a regulated DC output voltage ranging from 4.5V to 5.5V. The integrated, low RDS_{ON} synchronous rectifier and ultra-low dropout linear (LDO) regulator offers high efficiency making the product ideally suited for battery-operated applications.

The P9225-R includes an industry-leading 32-bit ARM® Cortex®-M0 microprocessor offering a high level of programmability. The P9225-R also features a programmable current limit and a patented over-voltage protection function eliminating the need for additional capacitors generally used by the receivers minimizing the external component count and cost. Together with the P9038-R transmitter (T_X), the P9225-R is a complete wireless power system solution for power applications up to 5W.

The P9225-R is available in a 52-WLCSP package, and it is rated for 0°C to 85°C ambient operating temperature range.

Typical Applications

- Headsets, tablets
- Digital cameras
- Portable media player
- Accessories
- Medical

Features

- Single-chip solution supporting up to 5W applications
- WPC-1.2.4 compliant, PMA SR1 compatible
- Patented over-voltage protection clamp eliminating external capacitors
- 82% peak DC-to-DC efficiency with P9038-R T_X
- Fully integrated synchronous rectifier with low RDS(ON) switches
- Programmable output voltage: 4.5V to 5.5V
- Embedded 32-bit ARM® Cortex®-M0 processor
- Dedicated remote temperature sensing
- Programmable current limit
- Active-low enable pin for electrical on/off
- Active-high End-of-Charge input pin
- Open-drain interrupt flag
- Support for I2C interface
- 0°C to +85°C ambient operating temperature range
- 52-WLCSP (2.64 × 3.94 mm; 0.4mm pitch)

Typical Application Circuit

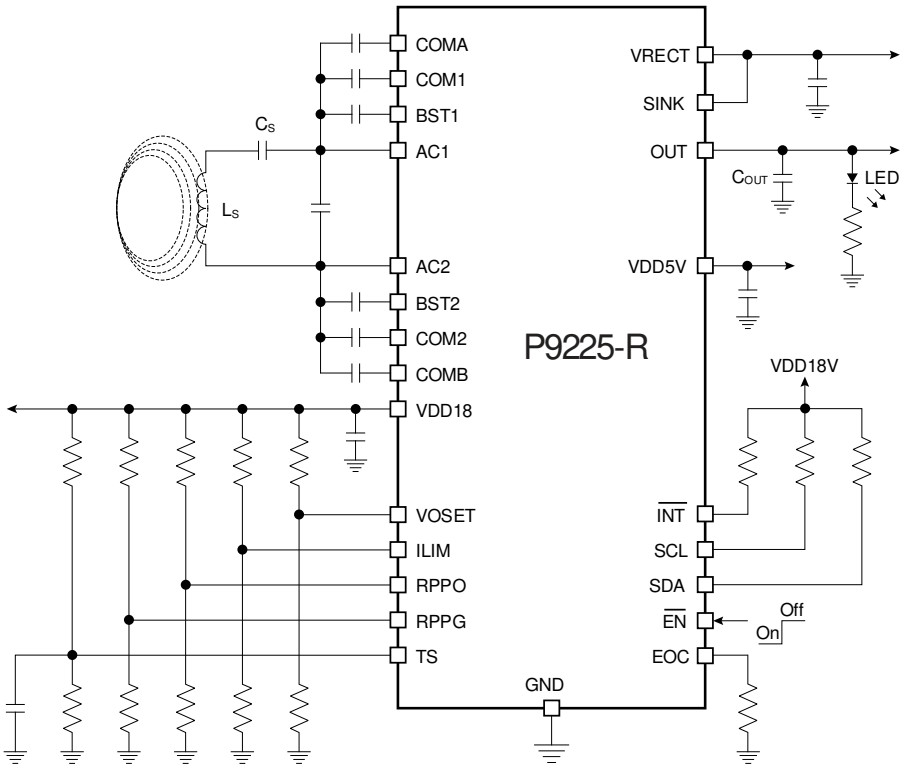

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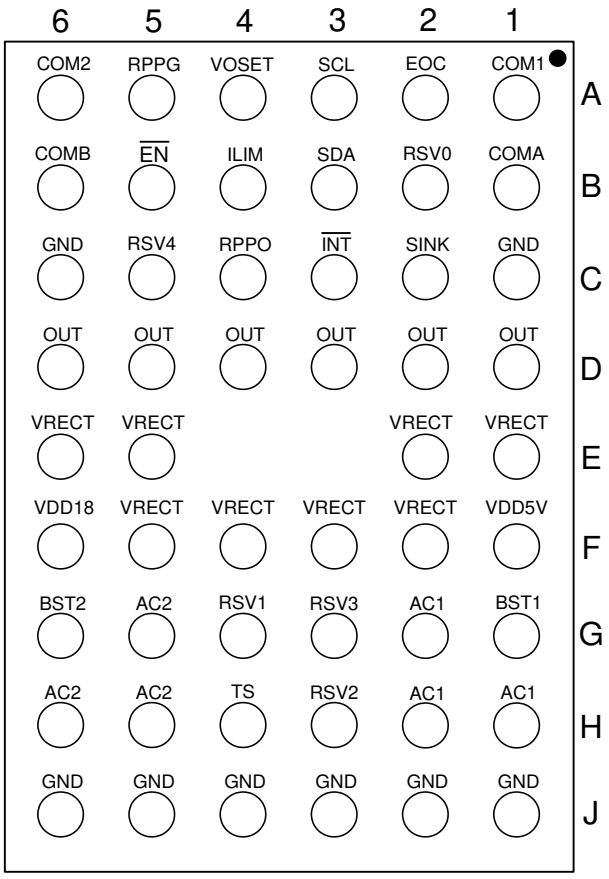
Figure 1. Pin Assignments – Bottom View



Bottom View

2. Pin Descriptions

Table 1. Pin Descriptions

Pins	Name	Type	Function
A1	COM1	Output	Open-drain output used to communicate with the transmitter. Connect a 47nF capacitor from AC1 to COM1.
A2	EOC	Input	Active-HIGH End-of-Charge input pin. When connected to logic HIGH, the device sends an End Power Transfer (i.e., charge complete) packet to the transmitter to terminate power delivery and shuts down. Use a 10kΩ resistor to GND to pull this pin down to logic LOW by default.
A3	SCL	Input	Serial clock line. Open-drain pin. Connect this pin to a 5.1 kΩ resistor to VDD18 pin if I2C access by external AP is used. Otherwise, this pin can be left floating.
A4	VOSET	Input	Programming pin for setting the output voltage. Connect this pin to the center tap of the external resistor divider to set the output voltage. For more information, refer to section 8.2 for different output voltage settings.
A5	RPPG	Input	Received Power Packet Gain (RPPG) calibration pin for foreign object detection (FOD) tuning. Connect this pin to the center tap of the external resistor divider to set the gain of the FOD. The FOD is disabled by connecting RPPG and RPPO to GND. Do not leave this pin floating.
A6	COM2	Output	Open-drain output used to communicate with the transmitter. Connect a 47nF capacitor from AC2 to COM2.
B1	COMA	Output	Open-drain output used to communicate with the transmitter. Connect a 47nF capacitor from AC2 to COMA. If PMA mode is not used, this pin can be left floating.
B2	RSV0	–	Reserved pin.
B3	SDA	Input/Output	Serial data line. Open-drain pin. Connect this pin to a 5.1 kΩ resistor to VDD18 pin if I2C access by external AP is used. Otherwise, this pin can be left floating.
B4	ILIM	Input	Programmable over-current limit pin. Connect this pin to the center tap of a resistor divider to set the current limit. For more information about the current limit function, see section 8.5.
B5	$\overline{EN}$	Input	Active-LOW enable pin. Pulling this pin to logic HIGH forces the device into Shut Down Mode. When connected to logic LOW, the device is enabled. Do not leave this pin floating.
B6	COMB	Output	Open-drain output used to communicate with the transmitter. Connect a 47nF capacitor from AC2 to COMB. If PMA mode is not used, this pin can be left floating.
C1, C6, J1, J2, J3, J4, J5, J6	GND	GND	Ground.
C2	SINK	Output	Open-drain output for controlling the rectifier clamp. Short this pin to the VRECT pin.
C3	$\overline{INT}$	Output	Interrupt flag pin. This is an open-drain output that signals fault interrupts. It is pulled LOW if any of these faults exist: an over-voltage is detected, an over-current condition is detected, the die temperature exceeds 140°C, or an external over-temperature condition is detected on the TS pin. It is also asserted LOW when $\overline{EN}$ is HIGH. Connect to VDD18 through a 10kΩ resistor. See section 8.6 for additional conditions affecting the interrupt flag.
C4	RPPO	Input	Received Power Packet Offset (RPPO) calibration pin for FOD tuning. Connect this pin to the center tap of the external resistor divider to set the offset of the FOD. The FOD is disabled by connecting RPPG and RPPO to GND. Do not leave this pin floating.
C5	RSV4	Input	Reserved. This pin must be connected to a 10kΩ resistor to the VDD18 pin.

Pins	Name	Type	Function
D1, D2, D3, D4, D5, D6	OUT	Output	Regulated output voltage pins. On each of these pins, connect a 22µF capacitor to GND. The default voltage is set to 5V when the VOSET pin is pulled up to VDD18 pin through a 10kΩ resister. For more information about VOSET, see section 8.2.
E1, E2, E5, E6, F2, F3, F4, F5	VRECT	Output	Output voltage of the synchronous rectifier bridge. On each of these pins, connect two 22µF capacitors and a 0.1µF capacitor in parallel to GND. The rectifier voltage dynamically changes as the load changes.
F1	VDD5V	Output	Internal 5V regulator output voltage for internal use. Connect a 1µF capacitor from this pin to ground. Do not load the pin.
F6	VDD18	Output	Internal 1.8V regulator output voltage. Connect a 1µF capacitor from this pin to ground. Do not load the pin.
G1	BST1	Output	Boost capacitor for driving the high-side switch of the internal rectifier. Connect a 15nF capacitor from the AC1 pin to BST1.
G2, H1, H2	AC1	Input	AC input power. Connect these pins to the resonant capacitance C_S (C1, C2, C3, and C5 in Figure 22).
G3	RSV3	–	Reserved pin. This pin must be connected to OUT pin.
G4	RSV1	–	Reserved pin.
G5, H5, H6	AC2	Input	AC input power. Connect to the Rx coil (L1 in Figure 22).
G6	BST2	Output	Boost capacitor for driving the HIGH-side switch of the internal rectifier. Connect a 15nF capacitor from the AC2 pin to BST2.
H3	RSV2	–	Reserved pin. This pin must be connected to the OUT pin.
H4	TS	Input	Remote temperature sensor for over-temperature shutdown. Connect to the NTC thermistor network. If not used, connect this pin to VDD18 pin through the 10kΩ resistor.

3. Absolute Maximum Ratings

Stresses greater than those listed as absolute maximum ratings in Table 2 could cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods might affect reliability.

Table 2. Absolute Maximum Ratings

Symbol/Pins [a], [d]	Parameter	Conditions	Minimum [b]	Maximum [b]	Units
AC1 [c], AC2 [c], COM1, COM2, COMA, COMB	Absolute Maximum Pin Voltage		-0.3	20	V
$\overline{EN}$	Absolute Maximum Pin Voltage		-0.3	28	V
SINK, VRECT	Absolute Maximum Pin Voltage		-0.3	24	V
ILIM, RPPG, RPPO, VDD18, VOSET	Absolute Maximum Pin Voltage		-0.3	2	V
$\overline{INT}$, SCL, SDA, TS, VDD5V, EOC	Absolute Maximum Pin Voltage		-0.3	6	V
BST1	Absolute Maximum Pin Voltage		-0.3	AC1+6	V
BST2	Absolute Maximum Pin Voltage		-0.3	AC2+6	V
OUT	Absolute Maximum Pin Voltage		-0.3	14.4	V
SINK	Maximum Pin Current		–	1	A
COM1, COM2	Maximum RMS Pin Current		–	500	mA
AC1, AC2	Maximum RMS Pin Current		–	2	A

[a] Absolute maximum ratings are not provided for reserved pins (RSV0, RSV1, RSV2, RSV3, and RSV4). These pins are not used in the application.

[b] All voltages are referenced to ground unless otherwise noted.

[c] During synchronous rectifier dead time, the voltage on the AC1 and AC2 pins is developed by current across the internal power FET's body diodes, and it might be lower than -0.3 V. This is normal behavior and does not negatively impact the functionality or reliability of the product.

[d] For the test conditions for the absolute maximum ratings specifications, the P9225-R chip characterization for the operating ambient temperature (T_{AMB}) specification has been performed down to -10°C only. Design simulation indicates normal operation down to -45°C. Limited bench functionality tests normal operation down to -40°C.

Table 3. ESD Information

Test Model	Pins	Ratings	Units
HBM	All pins except RSV0, RSV1, and RSV4	2	kV
	RSV2 and RSV3 pins	1	kV
CDM	All pins	500	V

4. Thermal Characteristics

Table 4. Package Thermal Information

Note: This thermal rating was calculated on a JEDEC 51 standard 4-layer board with dimensions 76.2 x 114.3 mm in still-air conditions.

Symbol	Description	WLCSP Rating 8 Thermal Balls	Units
θ_{JA}	Thermal Resistance, Junction to Ambient [a]	47	°C/W
θ_{JC}	Thermal Resistance, Junction to Case	0.202	°C/W
θ_{JB}	Thermal Resistance, Junction to Board	4.36	°C/W
T_J	Operating Junction Temperature [a]	-5 to +125	°C
T_{AMB}	Ambient Operating Temperature [a]	0 to +85	°C
T_{STOR}	Storage Temperature	-55 to +150	°C
T_{BUMP}	Maximum Soldering Temperature (Reflow, Pb-Free)	260	°C

[a] The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} – T_{AMB}) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

5. Electrical Characteristics

Table 5. Electrical Characteristics

Note: Unless otherwise noted, VRECT = 5.5V; C_{OUT} = 4.7µF; $\overline{EN}$ = LOW; and T_J = 0°C to 125°C. Typical values are at 25°C.

Note: See important table notes at the end of this table.

Symbol	Description	Conditions	Minimum	Typical	Maximum	Units
Under-Voltage Lock-Out (UVLO)						
V_{UVLO_Rising}	UVLO Rising	Rising voltage on VRECT		2.9	2.98	V
V_{UVLO_HYS}	UVLO Hysteresis	VRECT falling		200		mV
Over-Voltage Protection						
V_{OVP-DC}	DC Over-Voltage Protection	Rising voltage on VRECT		12		V
$V_{OVP-HYS}$	Over-Voltage Hysteresis			1		V
Quiescent Current						
I_{ACTIVE_SUPLY}	Supply Current	EN = LOW, No load; VRECT = 5.5V		3.0		mA
I_{SHD}	Shut Down Mode Current	EN = HIGH, VRECT = 5.5V		500		µA
VDD18 Voltage						
V_{VDD18}	VDD18 Pin Output Voltage [a]	I_{VDD18} = 10mA, C_{VDD18} = 1µF	1.62	1.8	1.98	V
VDD5V Voltage						
V_{VDD5V}	VDD5V Pin Output Voltage [a]	I_{VDD5V} = 10mA, C_{VDD5V} = 1µF	4.5	5	5.5	V

Symbol	Description	Conditions	Minimum	Typical	Maximum	Units
Low Drop-Out (LDO) Regulator						
I_{OUT_MAX}	Maximum Output Current			1.25		A
V_{OUT_5V}	5V Output Voltage	VOSET= 1.8V, VRECT=5.5V		5		V
Analog to Digital Converter						
N	Resolution			12		Bit
f_{SAMPLE}	Sampling Rate			67.5		kSa/s
Channel	Number of Channels			8		
$V_{IN,FS}$	Full-Scale Input Voltage			2.1		V
$\overline{EN}$ Pin						
V_{IH_EN}	Input Threshold HIGH		1.4			V
V_{IL_EN}	Input Threshold LOW				0.25	V
I_{IL_EN}	Input Current LOW	V_{EN} = 0V	-1		1	µA
I_{IH_EN}	Input Current HIGH	V_{EN} = 5V		2.5		µA
EOC pin						
V_{IH_EOC}	Input Threshold HIGH		1.4			V
V_{IL_EOC}	Input Threshold LOW				0.7	V
I_{IL_EOC}	Input Current LOW	V_{EOC}= 0V	-1		1	µA
I_{IH_EOC}	Input Current HIGH	V_{EOC}= 1.8V	-1		1	µA
VOSET, ILIM, TS, RPPO, RPPG						
I_{IL}	Input Current LOW	V_{VOSET}, V_{ILIM}, V_{TS}, V_{RPPO}, V_{RPPG} = 0V	-1		1	µA
I_{IH}	Input Current HIGH	V_{VOSET}, V_{ILIM}, V_{TS}, V_{RPPO}, V_{RPPG} = 1.8V	-1		1	µA
$\overline{INT}$ pin						
I_{LKG}	Input Leakage Current	$V_{\overline{INT}}$ = 0V and 5V	-1		1	µA
V_{OL}	Output Logic LOW	I_{OL} = 8mA			0.36	V
I2C Interface – SCL, SDA						
V_{IL}	Input Threshold LOW				0.7	V
V_{IH}	Input Threshold HIGH		1.4			V
I_{LKG}	Input Leakage Current	V_{SCL}, V_{SDA} = 0V and 5V	-1		1	µA
V_{OL}	Output Logic LOW	I_{OL} = 8mA			0.36	V
f_{SCL}	Clock Frequency				400	kHz
$t_{HD,STA}$	Hold Time (Repeated) for START Condition		0.6			µs
$t_{HD:DAT}$	Data Hold Time		0			ns
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs

Symbol	Description	Conditions	Minimum	Typical	Maximum	Units
$t_{SU:STA}$	Set-up Time for Repeated START Condition		0.6			µs
t_{BUF}	Bus-Free Time Between STOP and START Condition		1.3			µs
C_B	Capacitive Load for SCL and SDA			150		pF
C_I	SCL, SDA Input Capacitance			5		pF
Thermal Shutdown						
T_{SD}	Thermal Shutdown	Rising [b]		140		°C
		Falling		120		°C

[a] Do not externally load. For internal biasing only.

[b] If the die temperature exceeds 130°C, the *Thermal_SHTDN_Status* flag is set and an End Power Transfer (EPT) packet is sent (see Table 12).

6. Typical Performance Characteristics

The performance characteristics curves were taken using the P9038-R transmitter in WPC Mode.

Figure 2. Efficiency vs Output Load: V_{OUT} = 5.5V

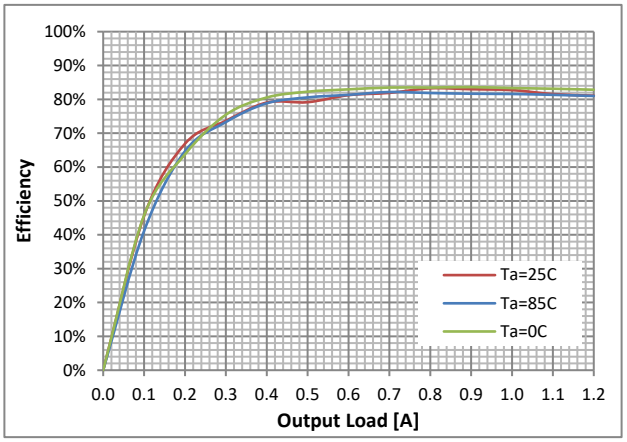


Figure 3. V_{OUT} vs Output Load: V_{OUT} = 5.5V

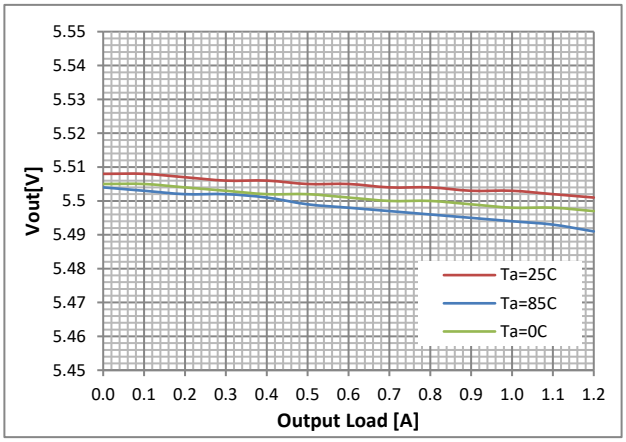


Figure 4. Efficiency vs Output Load: V_{OUT} = 5V

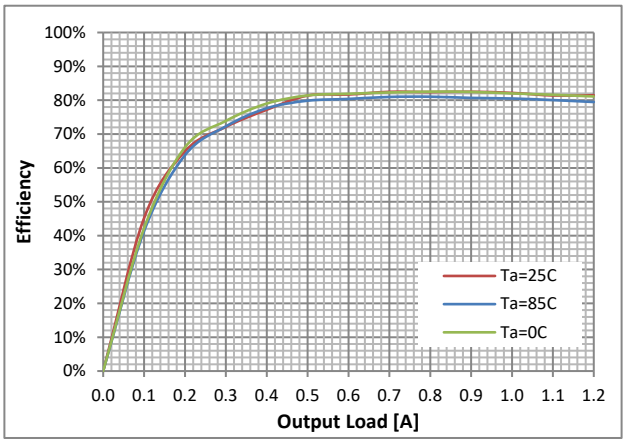


Figure 5. V_{OUT} vs Output Load: V_{OUT} = 5V

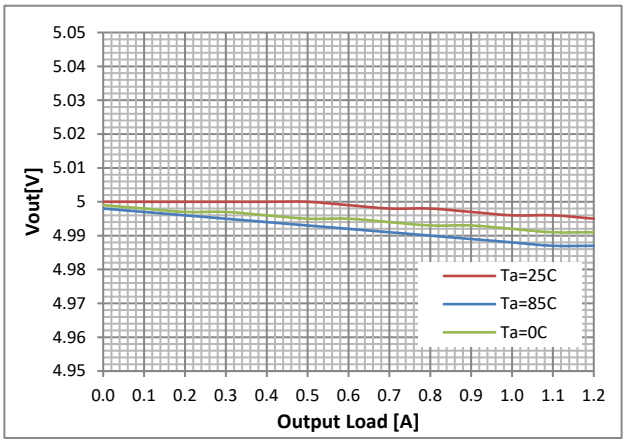


Figure 6. Efficiency vs Output Load: V_{OUT} = 4.5V

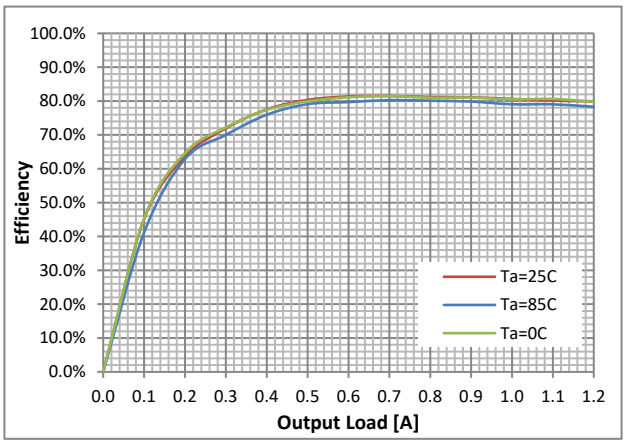


Figure 7. V_{OUT} vs Output Load: V_{OUT} = 4.5V

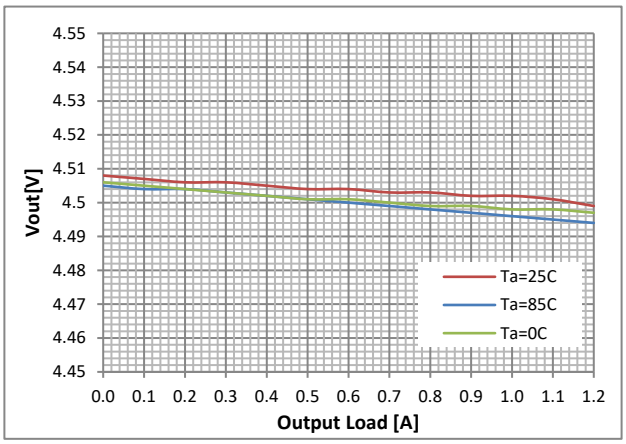


Figure 8. Rectified Voltage vs Output Load

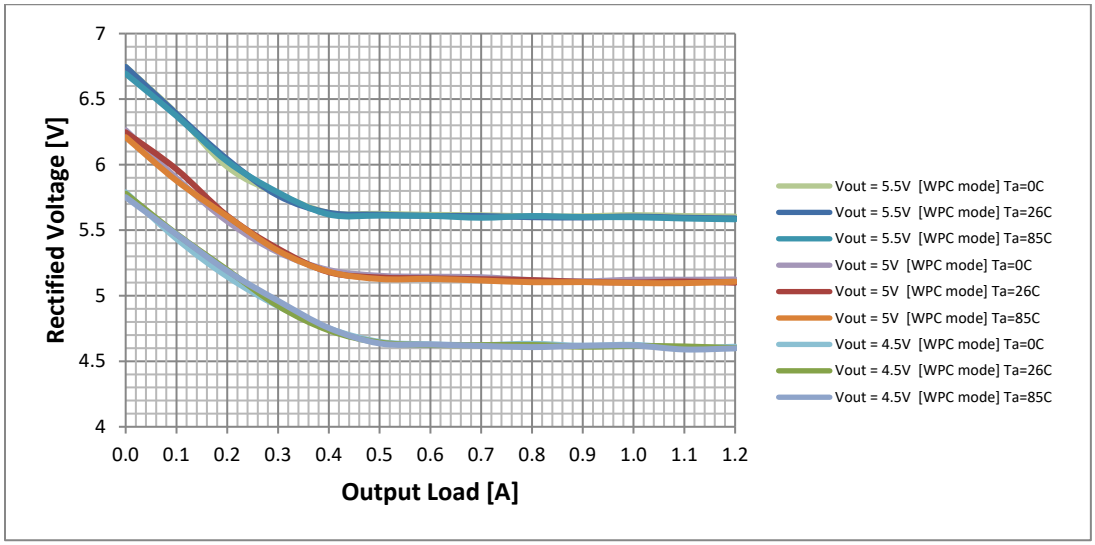


Figure 9. Load Transient: V_{OUT} = 5.5V, 0A ➔ 1.2A

Figure 10. Load Transient: V_{OUT} = 5.5V, 1.2A ➔ 0A

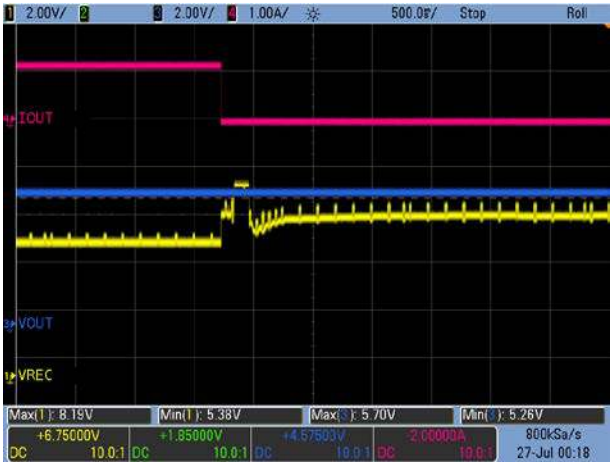


Figure 11. Load Transient: V_{OUT} = 5V, 0A ➔ 1.2A

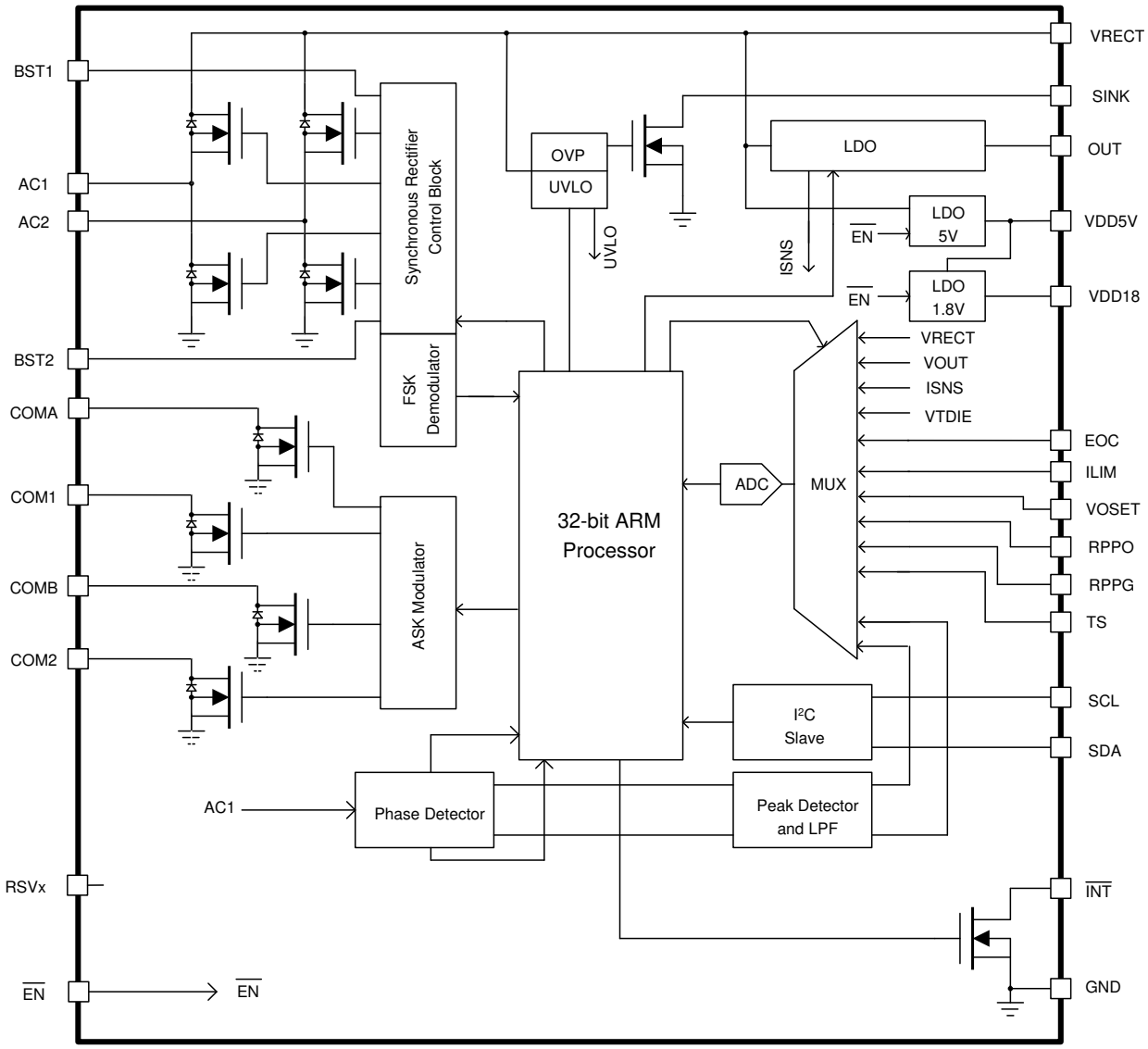
Figure 12. Load Transient: V_{OUT} = 5V, 1.2A ➔ 0A

Figure 13. Load Transient: V_{OUT} = 4.5V, 0A ➔ 1.2A

Figure 14. Load Transient: V_{OUT} = 4.5V, 1.2A ➔ 0A

7. Functional Block Diagram

Figure 15. Functional Block Diagram



8. Theory of Operation

The P9225-R is a highly-integrated, wireless power receiver targeted for 5W applications supporting both WPC and PMA standards. The device integrates a full-wave synchronous rectifier, low-dropout (LDO) linear regulator, and a 32-bit ARM®-based M0 processor to manage all of the digital control required to comply with the WPC-1.2.4 and PMA communication protocols. Using the near-field inductive power transfer, the receiver converts the AC signal to DC voltage using the integrated synchronous rectifier. The capacitor connected to the output of the rectifier smooths the full-wave rectified voltage into a DC voltage. After the internal biasing circuit is enabled, the “Synchronous Rectifier Control” block operates the switches of the rectifier in various modes to maintain reliable connections and optimal efficiency.

The rectifier voltage and the output current are sampled periodically and digitized by the analog-to-digital converter (ADC). The digital equivalents of the voltage and current are supplied to the internal control logic, which determines whether the loading conditions on the VRECT pin indicate that a change in the operating point is required. If the load is heavy enough and brings the voltage at VRECT below its target, the transmitter is instructed to increase the transmit power. If the voltage at VRECT is higher than its target, the transmitter is instructed to lower the transmit power. The P9225-R will modulate the load or coil voltage to send the instructions to the transmitter in WPC Mode. To maximize efficiency, the voltage at VRECT is programmed to decrease as the LDO’s load current increases. The internal temperature is continuously monitored to ensure proper operation.

In the event that the VRECT voltage increases above 12V, Control Error Packets will be sent to the transmitter in an attempt to bring the rectifier voltage back to a safe operating voltage level while simultaneously clamping the incoming energy using the open-drain SINK pin for VRECT linear clamping. The clamp is released when the VRECT voltage falls below V_{OVP-DC} minus $V_{OVP-HYS}$ (see Table 5).

The receiver utilizes IDT’s proprietary voltage clamping scheme, which limits the maximum voltage at the rectifier pin to 12V, reducing the voltage rating on the output capacitors while eliminating the need for over-voltage protection (OVP) capacitors. As a result, it provides a small application area, making it an industry-leading wireless power receiver for high power density applications. Combined with the P9038-R transmitter, the P9225-R is a complete wireless power system solution.

8.1 LDO – Low Dropout Regulators

The P9225-R has three low-dropout linear regulators. The main regulator provides the power required by the battery charger, and the output voltage can be set in the range of 4.5V to 5.5V. For more information about setting the output voltage, see section 8.2. It is important to connect a 22µF ceramic capacitance to the OUT pin.

The other two regulators, VDD5V and VDD18, bias the internal circuitry of the receiver. These LDOs must have local 1µF ceramic capacitors placed as close as possible to the pins.

8.2 Setting the Output Voltage – VOSET

The output voltage on the P9225-R is programmed by connecting the center tap of the external resistors R34 and R33 to the VOSET pin as shown in the application schematic in Figure 22.

The default output voltage is set to 5V in the P9225-R Evaluation Board provided in the P9225-R Evaluation Kit. Table 6 shows the resistor combination values for the target output voltage settings.

Table 6. Setting the Output Voltage

R34	R33	Output Voltage
10kΩ	OPEN	4.5V
10kΩ	49.9kΩ	4.6V
10kΩ	34kΩ	4.7V
10kΩ	20kΩ	4.8V
10kΩ	14.7kΩ	4.9V
OPEN	10kΩ	5.0V

R34	R33	Output Voltage
10kΩ	10kΩ	5.1V
14.7kΩ	10kΩ	5.2V
20kΩ	10kΩ	5.3V
34kΩ	10kΩ	5.4V
49.9kΩ	10kΩ	5.5V

8.3 SINK Pin

The P9225-R has an internal automatic DC clamping to protect the device in the event of high-voltage transients. The VRECT pin must be shorted to SINK.

8.4 Rectifier Voltage – VRECT

The P9225-R uses a high-efficiency synchronous rectifier to convert the AC signal from the coil to a DC signal on the VRECT pin. During startup, the rectifier operates as a passive diode bridge. Once the voltage on VRECT exceeds the under-voltage lock-out (UVLO) level (see Table 5), the rectifier will switch into full synchronous bridge rectifier mode. A total capacitance of 44µF is recommended to minimize the output voltage ripple.

8.5 Over-Current Limit – ILIM

The P9225-R has a programmable current-limit function for protecting the device in the event of an over-current or short-circuit fault condition. When the output current exceeds the programmed threshold, the P9225-R will limit the load current by reducing the output voltage. The current limit should be set to 120% of the target maximum output current.

Connect the ILIM pin to the center tap of a resistor divider to set the current limit. Table 7 shows the resistor combination values for the resistor divider for the ILIM setting. The default ILIM is set to 1.2A in the P9225-R Evaluation Board.

Table 7. Setting the Current Limit

R38	R22	ILIM
10kΩ	47kΩ	0.8A
10kΩ	22kΩ	0.9A
10kΩ	OPEN	1.0A
10kΩ	10kΩ	1.1A
OPEN	10kΩ	1.2A

8.6 Interrupt Function – $\overline{INT}$

The P9225-R provides an open-drain, active-LOW interrupt output pin. It is asserted LOW when $\overline{EN}$ is HIGH or any of the following fault conditions have been triggered: the die temperature exceeds 140°C, the external thermistor measurement exceeds the threshold (see section 8.9), or an over-current (OC) or over-voltage (OV) condition is detected (see sections 8.5 and 8 respectively).

During normal operation, the $\overline{INT}$ pin is pulled HIGH. This pin can be connected to the interrupt pin of a microcontroller. The fault condition triggering the interrupt flag is available in the I2C interrupt register (see Table 13).

8.7 Enable Pin – $\overline{EN}$

The P9225-R can be disabled by applying a logic HIGH to the $\overline{EN}$ pin. When the $\overline{EN}$ pin is pulled HIGH, the device is in Shut-Down Mode. Connecting the $\overline{EN}$ pin to logic LOW activates the device.

8.8 Thermal Protection

The P9225-R integrates thermal shutdown circuitry to prevent damage resulting from excessive thermal stress. The thermal protection will shut down the receiver if the die temperature exceeds 140°C. If the die temperature exceeds 130°C, the *Thermal_SHTDN_Status* flag is set and an End Power Transfer (EPT) packet is sent in order to lower the temperature.

8.9 External Temperature Sensing – TS

The P9225-R has a temperature sensor input, TS, which can be used to monitor an external temperature by using a thermistor. The TS pin voltage calculation is described by Equation 1.

$$V_{TS} = V_{VDD18} \times \frac{NTC}{R+NTC} \quad \text{Equation 1}$$

where NTC is the thermistor's resistance and R is the pull-up resistor connected to the VDD18 pin.

The over–temperature shutdown is triggered when the TS pin voltage is lower than 0.6V.

8.10 End of Charge – EOC

The End-of-Charge (EOC) pin is an active HIGH logic input, which can be used with an application processor or charger IC in battery management applications. When asserted, the receiver issues an End Power Transfer (EPT) packet to the transmitter terminating power transfer.

8.11 Received Power Packet Offset and Gain Calibration – RPPO and RPPG

The Received Power Packet Offset (RPPO) and Received Power Packet Gain (RPPG) calibrations utilize dedicated pins for tuning foreign object detection (FOD).

Received Power = Gain ✕ Power + Offset Equation 2

Power = Calculated Rx Power with Default Setting (in mW) Equation 3

$$Gain = \frac{ADC_{RPPG}}{1755}$$

where $ADC_{RPPG} = \text{INT}\left[\frac{V_{RPPG}}{2.1V} \times 4095\right]$ Equation 4

$$Offset = ADC_{RPPO} - 1755 \text{ (in mW)}$$

where $ADC_{RPPO} = \text{INT}\left[\frac{V_{RPPO}}{2.1V} \times 4095\right]$ Equation 5

To use the default FOD setting, set Gain to 1 and Offset to 0. That is equivalent to 0.9V at both RPPO and RPPG pins. To disable the FOD, the RPPO and RPPG pins must be pulled down to GND.

8.12 Advanced Foreign Object Detection (FOD)

When metallic objects are exposed to an alternating magnetic field, eddy currents cause such objects to heat up. Examples of such parasitic metal objects are coins, keys, paper clips, etc. The amount of heating depends on the strength of the coupled magnetic field, as well as on the characteristics of the object, such as its resistivity, size, and shape. In a wireless power transfer system, the heating manifests itself as a power loss, and therefore a reduction in power-transfer efficiency. Moreover, if no appropriate measures are taken, the heating could be sufficient that the foreign object could become heated to an undesirable temperature.

During the power transfer phase, the receiver periodically will communicate to the transmitter the amount of power received by means of a Received Power Packet. The transmitter will compare this power with the amount of power transmitted during the same time period. If there is a significant unexplained loss of power, then the transmitter will shut off power delivery because a possible foreign object might be absorbing too much energy.

For a WPC system to perform this function with sufficient accuracy, both the transmitter and receiver must account for and compensate for all of their known losses. Such losses could be due to resistive losses or nearby metals that are part of the transmitter or receiver, etc. Because the system accurately measures its power and accounts for all known losses, it can thereby detect foreign objects because they cause an unknown loss. The WPC specification requires that a power receiver must report to the power transmitter its received power (P_{PR}) in a Received-Power Packet (RPP). The maximum value of the received power accuracy P_{Δ} depends on the maximum power of the power receiver as defined in Table 8.

The power receiver must determine its P_{PR} with an accuracy of $\pm P_{\Delta}$, and report its received power as $P_{RECEIVED} = P_{PR} + P_{\Delta}$. This means that the reported received power is always greater than or equal to the transmitted power (P_{PT}) if there is no foreign object (FO) present on the interface surface.

Table 8. Maximum Estimated Power Loss

Maximum Power [W]	Maximum P_{Δ} [mW]
5	350

The compensation algorithm includes values that are programmable via either the I2C interface or OTP (one-time programmable) bits. Programmability is necessary so that the calibration settings can be optimized to match the power transfer characteristics of each particular WPC system to include the power losses of the transmit and receive coils, battery, shielding, and case materials under no-load to full-load conditions. The values are based on the comparison of the received power against a reference power curve so that any foreign object can be sensed when the received power is different from the expected system power.

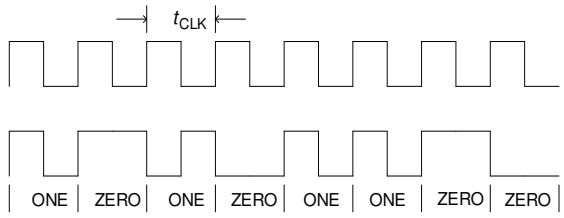
9. Communication Interface

9.1 Modulation/Communication

Receiver-to-transmitter communication is accomplished by modulating the load seen by the receiver's inductor; the communication is purely digital and logic 1's and 0's ride on top of the power signal that exists between the two coils. Modulation is done with amplitude-shift keying (ASK) modulation using internal switches to connect external capacitors from AC1 and AC2 to ground (see Figure 15) with a bit rate of 2Kbps. To the transmitter, this appears as an impedance change, which results in measurable variations of the transmitter's output waveform. The power transmitter detects this as a modulation of coil current/voltage to receive the packets.

As required by the WPC, the P9225-R uses a differential bi-phase encoding scheme to modulate data bits onto the power signal. A clock frequency of 2kHz is used for this purpose. A logic ONE bit is encoded using two narrow transitions, whereas a logic ZERO bit is encoded using one wider transition as shown below:

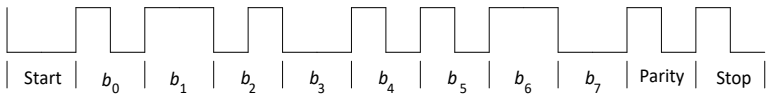
Figure 16. Bit Encoding Scheme



9.2 Byte Encoding for ASK

Each byte in the communication packet comprises 11 bits in an asynchronous serial format, as shown in Figure 17.

Figure 17. Byte Encoding Scheme



Each byte has a start bit, 8 data bits, a parity bit, and a single stop bit.

9.3 Packet Structure

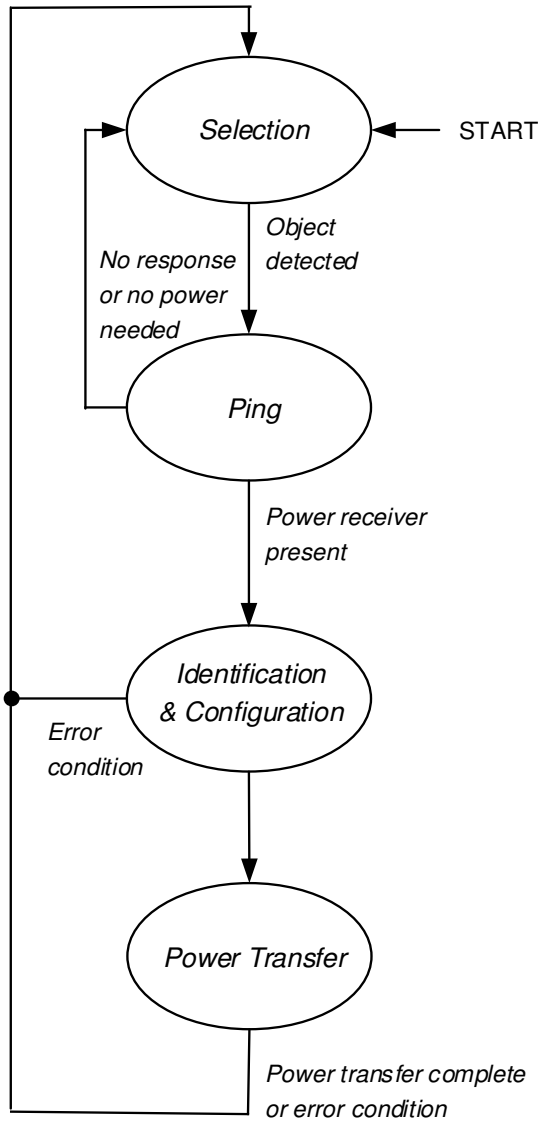
The P9225-R communicates with the base station via communication packets. Each communication packet has the following structure:

Figure 18. Communication Packet Structure

Preamble	Header	Message	Checksum

10. WPC Mode Characteristics

Figure 19. State Diagram for WPC Baseline Power Profile (BPP) Operation



10.1 Selection Phase or Startup

In the selection phase, the power transmitter determines if it will proceed to the ping phase after detecting the placement of an object. In this phase, the power transmitter typically monitors the interface surface for the placement and removal of objects using a small measurement signal. This measurement signal should not wake up a power receiver that is positioned on the interface surface.

10.2 Ping Phase (Digital Ping)

In the ping phase, the power transmitter will transmit power and will detect the response from a possible power receiver. This response ensures the power transmitter that it is dealing with a power receiver rather than some unknown object. When a mobile device containing the P9225-R is placed on a WPC “Qi” charging pad, it responds to the application of a power signal by rectifying this power signal. When the voltage on VRECT is greater than the UVLO threshold, then the internal bandgaps, reference voltage, and internal voltage regulators (5V and 1.8V) are turned on, and the microcontroller’s startup is initiated enabling the WPC communication protocol.

If the power transmitter correctly receives a signal strength packet, the power transmitter proceeds to the identification and configuration phase of the power transfer, maintaining the power signal output.

10.3 Identification and Configuration Phase

The identification and configuration phase is the part of the protocol that the power transmitter executes in order to identify the power receiver and establish a default power transfer contract. This protocol extends the digital ping in order to enable the power receiver to communicate the relevant information.

In this phase, the power receiver identifies itself by sending its identification packet and provides information for a default power transfer contract by sending the configuration packet.

10.4 Power Transfer Phase

In this phase, the P9225-R controls the power transfer by means of the following control data packets:

- Control Error Packets
- Received Power Packet (RPP, FOD-related)
- End Power Transfer (EPT) Packet

Once the identification and configuration phase is completed, the transmitter initiates the power transfer mode. The P9225-R control circuit measures the rectifier voltage and sends error packets to the transmitter to adjust the rectifier voltage to the level required to maximize the efficiency of the linear regulator and to send to the transmitter the Received Power Packet for foreign object detection (FOD) to guarantee safe, efficient power transfer.

In the event of an EPT issued by the application, the P9225-R continuously sends EPT packets until the transmitter removes the power and the rectified voltage on the receiver side drops below the UVLO threshold.

11. Functional Registers

The following tables provide the address locations, field names, available operations (R or RW), default values, and functional descriptions of all the internally accessible registers contained within the P9225-R. The default I2C slave address is 61_{HEX}.

Table 9. Device Identification Register

Address and Bit	Register Field Name	R/W	Default	Function and Description
0000_{HEX} [7:0]	Part_number_L	R	25_{HEX}	Chip ID low byte
0001_{HEX} [7:0]	Part_number_H	R	92_{HEX}	Chip ID high byte

Table 10. Firmware Major Revision

Address and Bit	Register Field Name	R/W	Default	Function and Description
0004_{HEX} [7:0]	FW_Major_Rev_L	R	01_{HEX}	Major firmware revision low byte
0005_{HEX} [7:0]	FW_Major_Rev_H	R	00_{HEX}	Major firmware revision high byte

Table 11. Firmware Minor Revision

Address and Bit	Register Field Name	R/W	Default	Function and Description
0006_{HEX} [7:0]	FW_Minor_Rev_L	R	27_{HEX}	Minor firmware revision low byte
0007_{HEX} [7:0]	FW_Minor_Rev_H	R	04_{HEX}	Minor firmware revision high byte

Table 12. Status Registers

Address and Bit	Register Field Name	R/W	Default	Function and Description
0034_{HEX} [7]	Vout_Status	R	0_{BIN}	“0” output voltage is off. “1” output voltage is on.
0034_{HEX} [6]	Reserved	R	0_{BIN}	
0034_{HEX} [5]	Reserved	R	0_{BIN}	
0034_{HEX} [4]	Reserved	R	0_{BIN}	
0034_{HEX} [3]	Reserved	R	0_{BIN}	
0034_{HEX} [2]	Thermal_SHTDN_Status	R	0_{BIN}	“0” indicates no over-temperature condition exists. “1” indicates that the die temperature exceeds 130°C or the NTC is less than 0.6V. The P9225-R sends an End Power Transfer (EPT) packet to the transmitter.
0034_{HEX} [1]	VRECT_OV_ Status	R	0_{BIN}	“1” indicates rectifier exceeds 20V for V_{OUT}=12. The P9225-R sends an End Power Transfer (EPT) packet to the transmitter.
0034_{HEX} [0]	Current_Limit_Status	R	0_{BIN}	“1” indicates current limit has been exceeded. The P9225-R sends an End Power Transfer (EPT) packet to the transmitter.
0035_{HEX} [7:0]	Reserved	R	00_{HEX}	

Table 13. Interrupt Status Registers

Address and Bit	Register Field Name	R/W	Default	Function and Description
0036_{HEX} [7]	INT_Vout_Status	R	0_{BIN}	"0" output voltage has not changed. "1" output voltage changed.
0036_{HEX} [6]	Reserved	R	0_{BIN}	
0036_{HEX} [5]	Reserved	R	0_{BIN}	
0036_{HEX} [4]	Reserved	R	0_{BIN}	
0036_{HEX} [3]	Reserved	R	0_{BIN}	
0036_{HEX} [2]	INT_OVER_TEMP_Status	R	0_{BIN}	"1" indicates over-temperature condition exists.
0036_{HEX} [1]	INT_VRECT_OV_Status	R	0_{BIN}	"1" indicates rectifier over-voltage condition exists.
0036_{HEX} [0]	INT_OC_Limit_Status	R	0_{BIN}	"1" indicates current limit has been exceeded.
0037_{HEX} [7:0]	Reserved	R	00_{HEX}	

Note: If any bit in the *Interrupt Status* register 36_{HEX} is "1" and the corresponding bit in the *Interrupt Enable* register 38_{HEX} is set to "1," the $\overline{INT}$ pin will be pulled down indicating an interrupt event has occurred.

Table 14. Interrupt Enable Registers

Address and Bit	Register Field Name	R/W	Default	Function and Description
0038_{HEX} [7]	Vout_Status_INT_EN	RW	0_{BIN}	"0" disables the *INT_Vout_Status* interrupt. "1" enables the interrupt.
0038_{HEX} [6]	Reserved	R	0_{BIN}	
0038_{HEX} [5]	Reserved	R	0_{BIN}	
0038_{HEX} [4]	Reserved	R	0_{BIN}	
0038_{HEX} [3]	Reserved	R	0_{BIN}	
0038_{HEX} [2]	OVER_TEMP_INT_EN	RW	0_{BIN}	"0" disables the *INT_OVER_TEMP* interrupt. "1" enables the interrupt.
0038_{HEX} [1]	VRECT_OV_INT_EN	RW	0_{BIN}	"0" disables the *INT_VRECT_OV* interrupt. "1" enables the interrupt.
0038_{HEX} [0]	OC_Limit_Status_INT_EN	RW	0_{BIN}	"0" disables the *INT_OC_Limit_Status* interrupt. "1" enables the interrupt.
0039_{HEX} [7:0]	Reserved	RW	00_{HEX}	

Table 15. Battery Charge Status

Address and Bit	Register Field Name	R/W	Default	Function and Description
$003A_{HEX}$ [7:0]	Batt_Charg_status	R/W	00_{HEX}	The application processor loads the battery charge status in this register. This value is sent to the transmitter when bit 4 of register $004E_{HEX}$ is set to "1."[a]

[a] Firmware only forwards the data from the application processor to transmitter.

Table 16. End Power Transfer

The application processor initiates the End Power Transfer (EPT).

Address and Bit	Register Field Name	R/W	Default	Function and Description
$003B_{HEX}$ [7:0]	EPT_Code	R/W	00_{HEX}	The application processor loads the EPT code value in this register. This value is sent to the transmitter when bit 3 of register $004E_{HEX}$ is set to "1."

Table 17. Read Register – Output Voltage

$$V_{OUT} = \frac{ADC\_VOUT * 6 * 2.1}{4095}$$

Address and Bit	Register Field Name	R/W	Default	Function and Description
$003C_{HEX}$ [7:0]	ADC_VOUT [7:0]	R	0_{HEX}	8 LSB of VOUT ADC value.
$003D_{HEX}$ [7:4]	Reserved	R	0_{HEX}	Reserved.
$003D_{HEX}$ [3:0]	ADC_VOUT [11:8]	R	0_{HEX}	4 MSB of VOUT ADC value.

Table 18. Read Register – VRECT Voltage

$$VRECT = \frac{ADC\_VRECT * 10 * 2.1}{4095}$$

Address and Bit	Register Field Name	R/W	Default	Function and Description
0040_{HEX} [7:0]	ADC_VRECT [7:0]	R	–	8 LSB of VRECT ADC value.
0041_{HEX} [7:4]	Reserved	R	0_{HEX}	Reserved
0041_{HEX} [3:0]	ADC_VRECT [11:8]	R	–	4 MSB of VRECT ADC value.

Table 19. Read Register – I_{OUT} Current

$$I_{OUT} = \frac{RX\_IOUT * 2 * 2.1}{4095}$$

Address and Bit	Register Field Name	R/W	Default	Function and Description
0044_{HEX} [7:0]	RX_IOUT [7:0]	R_{HEX}	–	8 LSB of IOUT. Output current in mA.
0045_{HEX} [7:0]	RX_IOUT [15:8]	R_{HEX}	–	8 MSB of IOUT. Output current in mA

Table 20. Read Register – Die Temperature

$T_{DIE} = (ADC\_Die\_Temp - 1350)\frac{83}{444} - 273$ where *ADC_Die_Temp* = 12 bits from *ADC_Die_Temp_H* and *ADC_Die_Temp_L*.

Address and Bit	Register Field Name	R/W	Default	Function and Description
0046_{HEX} [7:0]	ADC_Die_Temp_L	R	–	8 LSB of current die temperature in °C.
0047_{HEX} [7:4]	Reserved	R	0_{HEX}	Reserved
0047_{HEX} [3:0]	ADC_Die_Temp_H	R	–	4 MSB of current die temperature in °C.

Table 21. Read Register – Operating Frequency

$$f_{OP} = \frac{64 * 6000}{OP\_FREQ\,[15:0]}$$

Address and Bit	Register Field Name	R/W	Default	Function and Description
0048_{HEX} [7:0]	OP_FREQ[7:0]	R	–	8 LSB AC signal frequency on the coil.
0049_{HEX} [7:0]	OP_FREQ[15:8]	R	–	8 MSB AC signal frequency on the coil.

Table 22. Command Register

Address and Bit	Register Field Name	R/W	Default	Function and Description
$004E_{HEX}$ [7:6]	Reserved	R	0_{HEX}	Reserved.
$004E_{HEX}$ [5]	Clear_Interrupt	RW	0_{BIN}	If application processor sets this bit to "1," the P9225-R clears the interrupt pin.
$004E_{HEX}$ [4]	Send Batt Charge status	R	0_{BIN}	If the application processor sets this bit to "1," the P9225-R sends the battery charge status (see *Batt_Charg_status* in Table 15).
$004E_{HEX}$ [3]	Send_End_Power_Transfer	RW	0_{BIN}	If application processor sets this bit to "1," the P9225-R sends the End Power Transfer packet (defined in the *EPT_Code* register shown in Table 16) to the transmitter and then sets this bit to "0."
$004E_{HEX}$ [2]	Reserved	R	0_{BIN}	Reserved.
$004E_{HEX}$ [1]	Toggle_LDO_On-OFF	RW	0_{BIN}	If application processor sets this bit to "1," the P9225-R toggles the LDO output once (from ON to OFF or from OFF to ON), and then sets this bit to "0."
$004E_{HEX}$ [0]	Reserved	R	0_{BIN}	Reserved.

Table 23. Clear Interrupt Bits

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
0056_{HEX} [7]	Clear_Vout_Changed_Bit	RW	0_{BIN}	"1" clears the *INT_Vout_Status* bit in register 0036_{HEX} (refer to Table 13). Register 0036_{HEX} is updated after the application processor resets the interrupt pin by writing "1" to bit 5 of register $004E_{HEX}$ (refer to Table 22).
0056_{HEX} [6]	Reserved	RW	0_{BIN}	
0056_{HEX} [5]	Reserved	RW	0_{BIN}	
0056_{HEX} [4]	Reserved	RW	0_{BIN}	
0056_{HEX} [3]	Reserved	RW	0_{BIN}	
0056_{HEX} [2]	Clear_Over_Temperature_Bit	RW	0_{BIN}	"1" clears the *INT_OVER_TEMP_Status* bit in register $0036_{HEX.}$ Register 0036_{HEX} is updated after the application processor resets the interrupt pin by writing"1" to bit 5 of register $004E_{HEX}$.
0056_{HEX} [1]	Clear_Over_Voltage_Bit	RW	0_{BIN}	"1" clears the *INT_VRECT_OV_Status* bit in register $0036_{HEX.}$ Register 0036_{HEX} is updated after the application processor resets the interrupt pin by writing "1" to bit 5 of register $004E_{HEX}$.
0056_{HEX} [0]	Clear_Over_Current_Bit	RW	0_{BIN}	"1" clears the *INT_OC_Limit_Status* bit in register $0036_{HEX.}$ Register 0036_{HEX} is updated after the application processor resets the interrupt pin by writing "1" to bit 5 of register $004E_{HEX}$.

Table 24. WPC Power Transfer Phase Indicator Register

Address and Bits	Register Field Name	R/W	Default	Function and Description
$014A_{HEX}$	System_State	R	00_{HEX}	0_{DEC} = Selection Phase 1_{DEC} = Identification Phase 2_{DEC} = Configuration Phase 3_{DEC} = Reserved 4_{DEC} = Reserved 5_{DEC} = Power Transfer Phase 6_{DEC} = Reserved 7_{DEC} = Reserved 8_{DEC} = Error State

12. I2C Access Description

Figure 20. I2C Access Read Protocol

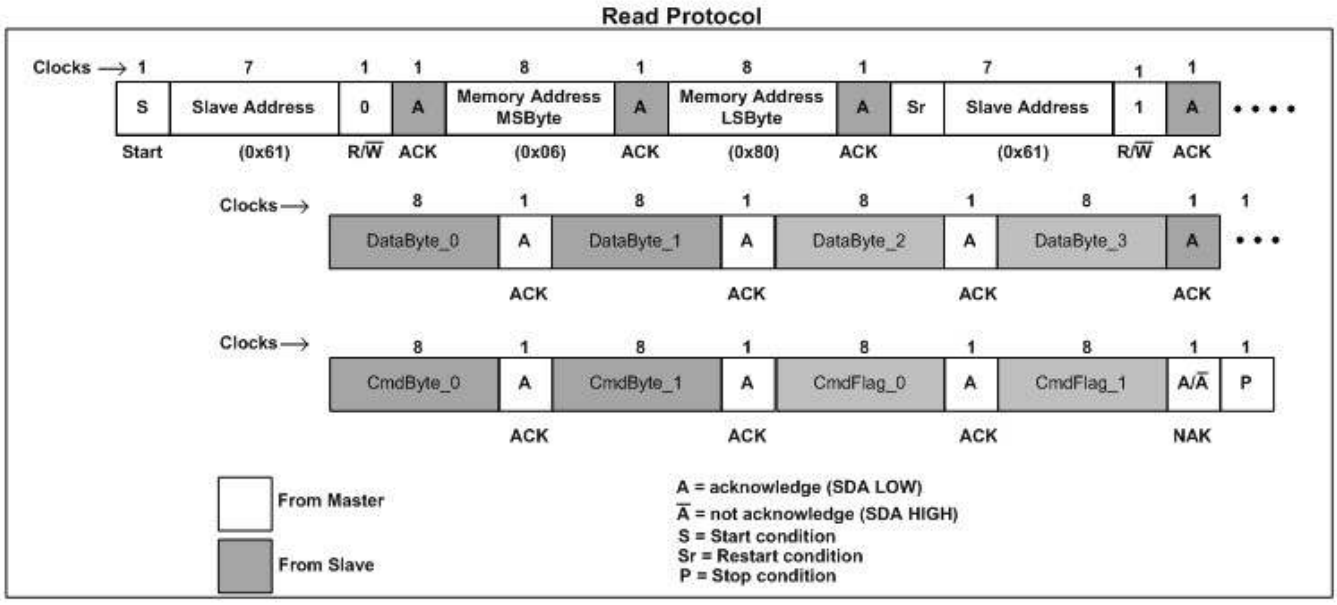
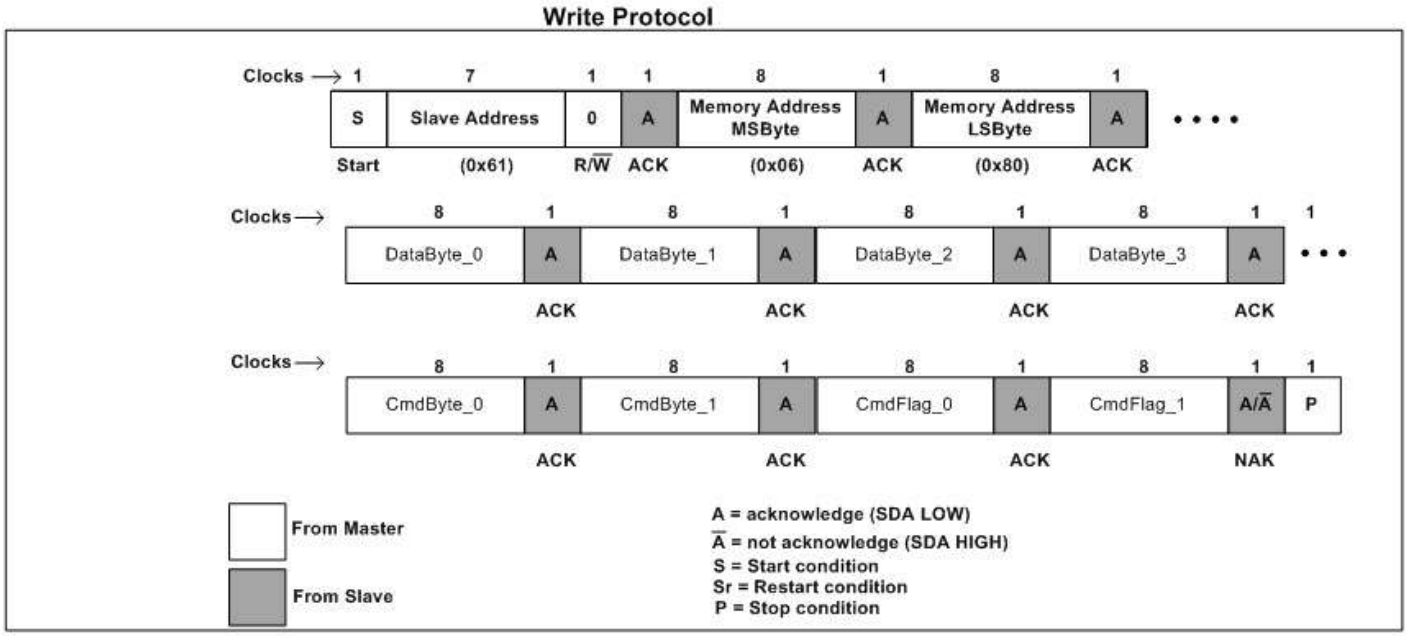


Figure 21. I2C Access Write Protocol



13. Application Information

13.1 Power Dissipation and Thermal Requirements

The use of integrated circuits in low-profile and fine-pitch surface-mount packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks, convection surfaces, and the presence of other heat-generating components must be taken into consideration.

The P9225-R package has a maximum power dissipation of approximately 1.72W, which is governed by the number of thermal vias between the package and the printed circuit board. The die's maximum power dissipation is specified by the junction temperature and the package thermal resistance. The WLCSP package has a typical θ_{JA} of 47°C/W with 8 thermal vias and 77°C/W with no thermal vias. Maximizing the thermal vias is highly recommended.

The ambient temperature surrounding the R9225-R0 will also have an effect on the thermal limits of the printed circuit board (PCB) design. The main factors influencing thermal resistance (θ_{JA}) are the PCB characteristics and thermal vias. For example, in a typical still-air environment, a significant amount of the heat generated is absorbed by the PCB. Changing the design or configuration of the PCB changes the overall thermal resistivity and therefore the board's heat-sinking efficiency.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow into the system

First, the maximum power dissipation for a given situation should be calculated using Equation 6:

$$P_{D(MAX)} = \frac{\left(T_{J(MAX)} - T_{AMB}\right)}{\theta_{JA}} \qquad \text{Equation 6}$$

Where

$P_{D(MAX)}$ = Maximum power dissipation

θ_{JA} = Package thermal resistance (°C/W)

$T_{J(MAX)}$ = Maximum device junction temperature (°C)

T_{AMB} = Ambient temperature (°C)

The maximum recommended junction temperature ($T_{J(MAX)}$) for the P9225-R device is 125°C. The thermal resistance of the 52-WLCSP package (AHG52) is nominally θ_{JA}=47°C/W with 8 thermal vias. Operation is specified to a maximum steady-state ambient temperature (T_{AMB}) of 85°C. Therefore, the maximum recommended power dissipation is

$$P_{D(MAX)} = \frac{(124°C - 85°C)}{47°C/W} \cong 0.85 \text{ Watt} \qquad \text{Equation 7}$$

All the above-mentioned thermal resistances are the values found when the P9225-R is mounted on a standard board of the dimensions and characteristics specified by the JEDEC 51 standard.

13.2 Recommended Coils

The following coil is recommended with the P9225-R receiver for 5W applications for optimum performance.

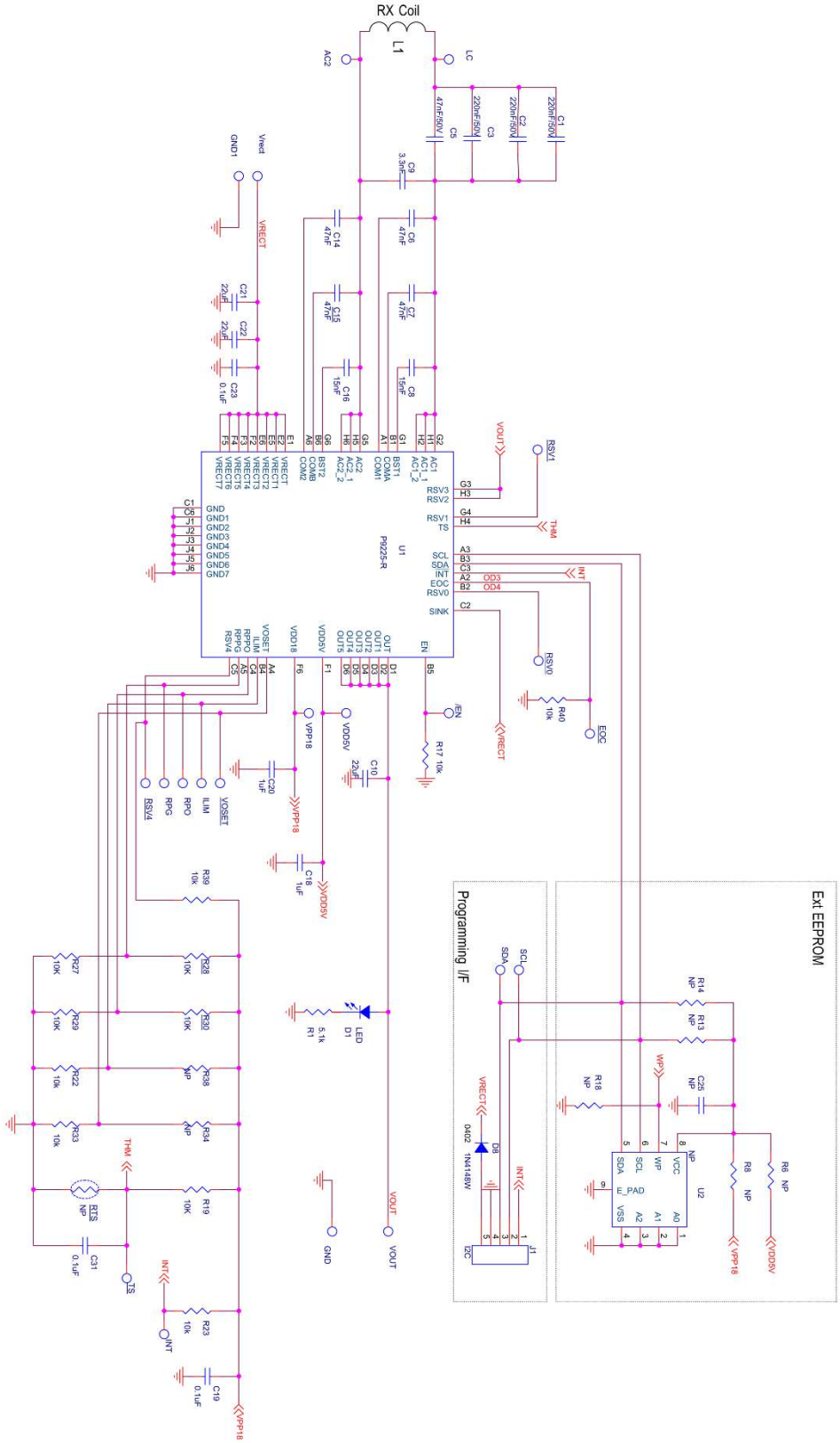
Table 25. Recommended Coil Manufacturers

WPC and PMA Dual Mode Receiver Coil:

Vendor	Part Number	Inductance at 100kHz	DCR at 20°C
Sunlord	SWA50R40H09C01BMDIDD	8.3µH±10%	150mΩ ±20%
Würth Elektronik	760308102207	8µH±10%	70mΩ ±20%

13.3 Typical Application Schematic

Figure 22. P9225-R Typical Application Schematic



13.4 Bill of Materials (BOM)

Table 26. P9225-R MM Evaluation Kit V1.0 Bill of Materials

Item	Reference	Quantity	Value	Description	Part Number	PCB Footprint
1	C1, C2, C3	3	220nF/50V	CAP CER 0.22µF 50V X7R 0603	GRM188R71H224KAC4D	0603
2	C5, C6, C7, C14, C15	5	47nF	CAP CER 0.047µF 50V X7R 0402	GRM155R71H473KE14D	0402
3	C8, C16	2	15nF	CAP CER 0.015µF 50V X7R 0402	GRM155R71H153KA12J	0402
4	C9	1	3.3nF	CAP CER 3300PF 50V X7R 0402	GRM155R71H332KA01D	0402
5	C10	1	22µF	CAP CER 22µF 16V X5R 0805	CL21A226MOCLRNC	0805
6	C18, C20	2	1µF	CAP CER 1µF 10V X5R 0402	GRM155R61A105KE15D	0402
7	C19, C31	2	0.1µF	CAP CER 0.1µF 10V X5R 0201	GRM033R61A104ME15D	0201
8	C21, C22	2	22µF	CAP CER 22µF 25V X5R 0805	CL21A226MAQNNNE	0805
9	C23	1	0.1µF	CAP CER 0.1µF 25V X5R 0201	GRM033R61E104KE14D	0201
10	C25	1	NP			
11	D1	1	LED	LED GREEN CLEAR 0603 SMD	150 060 GS7 500 0	0603_diode
12	D8	1	1N4148W	DFN 150mA 75V Sm Sgnl Switching	CDSQR4148	0402
13	J1	1	I2C	HEADER_1X5_0P1PITCH60P42D	68002-205HLF	header_1x5_0p 1Pitch60p42d
14	RTS	1	NP			
15	R1	1	5.1k	RES SMD 5.1K OHM 5% 1/16W 0402	MCR01MRTJ512	0402
16	R6, R8, R13, R14	4	NP			
17	R17, R23, R39, R40	4	10k	RES SMD 10kΩ 5% 1/20W 0201	ERJ-1GEJ103C	0201
18	R19, R22, R27, R28, R29, R30, R33	7	10k	RES SMD 10kΩ 1% 1/20W 0201	ERJ-1GEF1002C	0201
19	R18, R34, R38	3	NP			
20	U1	1	P9225-R	MP Wireless Power Receiver	P9225-R	csp52_2p64x3p 94_0p4mm
21	U2	1	NP			

* NP = not populated

14. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available and is subject to change.

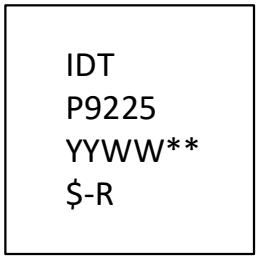
www.idt.com/document/psc/ahg52-package-outline-2640-x-3940mm-body-04mm-pitch-dsbga

15. Special Notes: WLCSP-52 (AHG52) Package Assembly

Unopened dry packaged parts have a one-year shelf life.

The HIC indicator card for newly-opened dry packaged parts should be checked. If there is any moisture content, the parts must be baked for a minimum of 8 hours at 125˚C within 24 hours of the assembly reflow process.

16. Marking Diagram



1. Line 1 company name.
2. Truncated part number.
3. “YYWW” is the last digit of the year and week that the part was assembled.

   ** is the lot sequential code.
4. “$” denotes mark code, -R is part of the device part number

17. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Ambient Temperature
P9225-RAHGI8	P9225-R Wireless Power Receiver for 5W Applications, 2.64 × 3.94 mm 52-WLCSP	MSL1	Reel	0°C to +85°C
P9225-R-EVK	P9225-R Evaluation Kit			

18. Revision History

Revision Date	Description of Change
November 12, 2018	▪ Added “Wurth Elektronik” to Table 25
July 18, 2018	▪ Deletion of "(WPC and PMA)" in the document title. ▪ Corrections for Table 3 regarding the ESD ratings for the RSVx pins.
May 22, 2018	▪ Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

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