2N3773

NPN Power Transistors

The 2N3773 is a PowerBase[™] power transistor designed for high power audio, disk head positioners and other linear applications. This device can also be used in power switching circuits such as relay or solenoid drivers, DC-DC converters or inverters.

Features

- High Safe Operating Area (100% Tested) 150 W @ 100 V
- Completely Characterized for Linear Operation
- High DC Current Gain and Low Saturation Voltage $h_{FE} = 15$ (Min) @ 8.0 A, 4.0 V $V_{CE(sat)} = 1.4 \text{ V (Max)} @ I_C = 8.0 \text{ A}, I_B = 0.8 \text{ A}$
- For Low Distortion Complementary Designs
- This is a Pb-Free Device

MAXIMUM RATINGS (Note 1)

, ,			
Rating	Symbol	Value	Unit
Collector - Emitter Voltage	V_{CEO}	140	Vdc
Collector - Emitter Voltage	V_{CEX}	160	Vdc
Collector - Base Voltage	V_{CBO}	160	Vdc
Emitter – Base Voltage	V_{EBO}	7	Vdc
Collector Current - Continuous - Peak (Note 2)	I _C	16 30	Adc
Base Current - Continuous - Peak (Note 2)	Ι _Β	4 15	Adc
Total Power Dissipation @ T _A = 25°C Derate above 25°C	P _D	150 0.855	W W/°C
Operating and Storage Junction Temperature Range	T _J , T _{stg}	-65 to +200	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Indicates JEDEC Registered Data.
- 2. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

THERMAL CHARACTERISTICS

April, 2013 - Rev. 11

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{ heta JC}$	1.17	°C/W

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



ON Semiconductor®

http://onsemi.com

16 A NPN POWER TRANSISTORS 140 V, 150 W

CASE 1-07



2N3773/D

MARKING

= Assembly Location

= Year

WW = Work Week

= Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

2N3773

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
DFF CHARACTERISTICS (Note 3)	•	•		
Collector–Emitter Breakdown Voltage (Note 4) (I _C = 0.2 Adc, I _B = 0)	V _{CEO(sus)}	140	-	Vdc
Collector–Emitter Sustaining Voltage (Note 4) (I _C = 0.1 Adc, V _{BE(off)} = 1.5 Vdc, R _{BE} = 100 Ohms)	V _{CEX(sus)}	160	-	Vdc
Collector-Emitter Sustaining Voltage (I _C = 0.2 Adc, R _{BE} = 100 Ohms)	V _{CER(sus)}	150	-	Vdc
Collector Cutoff Current (Note 4) (V _{CE} = 120 Vdc, I _B = 0)	I _{CEO}	-	10	mAdd
Collector Cutoff Current (Note 4) $ (V_{CE} = 140 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}) $ $ (V_{CE} = 140 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 150^{\circ}\text{C}) $	I _{CEX}	- -	2 10	mAdo
Collector Cutoff Current (V _{CB} = 140 Vdc, I _E = 0)	I _{CBO}	-	2	mAdd
Emitter Cutoff Current (Note 4) (V _{BE} = 7 Vdc, I _C = 0)	I _{EBO}	-	5	mAdo
ON CHARACTERISTICS (Note 3)	•			_
DC Current Gain ($I_C = 8$ Adc, $V_{CE} = 4$ Vdc) (Note 4) ($I_C = 16$ Adc, $V_{CE} = 4$ Vdc)	h _{FE}	15 5	60 -	_
Collector–Emitter Saturation Voltage ($I_C = 8$ Adc, $I_B = 800$ mAdc) (Note 4) ($I_C = 16$ Adc, $I_B = 3.2$ Adc)	V _{CE(sat)}	- -	1.4 4	Vdc
Base-Emitter On Voltage (Note 4) (I _C = 8 Adc, V _{CE} = 4 Vdc)	V _{BE(on)}	-	2.2	Vdc
DYNAMIC CHARACTERISTICS	<u>.</u>			
Magnitude of Common-Emitter Small-Signal, Short-Circuit, Forward Current Transfer Ratio (I _C = 1 A, f = 50 kHz)	h _{fe}	4	-	-
Small-Signal Current Gain (Note 4) $(I_C = 1 \text{ Adc}, V_{CE} = 4 \text{ Vdc}, f = 1 \text{ kHz})$	h _{fe}	40	-	-
SECOND BREAKDOWN CHARACTERISTICS	•			
Second Breakdown Collector Current with Base Forward Biased t = 1 s (non-repetitive), V _{CE} = 100 V, See Figure 12	I _{S/b}	1.5	-	Adc

^{3.} Pulse Test: Pulse Width = 300 μ s, Duty Cycle \leq 2%.

ORDERING INFORMATION

Device	Package	Shipping [†]
2N3773G	TO-204 (Pb-Free)	100 Unit / Tray

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{4.} Indicates JEDEC Registered Data.

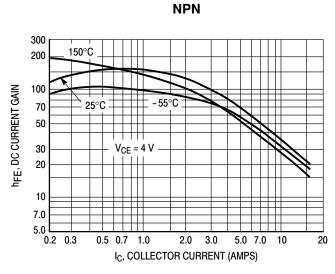


Figure 1. DC Current Gain

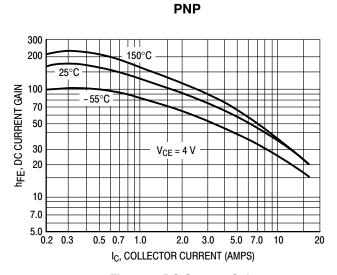


Figure 2. DC Current Gain

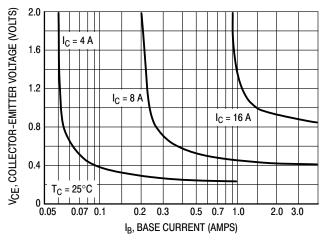


Figure 3. Collector Saturation Region

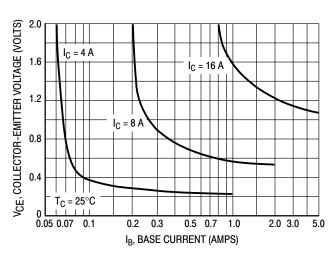


Figure 4. Collector Saturation Region

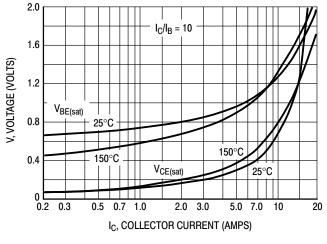


Figure 5. "On" Voltage

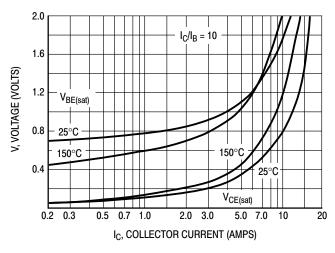


Figure 6. "On" Voltage

TYPICAL CHARACTERISTICS

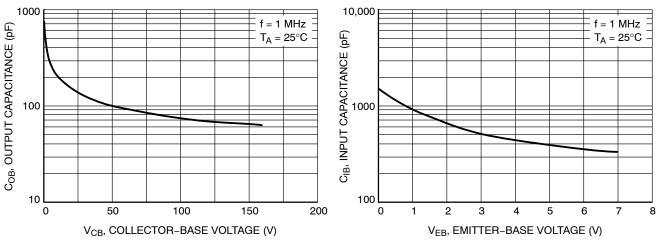


Figure 7. Output Capacitance

Figure 8. Input Capacitance

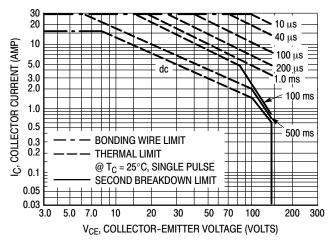


Figure 9. Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)} = 200^{\circ}C$; T_{C} is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^{\circ}C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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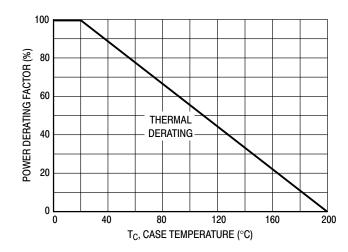


Figure 10. Power Derating

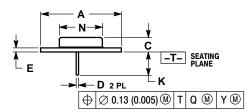


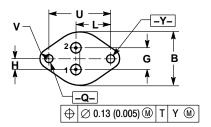
TO-204 (TO-3) **CASE 1-07 ISSUE Z**

DATE 05/18/1988



STYLE 1:





STYLE 2:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

STYLE 5:

 CONTROLLING DIMENSION: INCH.
 ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	1.550 REF		39.37 REF		
В		1.050		26.67	
С	0.250	0.335	6.35	8.51	
D	0.038	0.043	0.97	1.09	
Е	0.055	0.070	1.40	1.77	
G	0.430 BSC		10.92 BSC		
Н	0.215 BSC		5.46	BSC	
K	0.440	0.480	11.18	12.19	
L	0.665	BSC	16.89	BSC	
N		0.830		21.08	
Q	0.151	0.165	3.84	4.19	
U	1.187 BSC		30.15 BSC		
٧	0.131	0.188	3.33	4.77	

OTTLL I.	STILL Z.	STILL S.	STILL 4.	JIILL J.
PIN 1. BASE	PIN 1. BASE	PIN 1. GATE	PIN 1. GROUND	PIN 1. CATHODE
2. EMITTER	2. COLLECTOR	2. SOURCE	INPUT	EXTERNAL TRIP/DELAY
CASE: COLLECTOR	CASE: EMITTER	CASE: DRAIN	CASE: OUTPUT	CASE: ANODE
STYLE 6:	STYLE 7:	STYLE 8:	STYLE 9:	
PIN 1. GATE	PIN 1. ANODE	PIN 1. CATHODE #1	PIN 1. ANODE #1	
2. EMITTER	2. OPEN	CATHODE #2	ANODE #2	
CASE: COLLECTOR	CASE: CATHODE	CASE: ANODE	CASE: CATHODE	

STYLE 3:

STYLE 4:

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