

# **BUK9Y12-100E**

# N-channel 100 V, 12 m $\Omega$ logic level MOSFET in LFPAK56 Product data sheet

#### 1. **General description**

Logic level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

#### 2. **Features and benefits**

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with V<sub>GS(th)</sub> rating of greater than 0.5 V at 175 °C

#### **Applications** 3.

- 12 V, 24 V and 48 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

### Quick reference data

Quick reference data Table 1.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	-	100	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	-	85	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	-	238	W
Static characteristics							
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C}; Fig. 11$		-	9.5	12	mΩ
Dynamic characteristics							
$Q_{GD}$	gate-drain charge	$I_D = 25 \text{ A}; V_{DS} = 80 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ °C}; \underline{\text{Fig. 13}}; \underline{\text{Fig. 14}}$		-	24	-	nC



N-channel 100 V, 12 m $\Omega$  logic level MOSFET in LFPAK56

# 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb	D
2	S	source		
3	S	source	[q]	G
4	G	gate	و ق ق ق	mbb076 S
mb	D	mounting base; connected to drain	1 2 3 4 LFPAK56; Power- SO8 (SOT669)	

# 6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
BUK9Y12-100E	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669		

# 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Y12-100E	91210E

# 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	100	V
$V_{DGR}$	drain-gate voltage	$R_{GS}$ = 20 k $\Omega$		-	100	V
$V_{GS}$	gate-source voltage	DC; T <sub>j</sub> ≤ 175 °C		-10	10	V
		Pulsed; T <sub>j</sub> ≤ 175 °C	[1][2]	-15	15	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	238	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	85	Α
		V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 100 °C; <u>Fig. 2</u>		-	60	Α
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 \text{ °C}$ ; Fig. 3		-	339	Α

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### N-channel 100 V, 12 mΩ logic level MOSFET in LFPAK56

Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
Source-drain diode						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C		-	85	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$		-	339	Α
Avalanche ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 85 A; $V_{sup} \le 100$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[3][4]	-	139	mJ

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T<sub>j</sub> and or V<sub>GS</sub>
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.

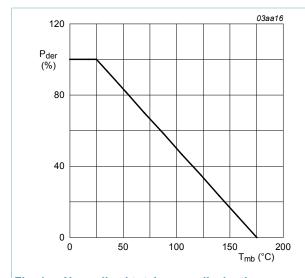


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

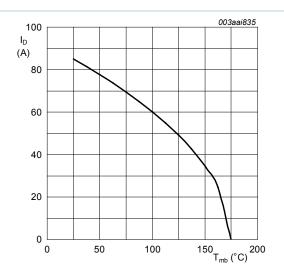


Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \ge 5V$$

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### N-channel 100 V, 12 m $\Omega$ logic level MOSFET in LFPAK56

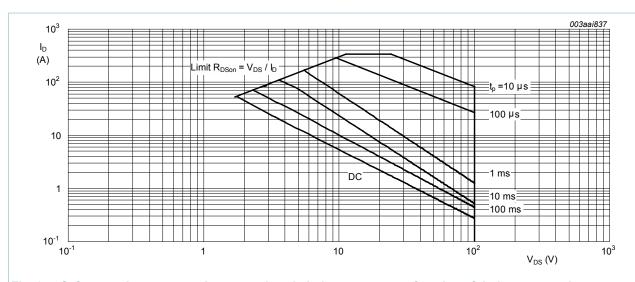
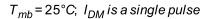


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



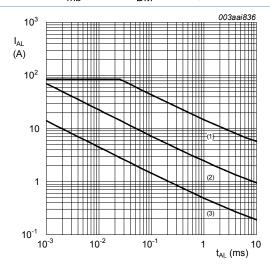


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

(1) 
$$T_{j(init)} = 25$$
°C; (2)  $T_{j(init)} = 150$ °C; (3) Repetitive Avalanche

### 9. Thermal characteristics

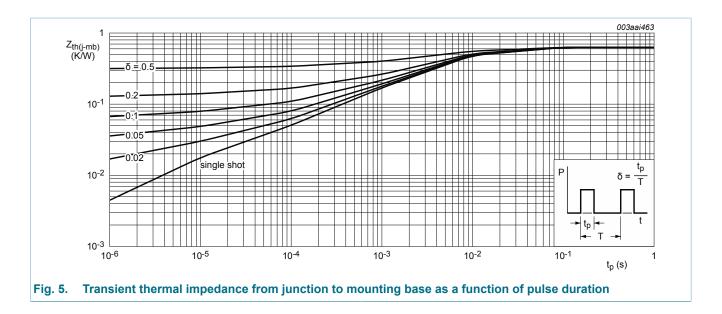
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	Fig. 5	-	-	0.63	K/W

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## N-channel 100 V, 12 m $\Omega$ logic level MOSFET in LFPAK56



# 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics					
V <sub>(BR)DSS</sub> drain-source		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 ^{\circ}C$	100	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}; Fig. 9;$ Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}; Fig. 9$	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C}; Fig. 9$	0.5	-	-	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.08	10	μA
		V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>	-	9.5	12	mΩ
	resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>	-	9.1	11.9	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; Fig. 11; Fig. 12	-	-	33.1	mΩ
Dynamic cl	haracteristics					
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 5 V;	-	64	-	nC
$Q_{GS}$	gate-source charge	T <sub>j</sub> = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	-	13	-	nC
$Q_{GD}$	gate-drain charge		-	24	-	nC

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Symbol	Parameter	Conditions	N	/lin	Тур	Max	Unit
C <sub>iss</sub>	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$	-	-	5980	7973	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 15</u>	-	-	349	419	pF
C <sub>rss</sub>	reverse transfer capacitance		-	-	214	293	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS}$ = 80 V; $R_{L}$ = 3.2 $\Omega$ ; $V_{GS}$ = 5 V; $R_{G(ext)}$ = 5 $\Omega$ ; $T_{j}$ = 25 °C	-	-	22	-	ns
t <sub>r</sub>	rise time		-	-	39	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	-	117	-	ns
t <sub>f</sub>	fall time		-	-	74	-	ns
Source-drain diode							
$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 16$	-	=	0.81	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S$ = 20 A; $dI_S/dt$ = -100 A/ $\mu$ s; $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; $T_j$ = 25 °C	-	-	47	-	ns
Q <sub>r</sub>	recovered charge		-	-	90	-	nC

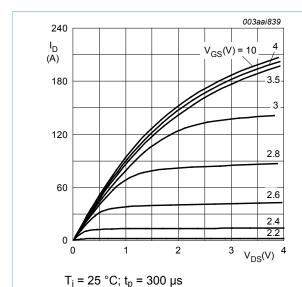


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

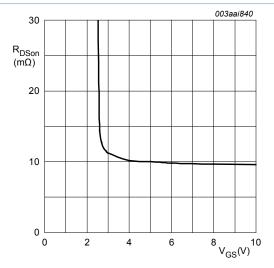


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^{\circ}C; I_D = 25A$$

### N-channel 100 V, 12 mΩ logic level MOSFET in LFPAK56

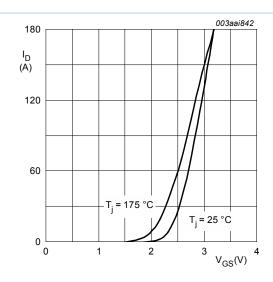


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



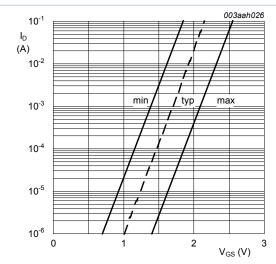


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^{\circ}C; \ V_{DS} = 5V$$

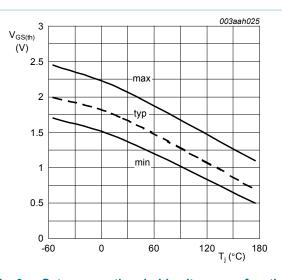
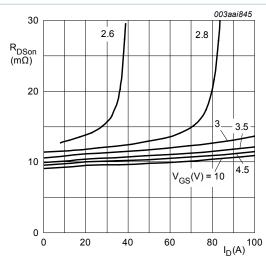


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D$$
 = 1 mA;  $V_{DS}$  =  $V_{GS}$ 



 $T_i$  = 25 °C;  $t_p$  = 300  $\mu$ s

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

### N-channel 100 V, 12 mΩ logic level MOSFET in LFPAK56

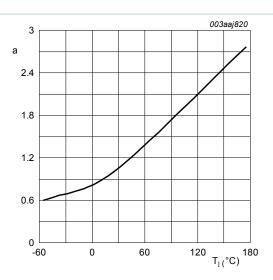


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}C)}$$

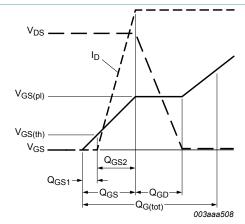


Fig. 14. Gate charge waveform definitions

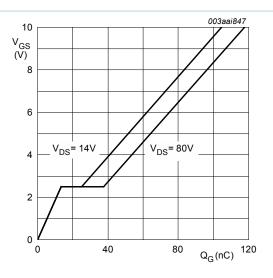


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25$$
°C;  $I_D = 25A$ 

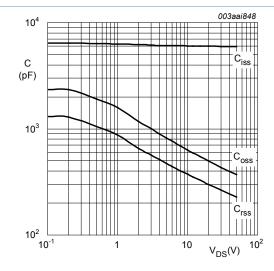


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V$$
;  $f = 1MHz$ 

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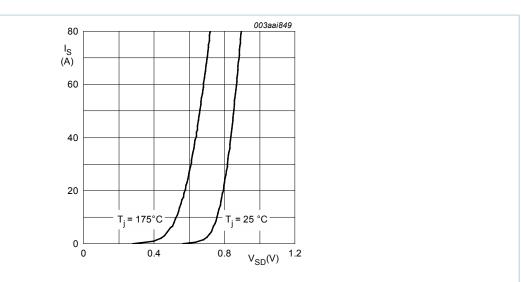
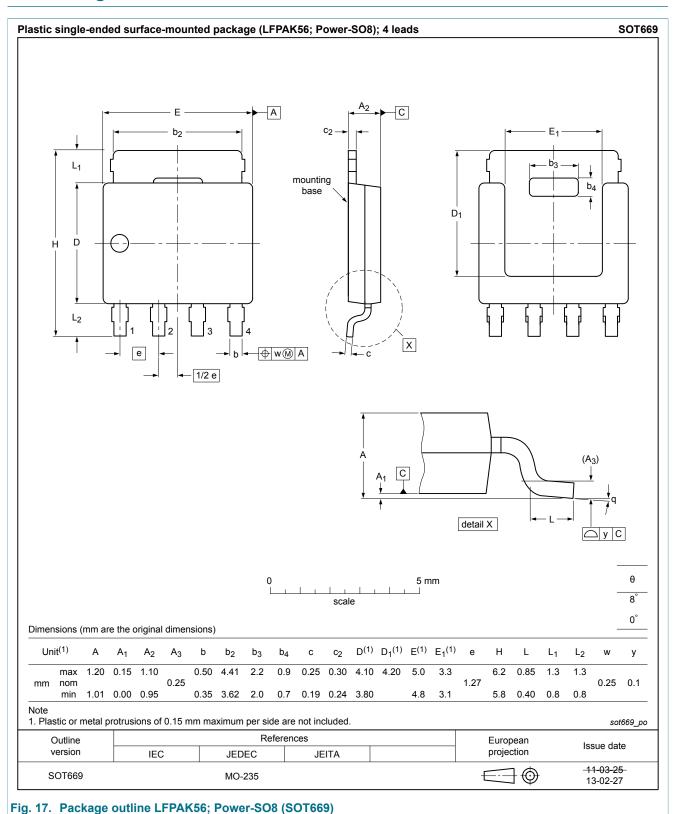


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values  $V_{GS} = 0V$ 

# 11. Package outline



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### N-channel 100 V, 12 mΩ logic level MOSFET in LFPAK56

## 12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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