THS8200-EP

All-Format Oversampled Component Video/PC Graphics D/A System With Three 11-Bit DACs, CGMS Data Insertion

Data Manual

Literature Number: SLES253
December 2009

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All-Format Oversampled Component Video/PC Graphics D/A System With Three 11-Bit DACs, CGMS Data Insertion

Check for Samples: THS8200-EP

1 Introduction

1.1 Features

- **Three 11-Bit 205-MSPS D/A Converters With Integrated Bi-Level/Tri-Level Sync Insertion**
- **Support for All ATSC Video Formats (Including 1080P) and PC Graphics Formats (Up to UXGA at 75 Hz)**

INPUT

- **Flexible 10/15/16/20/24/30-Bit Digital Video Input Interface With Support for YCbCr or RGB Data, Either 4:4:4 or 4:2:2 Sampled**
- **Video Synchronization Via Hsync, Vsync Dedicated Inputs or Via Extraction of Embedded SAV/EAV Codes According to ITU-R.BT601 (SDTV) or SMPTE274M/SMPTE296M (HDTV)**
- **Glueless Interface to TI DVI 1.0 (With HDCP) Receivers. Can Receive Video-Over-DVI Formats According to the EIA-861 Specification and Convert to YPbPr/RGB Component Formats With Separate Syncs or Embedded Composite Sync**

VIDEO PROCESSING

- **Programmable Clip/Shift/Multiply Function for Operation With Full-Range or ITU-R.BT601 Video Range Input Data**
- **Programmable Digital Fine-Gain Controller on Each Analog Output Channel, for Accurate Channel Matching and Programmable White-Balance Control**
- **Built-In 4:2:2 to 4:4:4 Video Interpolation Filter**
- **Built-In 2× Oversampling SDTV/HDTV Interpolation Filter for Improved Video Frequency Characteristic**
- **Fully Programmable Digital Color Space Conversion Circuit**
- **Fully Programmable Display Timing Generator to Supply All SDTV and HDTV Composite Sync Ttiming Formats, Progressive and Interlaced**
- **Fully Programmable Hsync/Vsync Outputs**
- **Vertical Blanking Interval (VBI) Override or Data Pass-Thru for VBI Data Transparency**
- **Programmable CGMS Data Generation and Insertion**

OUTPUT

- **Digital**
  - **ITU-R BT.656 Digital Video Output Port**
- **Analog**
  - **Analog Component Output from Software-Switchable 700-mV/1.3-V Compliant Output DACs at 37.5-Ω load**
  - **Programmable Video/Sync Ratio (7:3 or 10:4)**
  - **Programmable Video Pedestal**

GENERAL

- **Built-In Video Color Bar Test Pattern Generator**
- **Fast Mode I^2C Control Interface**
- **Configurable Master or Slave Timing Mode**
  - **Configuration Modes Allow the Device to Act as a Master Timing Source for Requesting Data from, e.g., the Video Frame Buffer. Alternatively, the Device Can Slave to an External Timing Master (Master Mode Only Available for PC Graphics Output Modes).**
- **DAC and Chip Powerdown Modes**
- **Low-Power 1.8-/3.3-V Operation**
- **80-pin PowerPAD™ Plastic Quad Flatpack Package with Efficient Heat Dissipation and Small Physical Size**

APPLICATIONS

- **DVD Players**
- **Digital-TV/Interactive-TV/Internet Set-Top Boxes**
- **Personal Video Recorders**
- **HDTV Display or Projection Systems**
- **Digital Video Systems**

2 Overview

2.1 Description

THS8200 is a complete video back-end D/A solution for DVD players, personal video recorders and set-top boxes, or any system requiring the conversion of digital component video signals into the analog domain.

THS8200 can accept a variety of digital input formats, in both 4:4:4 and 4:2:2 formats, over a 3×10-bit, 2×10-bit or 1×10-bit interface. The device synchronizes to incoming video data either through dedicated Hsync/Vsync inputs or through extraction of the sync information from embedded sync (SAV/EAV) codes inside the video stream. Alternatively, when configured for generating PC graphics output, THS8200 also provides a master timing mode in which it requests video data from an external (memory) source.

THS8200 contains a display timing generator that is completely programmable for all standard and nonstandard video formats up to the maximum supported pixel clock of 205 MSPS. Therefore, the device supports all component video and PC graphics (VESA) formats. A fully-programmable 3×3 matrixing operation is included for color space conversion. All video formats, up to the HDTV 1080I and 720P formats, can also be internally 2× oversampled. Oversampling relaxes the need for sharp external analog reconstruction filters behind the DAC and improves the video frequency characteristic.

The output compliance range can be set via external adjustment resistors and there is a choice of two settings, in order to accommodate without hardware changes both component video/PC graphics (700 mV) and composite video (1.3 V) outputs. An internal programmable clip/shift/multiply function on the video data assures standards-compliant video output ranges for either full 10-bit or reduced ITU-R.BT601 style video input. In order to avoid nonlinearities after scaling of the video range, the DACs are internally of 11-bit resolution. Furthermore, a bi- or tri-level sync with programmable amplitude (in order to support both 700/300-mV and 714/286-mV video/sync ratios) can be inserted either on the green/luma channel only or on all three output channels. This sync insertion is generated from additional current sources in the DACs such that the full DAC resolution remains available for the video range. This preserves 100% of the DAC's 11-bit dynamic range for video data.

THS8200 optionally supports the pass-through of ancillary data embedded in the input video stream or can insert ancillary data into the 525P analog component output according to the CGMS data specification.

2.2 Ordering Information

T_A	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PFP	THS8200IPFPEP	THS8200IEP

2.3 DEVICE INFORMATION

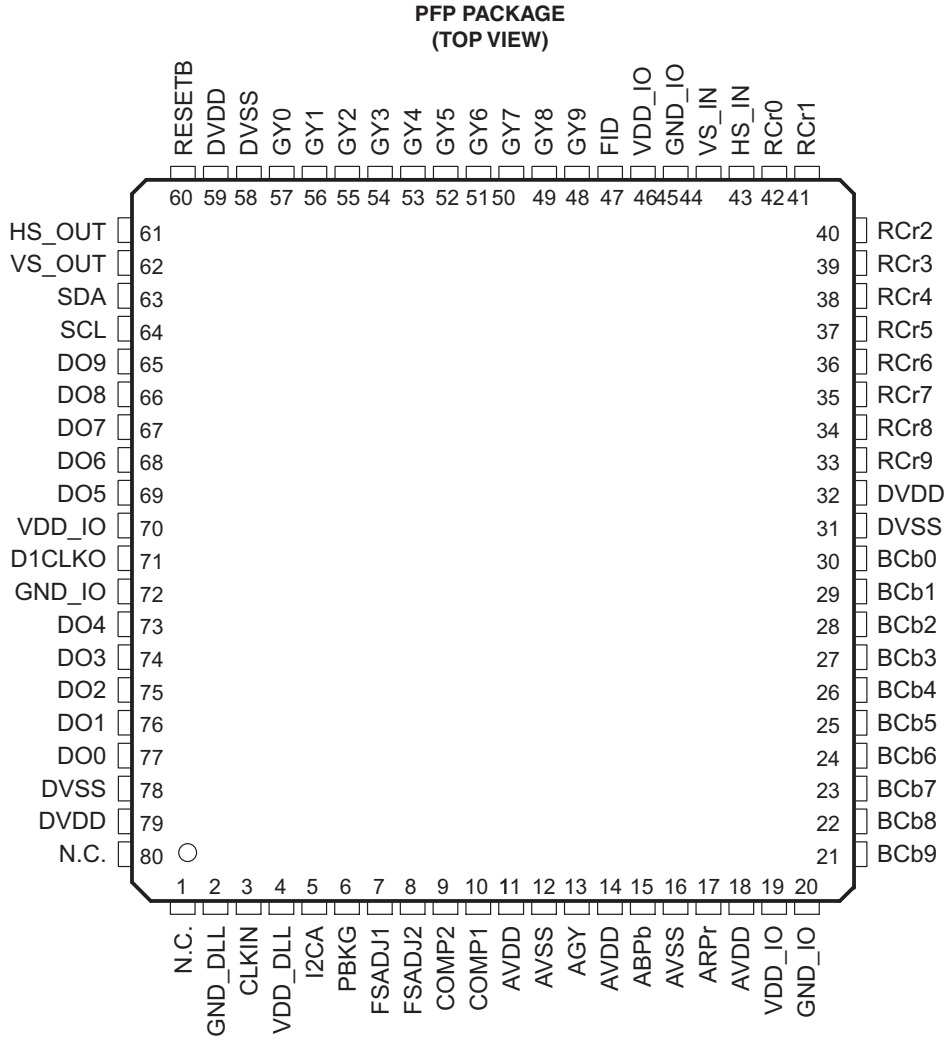


Table 2-1. TERMINAL FUNCTIONS

TERMINAL		I/O(1)	DESCRIPTION
NAME	NO.		
ABPb	15	O	Analog output of DAC2. See AGY.
ARPr	17	O	Analog output of DAC3. See AGY.
AG Y	13	O	Analog output of DAC1. With the proper setting of FSADJ<n>, this output is capable of driving 1.3-V full scale into a 37.5-Ω load.
AVDD	11, 14, 18	PWR	Analog power supply, nominal 3.3 V
AVSS	12, 16	PWR	Analog ground
BCb[9:0]	21 - 30	I	10-bit video data input port. All 10 bits or the 8 MSB of this port can be connected to the video data source. In 30-bit mode, the B data of RGB, or the Cb data of YCbCr, should be connected to this port. In 10-bit input mode, this port is unused. In 20-bit input mode, this port is used for CbCr input data.
CLKIN	3	I	Main clock input. Video input data on the GY[9:0]/BCb[9:0]/RCr[9:0] ports should be synchronized to CLKIN. Depending on the input data format, CLKIN is supplied to THS8200 at 1x or 2x the pixel clock frequency.
COMP1	10	P	Compensation pin for the internal reference amplifier. A 0.1-µF capacitor should be connected between COMP1 and analog power supply AVDD.
COMP2	9	P	Compensation pin for the internal reference amplifier. A 0.1-µF capacitor should be connected between COMP2 and analog power supply AVDD.
D1CLKO	71	O	Video ITU-R.BT656-compliant clock output. This clock output is off by default and should be activated via an I^2C register setting.
DO[9:5] DO[4:0]	65 - 69 73 - 77	O	ITU-R.BT656 compliant video data output port. Only available when ITU-R.BT656 input format is used. Can be used to connect to external PAL/NTSC video encoder. This port is off by default and should be activated via an I^2C register setting.
DVDD	32, 59, 79	PWR	Digital core power, nominal 1.8 V
DVSS	31, 58, 78	PWR	Digital core ground
FID	47	I	Field identification signal for interlaced video formats. In slave timing mode, this is an input from the video data source. In master timing mode this signal is unused, as only progressive-scan VESA formats are supported in master mode.
FSADJ1	7	P	Full scale adjustment control 1. A resistor should be connected between FSADJ1 and analog ground AGND to control the full-scale output current of the DAC output channels. Via the data_fsadj I^2C programming register, the user can select between two full-scale ranges, determined by FSADJ1 or FSADJ2. For 700-mV video output (1 Vpp including sync), the nominal value is 2.99 kΩ ; for 1.0-Vpp video output (1.3 Vpp including sync) output the nominal value is 2.08 kΩ.
FSADJ2	8	P	Full scale adjustment control 2. See FSADJ1.
GND_DLL	2	PWR	Ground of clock doubler. Should be connected to analog ground.
GND_IO	20, 45, 72	PWR	I/O ring ground
GY[9:0]	48 - 57	I	10-bit video data input port. All 10 bits or the 8 MSB of this port can be connected to the video data source. The G data of RGB or the Y data of YCbCr should be connected to this port. Port used in 10-bit mode for CbYCrY video input data; in 20-bit input mode for Y data.
HS_IN	43	I/O	Horizontal source synchronization. In slave timing mode, this is an input from the video data source. In master timing mode, this is an output to the video data source with programmable timing and polarity, serving as a horizontal data qualification signal to the video source.
HS_OUT	61	O	Horizontal sync output (to display). Irrespective of slave/master timing mode configuration, this is always an output with timing generated by the DTG.
12CA	5	I	I^2C device address LSB selection
N.C.	1, 80	I	Manufacturing test input. Must be tied to GND for normal operation.
PBKG (VSS)	6	PWR	Substrate ground. Should be connected to analog ground.
RCr[9:0]	33 - 42	I	10-bit video data input port. All 10-bits or the 8 MSB of this port can be connected to the video data source. In 30-bit mode, the R data of RGB or the Cr data of YCbCr should be connected to this port. In the 10- /20-bit input mode, this port is unused. For some input formats this port is unused.
RESETB	60	I	Software reset pin (active low). The minimum reset duration is 200 ns.

(1) I = input, O = output, B = bidirectional, PWR = power or ground, P = passive

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O[1]	DESCRIPTION
NAME	NO.		
SCL	64	B	Serial clock line of I^2C bus interface. Open-collector. Maximum specified clock speed is 400 kHz (fast I^2C).
SDA	63	B	Serial data line of I^2C bus interface. Open-collector.
VDD_DLL	4	PWR	Power supply of clock doubler, nominal 1.8 V
VDD_IO	19, 46, 70	PWR	I/O ring power, 1.8 V or 3.3 V nominal
VS_IN	44	I/O	Vertical source synchronization. In slave timing mode, this is an input from the video data source. In master timing mode, this is an output to the video data source with programmable timing and polarity, serving as a vertical data qualification signal to the video source.
VS_OUT	62	O	Vertical sync output (to display). Irrespective of slave/master timing mode configuration, this is always an output with timing generated by the DTG.

3 THS8200 Functional Overview

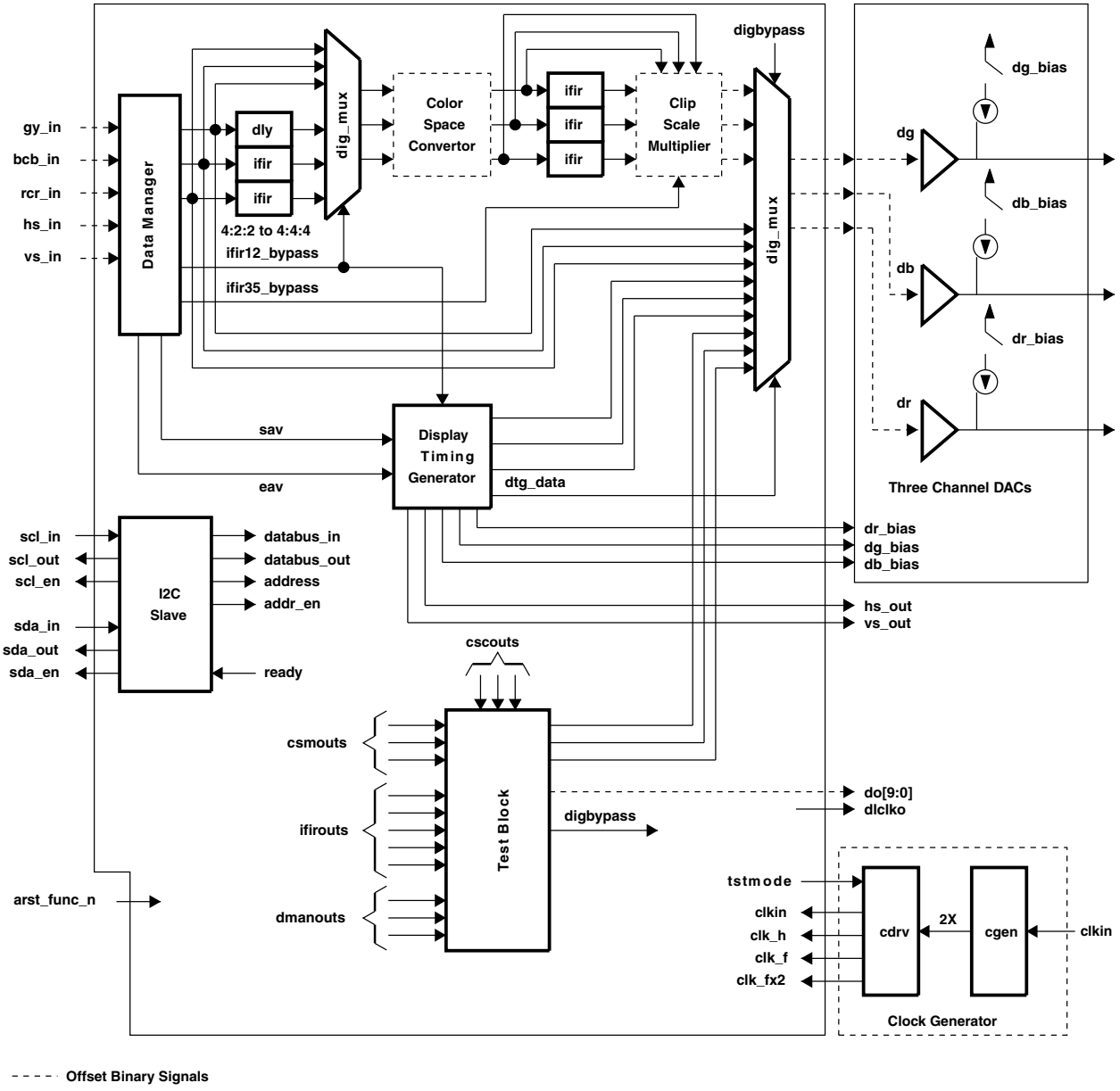


Figure 3-1. Functional Block Diagram

3.1 Data Manager (DMAN)

The data manager is the block that transforms the selected input video data format present on the chip input bus(es) to an internal 10-bit three-channel representation. Supported input formats include 10-/8-bit ITU-R.BT656 with embedded sync codes, 15-/16- or 24-/30-bit RGB with external sync, 20-/16-bit SMPTE274M/296M with embedded sync codes, as well as 20-/16-bit YCbCr 4:2:2 with external sync. The user can optionally include a 4:2:2 to 4:4:4 interpolation on the color data path. When a format with embedded sync is selected, DMAN also extracts H(Hsync), V(Vsync), F(FieldID) identifiers from the ITU-R.BT656 (SDTV) or SMPTE274M/296M (HDTV) data stream for internal synchronization of the DTG. Alternatively, the device synchronizes to HS_IN, VS_IN, FID inputs.

3.1.1 Interpolating Finite Impulse Responses Filter (IFIR)

The interpolating FIR is used to upsample the input data by 2×. In the THS82000 there are five IFIRs. The first two are used only when the input data is in 4:2:2 format for conversion to a 4:4:4 internal representation on both color difference channels. The last three IFIRs are used to upsample the internal data to the DACs on all three channels in case 2× video interpolation is enabled. By 2× oversampling the video data, the requirements for the analog reconstruction filter at the DAC outputs are relaxed so it can be built with fewer components, thereby also improving the overall video frequency characteristic (less group delay variation). All of the IFIRs can be bypassed or switched in by programming the appropriate I^2C registers. The coefficients of all IFIRs are fixed.

3.1.2 Color-Space Conversion (CSC)

The color-space converter block is used to convert input video data in one type of color space to output video data in another color space (e.g., RGB to YCbCr, or vice versa). This block contains a 3×3 matrix multiplier/adder and a 3×1 adder. All multiplier and adder coefficients can be programmed via the I^2C interface to support any linear matrixing+offset operation on the video data.

3.1.3 Clip/Shift/Multiplier (CSM)

The clip-shift-multiply block optionally clips the input code range at a programmed low/high code, shifts the input video data downwards, and multiplies the input by a programmable coefficient in the range 0−1.999. This allows for operation with a reduced input code range such as prescribed in the ITU-R.BT601 recommendation. Each channel can be independently programmed to accommodate different digital ranges for each of the three input channels. For example, for standard video signals the Y channel has a digital input range of 64−940, whereas the two other channels have an input range of 64−960. All three channels must have a DAC output range of 0−700 mV, so normally the analog voltage corresponding to 1 LSB would have to change to account for the different digital inputs. This might cause matching errors. Therefore in the THS8200 the DAC LSB does not change; rather LSB conversion is done by scaling the digital inputs to the DAC's full input range. Furthermore, the CSM output is 11 bits wide and is sent to the 11-bit DACs. The extra bit of resolution resolves nonlinearities introduced by the scaling process. The clipping function can be switched off to allow for super-white/super-black excursions.

3.1.4 Digital Multiplexer (DIGMUX)

This multiplexer in front of the DACs can select between video signals at 1× or 2× the pixel clock rate. It is also used to switch in blanking/sync level data generated by the display timing generator (DTG) block and test pattern data (e.g., color bars, I^2C-controlled DAC levels) or to perform data insertion (CGMS) during vertical blanking.

3.1.5 Display Timing Generator (DTG)

The display timing generator is responsible for the generation of the correct frame format including all sync, equalization and serration pulses. In master timing mode, the DTG is synchronized to external synchronization inputs, either from the dedicated device terminals HS_IN, VS_IN, and FID or is synchronized to the identifiers extracted from the input data stream, as selected by the DMAN mode. In master timing mode, the DTG generates the required field/frame format based on the externally applied pixel clock input.

When active data is not being passed to the DACs, i.e., during the horizontal/vertical blanking intervals, the DTG generates the correct digital words for blank, sync levels and other level excursions, such as pre- and post-serration pulses and equalization pulses.

Horizontal timings, as well as amplitudes of negative and positive sync, HDTV broad pulses and SDTV pre- and post-equalization and serration pulses, are all I^2C-programmable to accommodate, e.g., the generation of both EIA.770-1 (10:4 video/sync ratio) and EIA.770-2 (7:3 video/sync ratio) compliant analog component video outputs, and to support nonstandard video timing formats.

In addition or as an alternative to the composite sync inserted on green/luma channel or all analog outputs, output video timing can be carried via dedicated Hsync/Vsync output signals as well. The position, duration and polarity of Hsync and Vsync outputs are fully programmable in order to support, for example, the centering of the active video window within the picture frame.

The DTG also controls the data multiplexer in the DIGMUX block. DIGMUX can be programmed to pass device input data only on active video lines (inserting DTG-generated blanking level during blanking intervals). Alternatively, the DTG can pass device input data also during some VBI lines (ancillary data in the input stream is passed transparently on some VBI lines). Finally, the device can also generate its own ancillary data and insert it into the analog outputs according to the CGMS data format for the 525P video format.

3.1.6 Clock Generator (CGEN)

The clock generator is an analog delay-locked loop (DLL) based circuit and provides a 2× clock from the CLKIN input. The 2× clock is used by the CDRV block for 2× video interpolation. Some video formats also require a 1/2 rate clock used for 4:2:2 to 4:4:4 conversion.

3.1.7 Clock Driver (CDRV)

The clock drive block generates all on-chip clocks. Its inputs are control signals from the digital logic, the original CLKIN, and the 2× clock from CGEN. Outputs include a half-rate clock, full-rate clock, and a 2× full-rate clock. The clocks are used for both optional on-chip interpolation processes: 4:2:2 to 4:4:4 interpolation and 1× to 2× video oversampling.

3.1.8 I^2C Host Interface (I2CSLAVE)

The I^2C interface controls and programs the internal I^2C registers. The THS8200 I^2C interface implementation supports the fast I^2C specification (SCL: 400 kHz) and allows the writing and reading of registers. An auto-increment addressing feature simplifies block register programming. The I^2C interface works without a clock present on CLKIN.

3.1.9 Test Block (TST)

The test block controls all the test functions of the THS8200. In addition to manufacturing test modes, this block contains several user test modes including a DAC internal ramp generator and a 75% SMPTE video color bar generator.

3.1.10 D/A Converters (DAC)

THS8200 contains three DACs operating at up to 205 MSPS and with an internal resolution of 11 bits. Each DAC contains an integrated video sync inserter. The sync(s) is (are) inserted by means of additional current source circuits either on the green/luma (Y) channel only or on all the DAC output channels, in order to be compliant with both consumer (EIA, sync-on-G/Y) as well as professional (SMPTE, sync-on-all) standards.

The DAC speed supports all ATSC formats, including 1080P, as well as all PC graphics (VESA) formats up to UXGA at 75 Hz (202.5 MSPS).

4 Detailed Functional Description

4.1 Data Manager (DMAN)

Table 4-1. Supported Input Formats

	INPUT INTERFACE					TIMING CONTROL		SYNCHRONIZATION	
	30 BIT	20 BIT	10 BIT(1)	16 BIT	15 BIT	EMBEDDED TIMING	DEDICATED TIMING	MASTER	SLAVE
[PRESET] HDTV-SMPTE296M progressive (720P)	X (4:4:4)	X (4:2:2)				X	X		X
[PRESET] HDTV-SMPTE274M progressive (1080P)	X (4:4:4)	X (4:2:2)				X	X		X
[PRESET] HDTV-SMPTE274M progressive (1080I)	X (4:4:4)	X (4:2:2)				X	X		
[GENERIC] HDTV	X (4:4:4)	X (4:2:2)				X	X		X
[PRESET] SDTV-ITU.1358 (525P)	X (4:4:4)	X (4:2:2)	X(2)			X	X(3)		X
[PRESET] SDTV-ITU-R.BT470 (525I)	X (4:4:4)	X (4:2:2)	X(4)			X	X(3)		X
[PRESET] SDTV-ITU-R.BT470 (625i)	X (4:4:4)	X (4:2:2)	X(4)			X	X(3)		X
[GENERIC] SDTV	X (4:4:4)	X (4:2:2)				X	X		X
[PRESET] VESA	X (5)			X(5)	X(5)		X	X	X

(1) When the device is configured to receive data over a 10-bit interface, the ITU-R.BT656 output bus on the THS8200 can be enabled via an I^2C register bit to send the received data to an external device. In other DMAN modes, this output should remain off (data_tristate656 register).
(2) SMPTE293M-compliant
(3) Dedicated timing not supported with 10-bit interface.
(4) ITU-R.BT656-compliant
(5) Because PC graphics data is normally only 8 bits wide, only 3×8 bits (8 MSBs of each bus) are used. Color space converter bypass is required for modes with pixel clock > 150 MSPS.

Table 4-1 summarizes all supported video mode configurations.

Each video mode is characterized by three attributes:

- **Input Interface**: Data is accepted over 10-, 20- or 30-bit interface (or 8- ,16-, 24-bit interface for 8-bit data when using 8 MSBs of each input data bus and connecting 2 LSBs to ground). This selection is controlled by the dman_cntl register.
- **Timing control**: Video timing is either embedded in the data stream or supplied via dedicated timing signals. In the latter case additional Hsync (HS_IN), Vsync (VS_IN) and FieldID (FID) input signals are required to synchronize the video data source and THS8200 in the case of slave timing mode. This selection is controlled by the dtg2_embedded_timing register.
- **Synchronization**: Video timing either is supplied to the device (slave) or the THS8200 requests video data from the source (master). This selection is controlled by the chip_ms register.

NOTE

Device operation with combinations of settings for the dman_cntl, dtg2_embedded_timing and chip_ms registers that result in operating modes not marked in Table 4-1 is not assured. See detailed register map description for actual register settings.

Furthermore, Table 4-1 shows for which modes presets are defined. When in a preset video mode, the line-type/breakpoint-pairs that define the frame format (see Display Timing Generator, Section 4.7) are preprogrammed. Therefore the user does not need to define the table with line type/breakpoint settings, nor does the field and frame size need to be programmed. However, when in preset mode, the horizontal parameters (all dtg1_spec_x registers for the line types used by the preset setting, and dtg1_total_pixels registers) still need to be programmed. Presets are available for most popular DTV video formats. Alternatively, generic modes for SDTV, HDTV or VESA can be selected, which allow full programmability of the field/frame sizes and DTG parameters.

Note from the table that:

- If embedded timing is used, the device is always in slave mode, because the data stream supplied to THS8200 contains the video timing information.
- Master operation is only supported for PC graphics (VESA) formats.
- In HDTV modes with embedded timing, data is supplied to the device over a 20-bit interface, as defined in SMPTE274/296M.
- In SDTV modes with embedded timing, data is supplied to the device over a 10-bit interface. When the video format is interlaced, this interface is known as ITU-R.BT656 (525I, 625I). When the video format is progressive, only 525P is supported with embedded timing. The 625P interface can be supported with dedicated timing, using the SDTV generic mode.
- In generic modes with dedicated timing, both 20 bits (4:2:2) and 30 bits (4:4:4) are supported.
- In PC graphics modes (VESA generic), input data is either over the 30-bit interface or over the 16-/15-bit interface and always has dedicated timing. Note that the 16-bit interface is not equivalent to a 2×8-bit version of the 20-bit interface; see Section 4.2, Input Interface Formats, for details.

4.2 Input Interface Formats

The following figures define the input video format for each input mode, as selected by the data_dman_cntl register setting. Video data is always clocked in at the rising edge of CLKIN.

NOTE

For 8-bit operation with 10-bit input buses, connect only the 8 MSBs of each input bus used, and tie the 2 LSBs to ground.

- 30-bit YCbCr/RGB 4:4:4

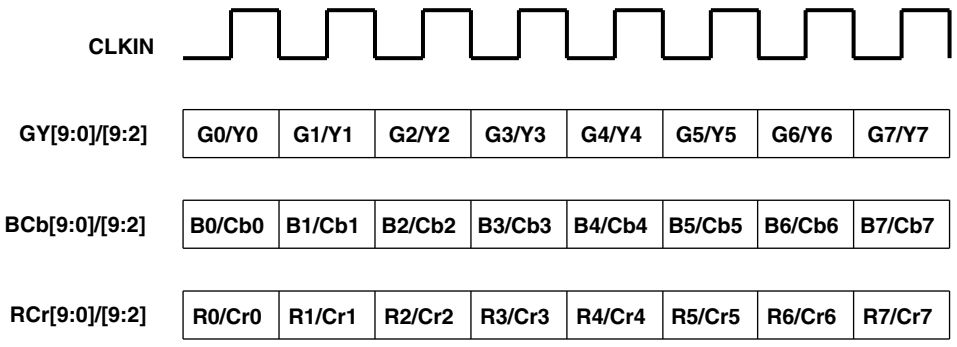


Figure 4-1. 24-/30-Bit RGB or YCbCr Data Format

- 20-bit YCbCr 4:2:2

  CLKIN is equal to the 1× pixel clock. The pixel clock equals the rate of the Y input and is 2× the rate of the 2 other channels in this input format where Cb and Cr are multiplexed onto the same input bus.

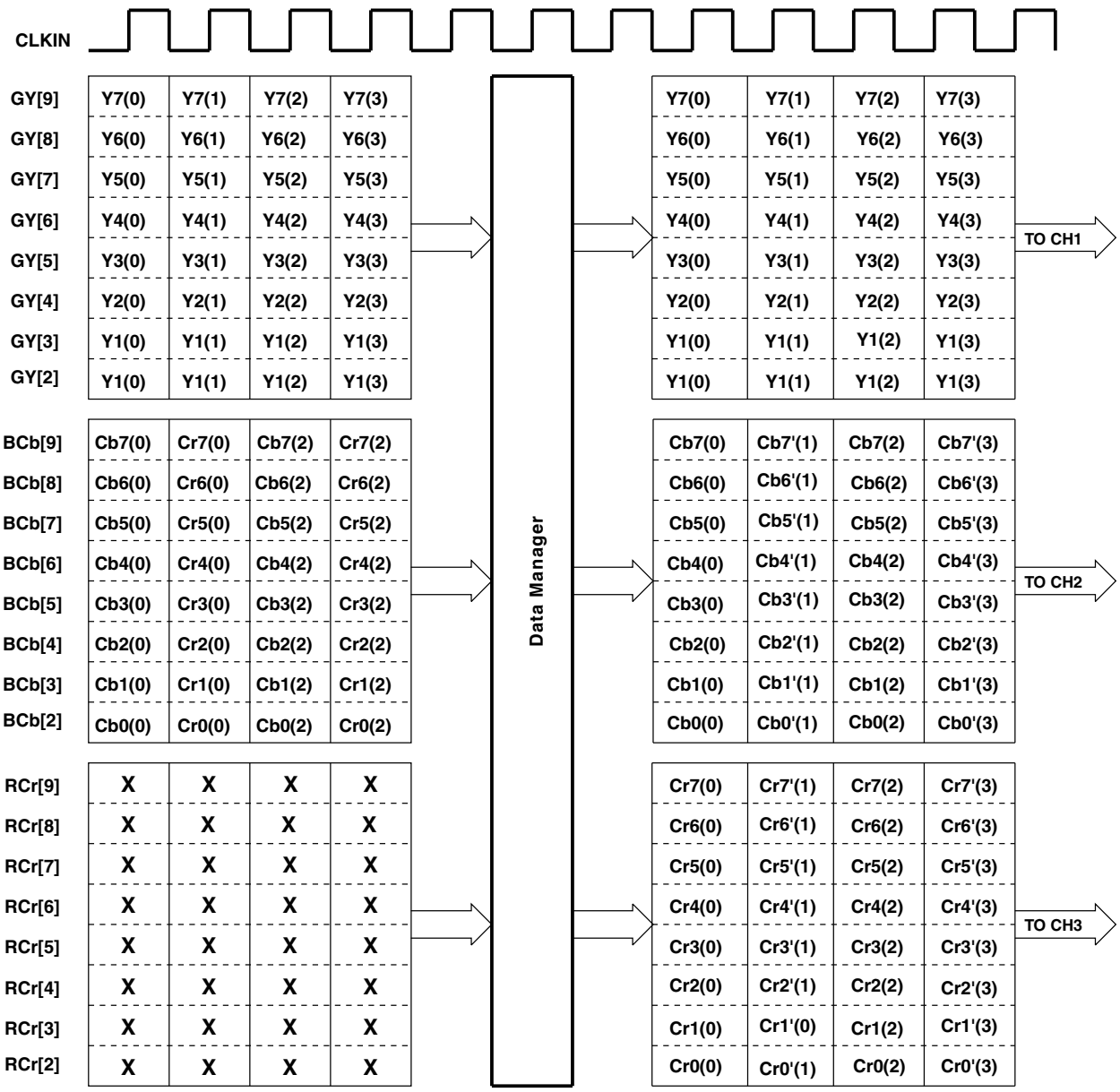


Figure 4-2. 20-/16-Bit YCbCr 4:2:2 Data Format (16-Bit Operation Shown)

When dedicated timing is used in this mode, there is a fixed relationship between the first active period of HS_IN (i.e., the first CLKIN rising edge seeing HS_IN active) and a Cb color component assumed present during that clock period on the bus receiving CbCr samples. When embedded timing is used in this mode, the SAV/EAV structure also unambiguously defines the CbCr sequence, according to SMPTE274M/296M for HDTV.

NOTE

The figure shows the case when only 8 bits of each 10-bit input bus are used.

- 10-bit YCbCr 4:2:2 (ITU mode)

  CLKIN is equal to 2× the pixel clock since all components are multiplexed on a single 10-bit bus with a 4-multiple sequence: CbYCrY. Therefore the pixel clock (i.e., the Y input rate) is 1/2 of CLKIN and the Cb and Cr rate are 1/4 of CLKIN.

  When dedicated timing is used in this mode, there is a fixed relationship between the first active period

of HS_IN (i.e. the first CLKIN rising edge seeing HS active) and a Cb color component assumed present during that clock period on the input bus. When embedded timing is used in this mode, the SAV/EAV structure also unambiguously defines the CbCr sequence, according to ITU-R.BT656 (for 625I and 525I) and SMPTE293M (for 525P).

- 16-bit RGB 4:4:4

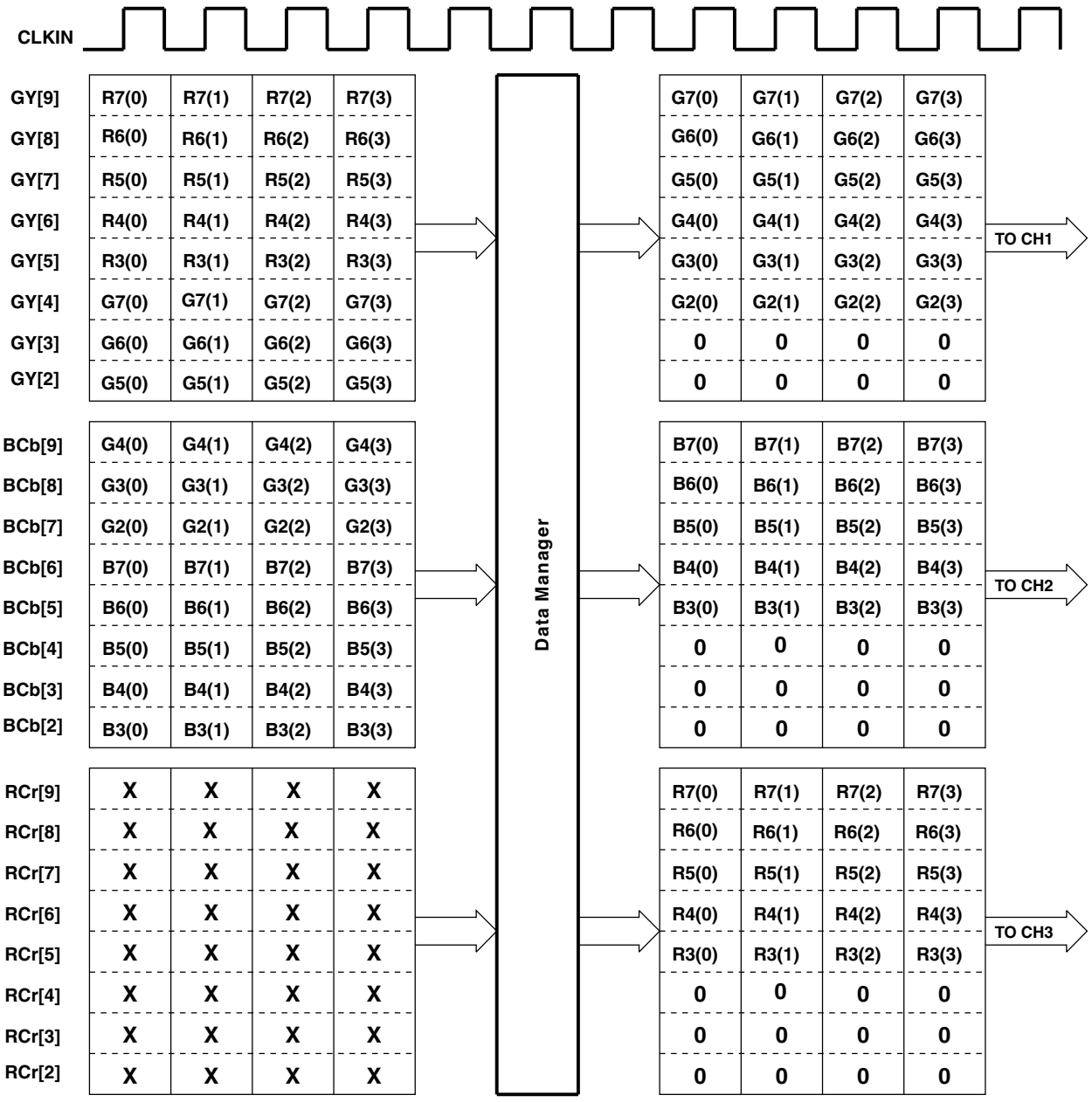


Figure 4-3. 16-Bit RGB 4:4:4 Data Format

CLKIN is equal to 1× the pixel clock. This format is only supported in VESA mode and can be used for PC graphics applications that do not require full 8-bit resolution on each color component.

- 15-bit RGB 4:4:4

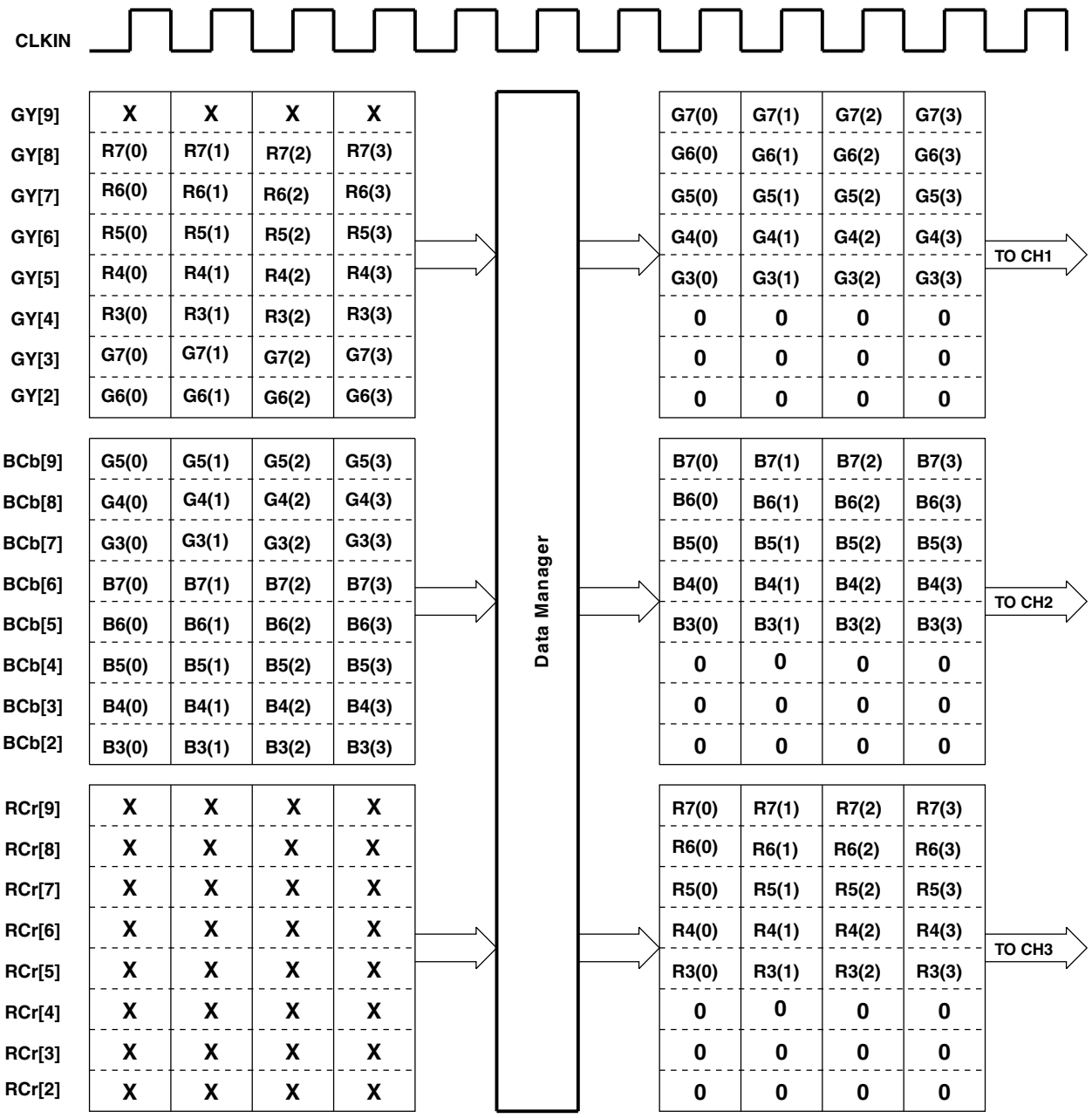


Figure 4-4. 15-Bit RGB 4:4:4 Data Format

CLKIN is equal to 1× the pixel clock. This format is only supported in VESA mode and can be used for PC graphics applications that do not require full 8-bit resolution on each color component.

4.3 Clock Generator (CGEN)/Clock Driver (CDRV)

The clock generator/clock driver blocks generate all on-chip clocks for 4:2:2 to 4:4:4 and 2× video oversampling. The DMAN setting controls whether the input data is 4:2:2 or 4:4:4 sampled, and whether a 30-, 20- or 10-bit interface is used. This selection affects the clock input frequency assumed to be present on CLKIN.

- **30-bit 4:4:4**: 1× pixel clock. 4:2:2 to 4:4:4 interpolation should be bypassed. Optional 2× oversampling is available for formats with pixel clock up to 80 MHz.

- **20-bit 4:2:2**: 1× pixel clock. 4:2:2 to 4:4:4 interpolation should be switched in, and is available for formats with pixel clock up to 150 MHz. Optional 2× oversampling available for formats with pixel clock up to 80 MHz.
- **10-bit 4:2:2 (ITU)**: 1/2× pixel clock. 4:2:2 to 4:4:4 interpolation should be switched in, and is available for formats with pixel clock up to 150 MHz. Optional 2× oversampling is available for formats with pixel clock up to 80 MHz.

The internal DLL (delay-locked loop) generates the higher clock frequencies. The user should program the input frequency range selection register, dll_freq_sel, according to the frequency present on CLK_IN when using either or both interpolation/oversampling stages.

The 4:2:2 to 4:4:4 stage is switched in or bypassed, depending on the setting of data_ifir12_bypass register (interpolation only on chroma channels). This feature should only be used with YCbCr 4:2:2 input. The THS8200 can perform color space conversion to RGB depending on the CSC setting. The dtg2_rgbmode_on register should be set corresponding to the color space representation of the DAC output.

The 2× oversampling stage is switched in or bypassed, depending on the setting of data_ifir35_bypass register.

The user should not enable the 2× oversampling stage when the CLK_IN frequency exceeds 80 MHz, as is the case for the higher PC graphics formats and 1080P HDTV. In this case the DLL should be bypassed using the vesa_clk register to disable the 2× frequency generation. As explained in the detailed register map description for this register, it is still possible to support 20-bit 4:2:2 input in this mode (e.g., for 1080P).

A second bypass mode operation exists for the DLL, enabled by the dll_bypass register. When this bypass mode is active, the CLKIN input is assumed to be 2× pixel frequency. This mode is meant only for test purposes as it does not correspond to any mode in the supported input formats table.

4.4 Color Space Conversion (CSC)

THS8200 contains a fully-programmable 3×3 multiply/add and 3×1 adder block that can be switched in for all video formats up to a pixel clock frequency of 150 MHz. Color space conversion is thus available for all DTV modes, including 1080P and VESA modes up to SXGA at 75 Hz (135 MSPS). The operation is done after optional 4:2:2 to 4:4:4 conversion, and thus on the 1× pixel clock video data prior to optional 2× video oversampling. The CSC block can be switched in or bypassed depending on the setting of register csc_bypass.

Each of the nine floating point multiplier coefficients of the 3×3 multiply/add is represented as the combination of a 6-bit signed binary integer part, and a 10-bit fractional part. The integer part is a signed magnitude representation with the MSB as the sign bit. The fractional part is a magnitude representation; see the following example.

The register nomenclature is: csc_<r,g,b> <i,f>c<1,2,3> where:

- <r,g,b> identifies which input channel is multiplied by this coefficient (r = red/Cr, g = green/Y, b = blue/Cb input).
- <i,f> identifies the integer (i) or fractional (f) part of the coefficient.
- <1,2,3> identifies the output channel from the color space converter: 1 = Yd/Gd, 2 = Cb/Bd, 3 = Cr/Rd.

For the offset values, a value of 1/4 of the desired digital offset needs to be programmed in the individual offset register, so a typical offset of 512 (offset over 1/2 of the video range) requires programming a value of 128 decimal into the offset<1,2,3> registers, where again <1,2,3> defines the output channel affected, with similar convention as shown previously.

Saturation logic can be switched in to avoid over- and underflow on the result after color space conversion using the csc_uof_cntl register.

We next show an example of how to program the CSC. This also explains the numeric data formats.

CSC configuration example: HDTV RGB to HDTV YCbCr

The formulas for RGB to YCbCr conversion are:

- Yd = 0.2126*Rd + 0.7152*Gd + 0.0722*Bd
- Cb = −0.1172*Rd – 0.3942*Gd + 0.5114*Bd + 512
- Cr = 0.5114*Rd – 0.4646*Gd – 0.0468*Bd + 512

To program the red coefficient of channel 1 (Y) with the value of 0.2126 the following must be done:

1. Realize that this is a positive value so the sign bit of the integer part is 0 (bit 5 of csc_ric1 = 0).
2. Note that there is no integer portion of the coefficient (bit 4−bit 0 = 00000).
3. The binary representation of the fractional part can be constructed directly from the binary equivalent of the fractional part multiplied by 1024 (0.2126 × 1024 = 217.7), rounded to the nearest integer (218) and represented as a binary 10-bit number (00 1101 1010).

Using the above method all the registers for the CSC blocks can be programmed with the correct value for RGB to YCbCr conversion. Below is a complete list of register values for the above conversion.

0.2126 → csc_ric1 = 00 0000	csc_rfc1 = 00 1101 1010
0.7152 → csc_gic1 = 00 0000	csc_gfc1 = 10 1101 1100
0.0722 → csc_bic1 = 00 0000	csc_bfc1 = 00 0100 1010
−0.1172 → csc_ric2 = 10 0000	csc_rfc2 = 00 0111 1000
−0.3942 → csc_gic2 = 10 0000	csc_gfc2 = 01 1001 0100
0.5114 → csc_bic2 = 00 0000	csc_bfc2 = 10 0000 1100
0.5114 → csc_ric3 = 00 0000	csc_rfc3 = 10 0000 1100
−0.4646 → csc_gic3 = 10 0000	csc_gfc3 = 01 1101 1100
−0.0468 → csc_bic3 = 10 0000	csc_bfc3 = 00 0011 0000

For the offsets necessary in the second and third equation the csc_offset<n> registers need to be programmed. We need to add 512 to the Cb and Cr channels. The value to be programmed is 1/4 of this offset in a signed magnitude representation, thus 128 or csc_offset2 = csc_offset3 = 00 1000 0000.

Packing these individual registers into the I^2C register map, the programmed values are:

SUBADDRESS	REGISTER NAME	VALUE
0x04	csc_r11	0000 0000
0x05	csc_r12	1101 1010
0x06	csc_r21	1000 0000
0x07	csc_r22	0111 1000
0x08	csc_r31	0000 0010
0x09	csc_r32	0000 1100
0x0A	csc_g11	0000 0010
0x0B	csc_g12	1101 1100
0x0C	csc_g21	1000 0001
0x0D	csc_g22	1001 0100
0x0E	csc_g31	1000 0001
0x0F	csc_g32	1101 1100
0x10	csc_b11	0000 0000
0x11	csc_b12	0100 1010
0x12	csc_b21	0000 0010
0x13	csc_b22	0000 1100
0x14	csc_b31	1000 0000
0x15	csc_b32	0011 0000
0x16	csc_offs1	0000 0000
0x17	csc_offs12	0000 1000
0x18	csc_offs23	0000 0010
0x19	csc_offs3	0000 0000

CSC configuration example: HDTV YCbCr to HDTV RGB

- Gd = –0.4577*Cr + Yd – 0.1831*Cb +328 (= 0.6408*128*4)
- Bd = 0*Cr + Yd + 1.8142* Cb – 929 (= −1.8142*128*4)
- Rd = 1.5396* Cr +Yd +0*Cb – 788 (= −1.5396*128*4)

In a similar manner, it can be calculated that the programming array is in this case:

SUBADDRESS	REGISTER NAME	VALUE
0x04	csc_r11	1000 0001
0x05	csc_r12	1101 0101
0x06	csc_r21	0000 0000
0x07	csc_r22	0000 0000
0x08	csc_r31	0000 0110
0x09	csc_r32	0010 1001
0x0A	csc_g11	0000 0100
0x0B	csc_g12	0000 0000
0x0C	csc_g21	0000 0100
0x0D	csc_g22	1000 0000
0x0E	csc_g31	0000 0100
0x0F	csc_g32	0000 0000
0x10	csc_b11	1000 0000
0x11	csc_b12	1011 1011
0x12	csc_b21	0000 0111
0x13	csc_b22	0100 0010
0x14	csc_b31	0000 0000
0x15	csc_b32	0000 0000
0x16	csc_offs1	0001 0100
0x17	csc_offs12	1010 1110
0x18	csc_offs23	1000 1011
0x19	csc_offs3	0001 0100

4.5 Clip/Scale/Multiplier (CSM)

There are limits on the code range of the video data if sampled according to ITU or SMPTE standards. In other words, the full 10-bit range [0:1023] is not used to represent video pixels. For example, typically 64 decimal is the lowest code allowed to represent a video signal and corresponds to the blanking level. Similarly for Y, typically the maximum code is 940 decimal. Excursions outside this range can be the result of digital video processing.

THS8200 can handle such instantaneous excursions in either of two ways: by limiting the input codes to programmable max/min values, or by allowing such excursions to occur.

Depending on which approach is chosen, the user can scale up the video data in the CSM to make sure the full-scale dynamic range of the DAC is used for optimal performance when using limiting. Alternatively, the instantaneous excursions outside the code range can be output by the DAC in the analog output signal (allowing super-white/black in analog output) when this clipping is disabled.

The CSM block allows the user to specify the behavior of THS8200 with such reduced-swing input video codes. It consists of the following:

1. An optional clipping of the input video data at a high and low limit, where the limits are individually programmable per channel.
2. A downward shift of the input video data, where the shift amount is individually programmable per channel.
3. A multiply (magnitude scaling) function of the video data, where the multiplier coefficient is individually programmable per channel.

4.5.1 Clipping

Clipping (limiting) of the video input data can be turned on or off on a per-channel basis, and selectively at the high and/or low end, by programming the csm_<gy,rcr,bcb>_<high,low>_clip_on registers. The high/low clipping values can be programmed on a per-channel basis using registers csm_clip_<gy,rcr,bcb>_<high,low>.

Figure 4-5 shows a typical situation to clip ITU-R.BT601 sampled video signals.

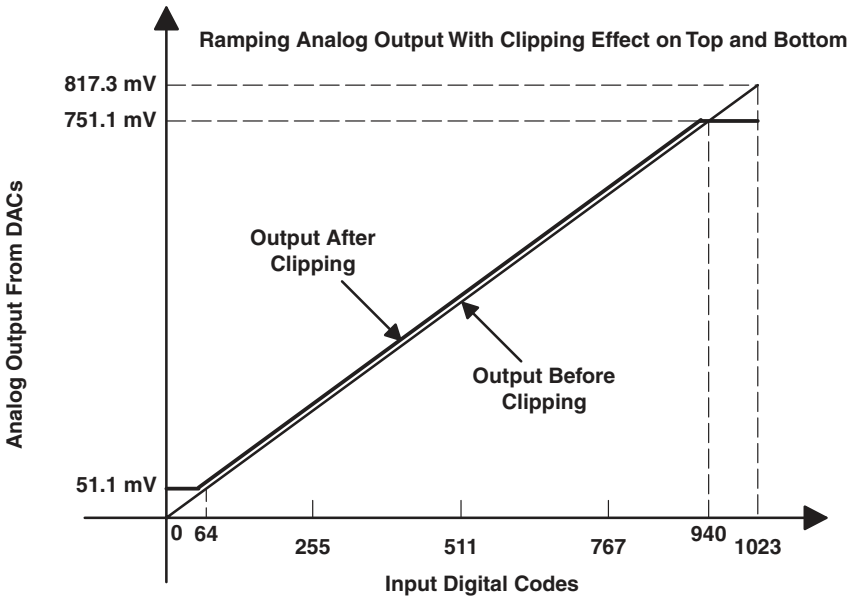


Figure 4-5. Effect of Clipping on Analog Output

4.5.2 Shifting

Next the video data can be shifted over a programmable amount downward. The number of codes over which to shift the input video data is set per channel by programming csm_shift_<gy,rcr,bcb>. Shifting of the input video data can be done downwards over 0..255 codes inside the CSM.

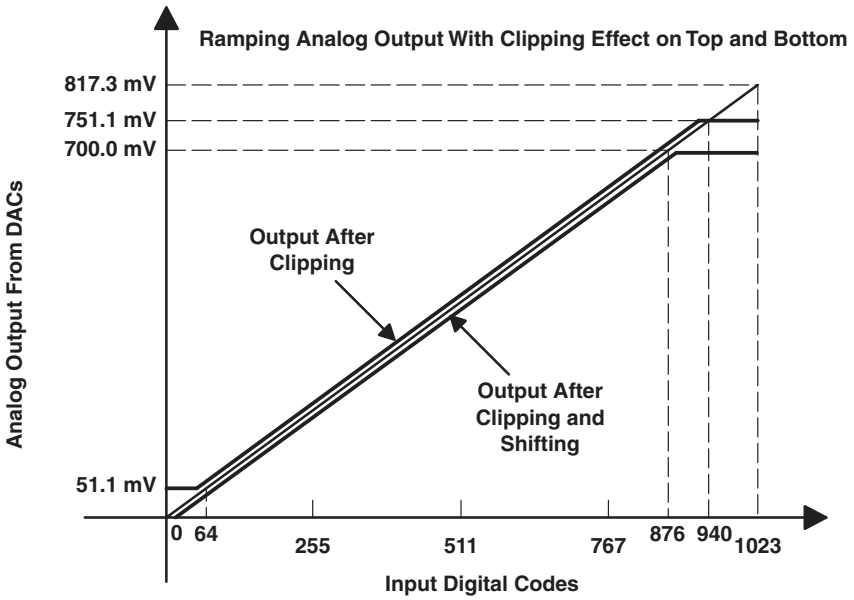


Figure 4-6. Effect of Shifting on Clipped Analog Output

Figure 4-5 and Figure 4-6 also show the analog output from the DAC if the full-scale video range over the [64..940] input would correspond to the normal 700-mV range for component video. This full-scale range is set by the selected FSADJ full-scale setting (register data_fsadj).

4.5.3 Multiplying

When the 10-bit range is not fully used for video, we can scale the input video data to use the full 10-bit dynamic range of the DACs. Care should be taken not to over/underflow the available range after scaling.

This multiplying control serves two purposes:

- Use of the full 10-bit DAC range for inputs of reduced range.
- Individual fine gain control per channel to compensate for gain errors and provide white balance control.

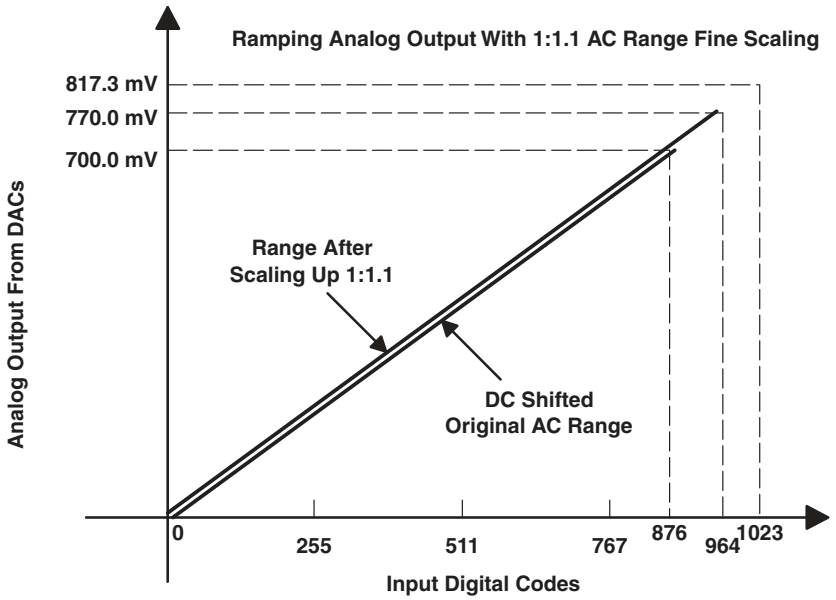


Figure 4-7. Effect of Scaling the Analog Video Output

Figure 4-7 illustrates a shifted analog ramping output. The multiplication factor could be calculated to scale this output range to the full 10-bit range of the DAC. Note that this scaling can be programmed individually per channel using registers csm_mult_<gy,rcr,bcb>. The range of the multiplication is 0..1.999, coded as a binary weighted 11-bit value, thus: csm_mult_<gy,rcr,bcb> = (Desired scale (0 to 1.999) / 1.999) × 2047.

Note that this approach allows to scale input code ranges that are different on each channel to an identical full-scale DAC output compliance, as is required for ITU-R.BT601 sampled signals where Y video data is represented in the range [64..940] and both Cb,Cr color difference channels are coded within the range [64..960]. All three channels need to generate a 700-mV nominal analog output compliance. Using a combination of FSADJ—adjusting the full-scale current of all DAC channels simultaneously in the analog domain—and digital CSM control, different trade-offs can be made for DAC output amplitude control, including channel matching.

As discussed in Display Timing Generator (Section 4.7), the user also controls the DAC output levels during blanking, negative and positive sync, pre- and post-equalization, and serration pulses. Using a combination of CSM and DTG programming, it is therefore possible to accommodate many video standards, including those that require a video blank-to-black level setup, as well as differing video/sync ratios (e.g., 10:4 or 7:3).

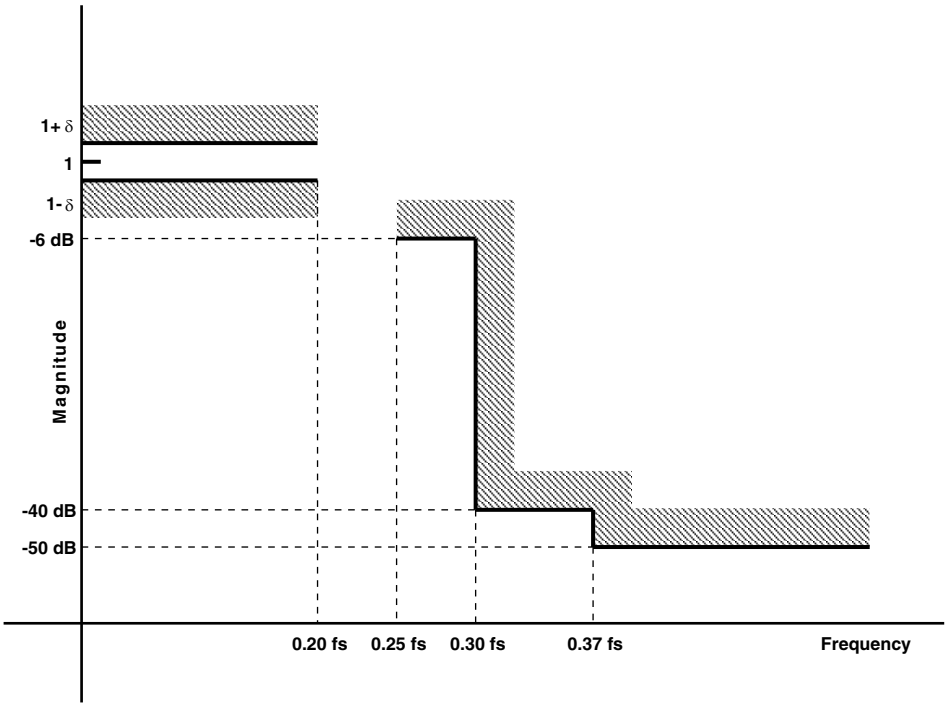
Finally, using the selectable full-scale adjustment from the FSADJ1 or FSADJ2 terminals, it is possible to switch between two analog output compliance settings with no hardware changes.

Physically, the CSM output is represented internally as an 11-bit value to improve the DAC linearity at the 10-bit level after scaling. Each DAC internally is of 11-bit resolution.

4.6 Interpolating Finite Impulse Response Filter (IFIR)

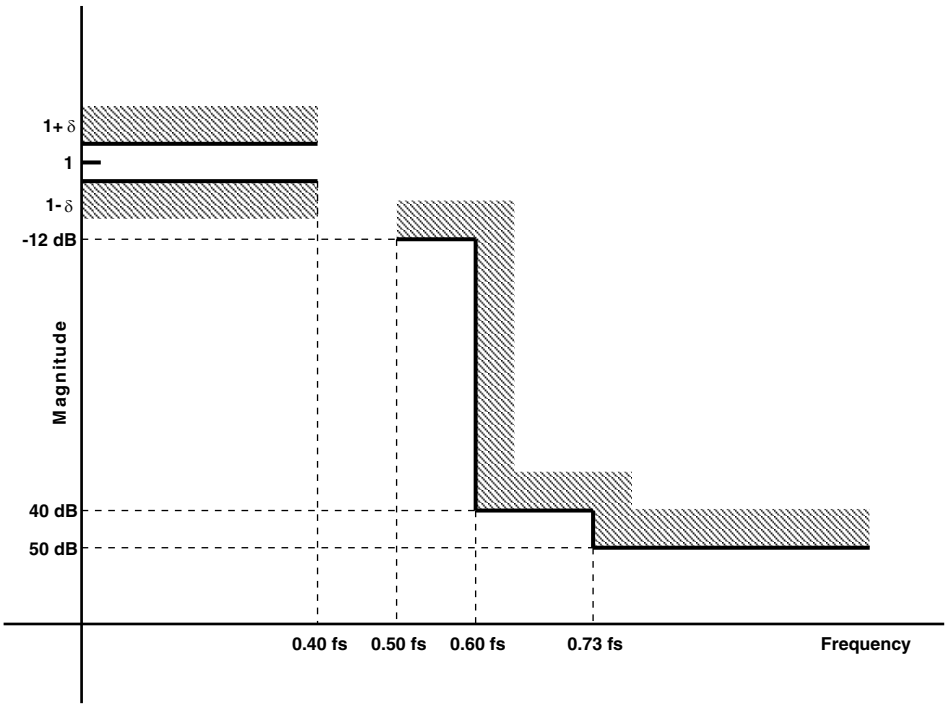
For relaxing the requirements of the reconstruction filter behind the DAC in the analog domain, and in order to take advantage of the high-speed capability of the DACs in THS8200, a 2× digital up-sampling and interpolation filter module is integrated.

Figure 4-8 through Figure 4-11 show the YRGB and CbCr filtering requirements for HDTV (SMPTE274M/296M standards) and SDTV (ITU-R.BT601 standard), respectively.



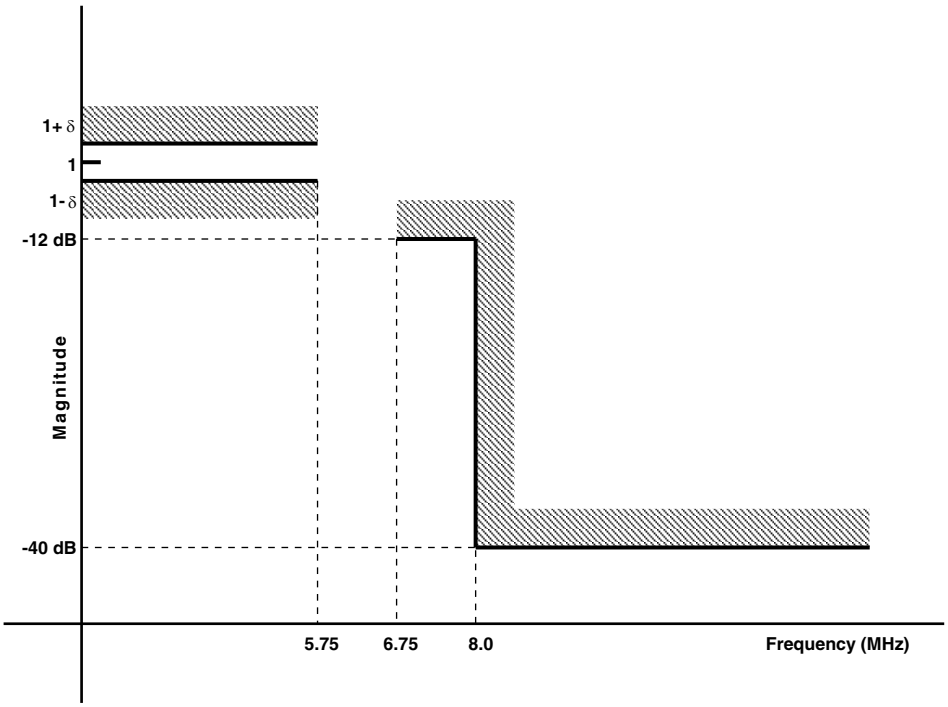
NOTE: δ = 0.05 dB. fs=74.25 MSPS for 1080I and 720P HDTV formats.

Figure 4-8. P_B and P_R Filter Requirements Based on SMPTE 296M/274M



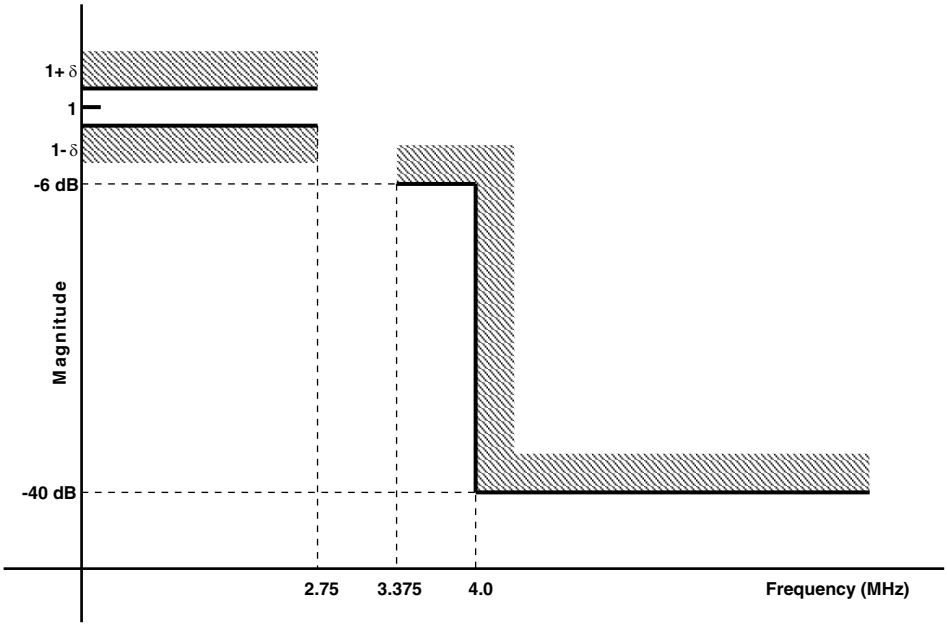
NOTE: δ = 0.05 dB. fs=74.25 MSPS for 1080I and 720P HDTV formats.

Figure 4-9. Y and RGB Filter Requirements Based on SMPTE 296M/274M



NOTE: δ = 0.05 dB

Figure 4-10. Y and RGB Filter Requirements Based on ITU-R.BT601



NOTE: δ = 0.05 dB

Figure 4-11. Cb and Cr Filter Requirements Based on ITU-R.BT601

Figure 4-12 through Figure 4-14 illustrate the frequency and phase responses of the interpolating filters. The actual response using the finite-word length coefficients present in THS8200 is shown. The same filter characteristic is used for SDTV/HDTV modes and for both 4:2:2 to 4:4:4 interpolation (2 filters, one on each of Cb and Cr channels, switched in when a 4:2:2 input mode is selected on DMAN to interpolate chrominance from 1/2 to 1× pixel clock rate) as well as for 2× video oversampling (3 filters, one on each DAC channel, switched in when 2× interpolation is activated).

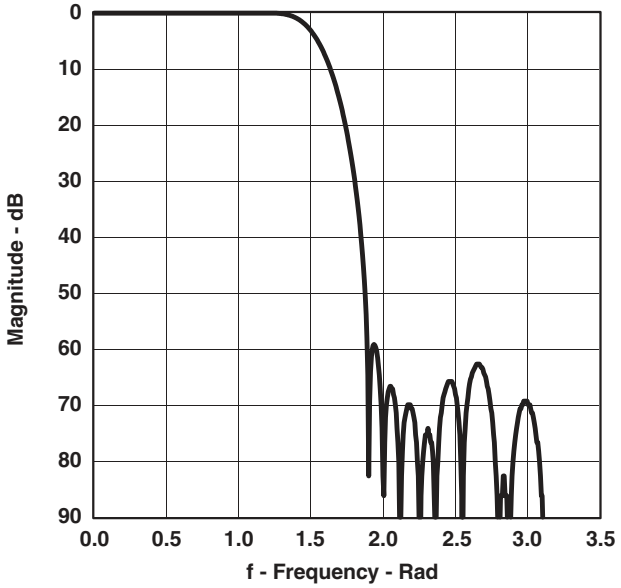


Figure 4-12. IFIR Frequency Response

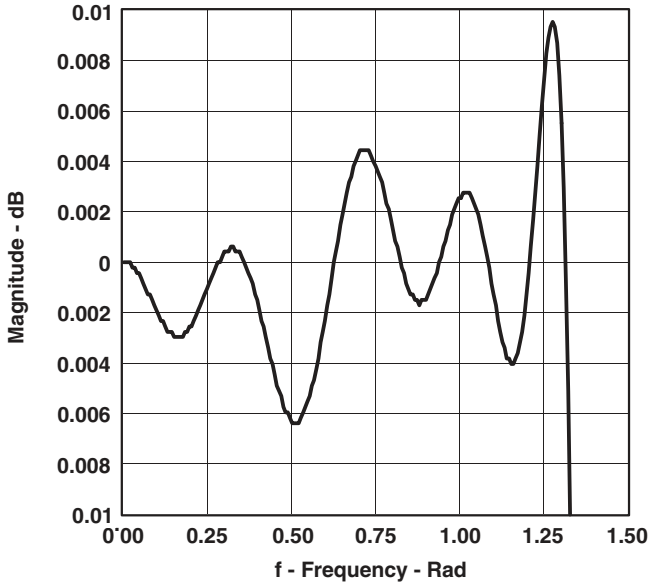


Figure 4-13. IFIR Pass-Band Frequency Response

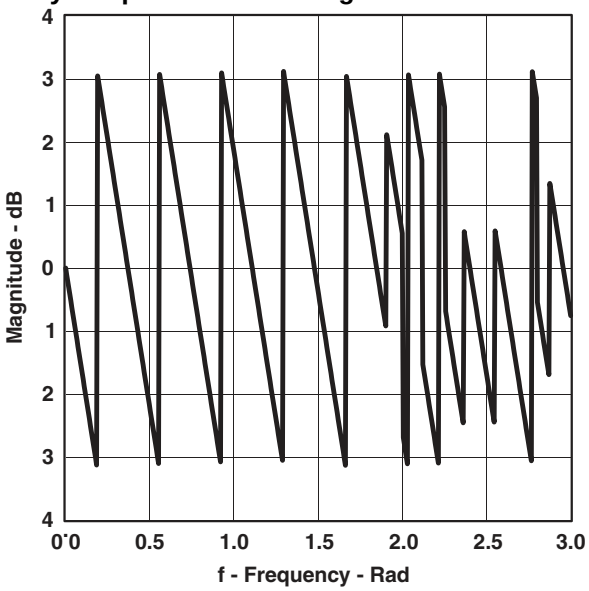


Figure 4-14. IFIR Phase Response

Each of the two interpolation stages can be switched in or bypassed:

- Register data_ifir12_bypass controls the 4:2:2 to 4:4:4 filter bank (these filters should be set active when a 4:2:2 input mode is selected on DMAN).
- Register data_ifir35_bypass controls the 1× to 2× interpolation stage and can be set active for optional 2× interpolation when an input format with pixel clock < 80 MSPS is present.

4.7 Display Timing Generator (DTG)

4.7.1 Overview of Functionality

THS8200 can generate dedicated Hsync/Vsync/FieldID video synchronization outputs, as well as a composite sync inserted on either the G/Y or all analog output channels. Both types of output synchronization can be available simultaneously and programmed independently. Synchronization patterns are fully programmable to accommodate all standard VESA (PC graphics) and ATSC (DTV) formats as well as nonstandard formats.

For the purpose of output video timing generation, the device is configured in HDTV, SDTV or VESA mode (dtg1_mode register). Depending on the selected DTG mode, a number of line types are available to generate the full video frame format. The timing and position of horizontal and vertical syncs, the position of horizontal and vertical blanking intervals, and the structure, position and width of equalization pulses, pre- and post-serration pulses within the vertical blanking interval are user-programmable.

The DTG determines:

- the frame format/field format (number of pixels/line, number of lines/field1, number of lines/field2, number of fields/frame = 1 for progressive or 2 for interlaced formats) and its synchronization to the input data source.
  - Registers: dtg1_total_pixels, dtg1_linecnt, dtg1_frame_size, dtg1_field_size
- in slave mode, whether HS_IN, VS_IN, FID (dedicated sync inputs) are used for input video synchronization or video timing is extracted from embedded SAV/EAV codes, as well as the relative position of the video frame with respect to these synchronization signals.
  - Registers: dtg2_embedded_timing, dtg2_hs_in_dly, dtg2_vs_in_dly
- the I/O direction of the HS_IN and VS_IN input signals (master vs slave mode), and the polarity of the HS_IN, VS_IN, and FID signals.
  - Registers: dtg2_hs_pol, dtg2_vs_pol, dtg2_fid_pol
- the position and width of the HS_OUT, VS_OUT output signals, and their polarity.
  - Registers: dtg2_hlength, dtg2_hdly, dtg2_vlength1, dtg2_vdly1, dtg2_vlength2, dtg2_vdly2, dtg2_vsout_pol, dtg2_hsout_pol
- field reversal within DTG.
  - Register: dtg1_field_flip
- the active video window: width and position of horizontal blanking interval, width and position of vertical blanking interval.
  - Registers: dtg2_bp<n>, dtg2_linetype<n> and the dtg1_spec_x registers, see DTG Line Type Overview (Section 4.7.3).
- the composite sync format: horizontal line timing includes serration, interlaced sync and broad pulses on each line in vertical blanking interval, width of vertical sync.
  - Registers: dtg1_mode, dtg1_spec_<a,b,c,d,d1,e,g,h,i,k,k1>
- the behavior of the composite sync insertion: inserted on G/Y-channel only, or inserted on all channels, or no composite sync insertion; the amplitudes of the inserted negative and positive sync, the amplitudes of all serration pulses and broad pulses during the vertical blanking interval.
  - Registers: dtg1_<y,cbcr>_sync_high, dtg1_<y,cbcr>_sync_low
- the DAC output amplitude during blanking and whether video data is passed or not during the active video portion of lines within the vertical blanking interval that contain no vertical sync, serration, or broad pulses.
  - Registers: dtg1_<y,cbcr>_blank, dtg1_pass_through
- the width of each color bar of the color bar test pattern.
  - Registers: dtg1_vesa_cbar_size

4.7.2 Functional Description

The user should program the DTG with the correct parameters for the current video format. The DTG contains a line and a pixel counter, and a state machine to determine which user−defined line waveform to output for each line on the analog outputs. The pixel counter counts horizontally up to the total number of pixels per line, programmed in 'dtg1_total_pixels'. The line counter counts up to 'dtg1_field_size' lines in the first field, and continues its count up to 'dtg1_frame_size' lines in the total frame (field1+field2).

The current field is derived from the even/odd field ID signal, which is sampled at the start of the Vsync period. The source for the internal FID signal can be either the signal to the FID terminal, or can be internally derived from relative Hsync/Vsync alignment on the corresponding terminals, as selected by 'dtg2_fid_de_cntl' and the current DTG mode (VESA vs. SDTV/HDTV). See register map description of 'dtg2_fid_de_cntl' for more details. Derivation of FID from Hsync/Vsync input alignment is done according to the EIA−861 specification. There is a tolerance implemented on Hsync/Vsync transition misalignment. When the active edge of the Vsync transition occurs within ±63 clock cycles from the active edge of Hsync, both signals are interpreted as aligned, which signals field 1. Because of this timing window, the internal FieldID signal is generated later than the start of Vsync period. Since the signal is internally sampled at the start of the Vsync period to determine the current field, the field interpretation is opposite. Use the 'field_flip' register to correct this through field reversal.

If the video format is progressive, only field1 exists and no FID signal is needed. However the DTG will only startup when a field 1 condition is detected i.e when FID is detected low at the start of the Vsync period. Thus in the case of a progressive video format, and when using the device with external FID input, the user must make sure to keep the FID terminal low.

It is also needed for proper DTG synchronization that the programmed Hsync and Vsync input polarities are correct. Since Hsync, Vsync polarities change for different VESA PC formats, the device has built−in support to detect the incoming sync polarities. This is done by comparing the width of Hsync high ('misc_ppl') to the total line length ('dtg2_pixel_cnt') to derive the Hsync duty cycle and thus its polarity. Upon this detection, the user can program the detected incoming polarity for DTG input synchronization ('dtg2_hs_pol') – it is not set automatically by the device. The procedure is similar for Vsync polarity detection, using registers 'misc_lpf', 'dtg2_line_cnt' and 'dtg2_vs_pol'.

The DTG synchronization can be separated into three functions:

- **Internal synchronization**: How the DTG is synchronized with respect to the internal horizontal and vertical counters.
- **Source synchronization**: How the horizontal and vertical counters are synchronized to the HS_IN/VS_IN/FID or SAV/EAV signals.
- **Output synchronization**: how the output timings HS_OUT, VS_OUT, and the composite sync output are synchronized to the DTG and the horizontal and vertical counters.

The DTG is based on a state machine that can generate a set of line types which can override the values on the DAC inputs. The DTG output is multiplexed into the data path by the DIGMUX. The selected video format preset setting, or the programmed (line type, breakpoint) table in case a generic mode is selected in dtg1_mode, determines which line type is generated for a particular line, and where this DTG output is used to override the normal DAC inputs. Internally, a fixed preconfigured number of line types exists from which the user can select.

Also, for each set of line types (we will see next there are two different sets of line types possible) the user can program the horizontal duration of each predefined excursion (negative sync, positive sync, back porch, front porch, broad pulse, interlaced sync, etc.) and also the amplitude (e.g., negative sync amplitude, positive sync amplitude, blank amplitude).

The setting of dtg1_mode determines:

- **Internal synchronization**: The 0H reference (horizontal reset of the DTG) is different between SDTV and HDTV.

- **Output synchronization**: The available set of output synchronization line types depends on these modes. The user can choose from a number of predefined line types for each mode. In each mode, the user is able to program the timings along the line. However some timings are hard coded by the selected DTG_mode (e.g., rise/fall times for sync are different; see DTG Line Type Overview, Section 4.7.3) and not all line types can be selected in each DTG mode (e.g., HDTV allows tri-level sync, while SDTV only allows generation of bi-level negative syncs).

4.7.2.1 Predefined DTG Video Formats (Presets)

While the DTG has the flexibility to generate a wide array of video output formats and their synchronization signals, the most common video formats have predefined settings for the field and frame sizes and for (line type, breakpoint) settings.

When selecting a video format preset, the horizontal timings of the line types still need to be programmed. The preset only fixes the (line type, breakpoint) table.

4.7.2.2 Internal Synchronization

The pixel and line counters of the DTG are reset by internal signals. In slave mode (THS8200 slaves to external video input source) these signals are derived from either the embedded SAV/EAV codes or the dedicated Hsync/Vsync/FID inputs. In master mode, these counters are in free-run and the HS_IN/VS_IN signals are generated by the THS8200 based on the programmed field/frame parameters. Master mode is only available for progressive-scan VESA modes. FID is not generated in master mode.

The user can delay, in both horizontal and vertical directions, the 0-reference of the DTG by programming the input delay registers. Physically, the horizontal and vertical DTG startup values are altered. The effect is that, when a vertical or horizontal sync is received, either from dedicated inputs or from embedded SAV/EAV codes, the output frame starts at position (x,y). This ensures that, for example, the output video frame can be centered on the display.

Based on the 0-reference of the DTG, the line types are generated and the DIGMUX will select between the video input and the DTG output for each line type. All horizontal timings of the different line types are programmable, including the portion of the video line seen as active video. A complete overview of all available line types in either SDTV or HDTV mode is presented in Section 4.7.3.

Additionally, Hsync/Vsync outputs can be generated, synchronized to the THS8200 DAC outputs. These outputs are programmable in width, position and polarity, based on the horizontal/vertical pixel counters, and thus independently of the DTG reference. This ensures that independent synchronization is possible between the composite sync output inserted into the DAC output(s) and the dedicated Hsync/Vsync outputs. Because of their programmability, these output signals could be used for other purposes as well; e.g., Vsync could be programmed as a signal active during the VBI.

Figure 4-15 shows how the internal pixel and line counters are synchronized to internal HS and VS signals in slave mode. HS and VS are internal signals derived from either HS_IN, VS_IN, or from embedded SAV/EAV codes in the input video data. Since the 0-reference of the DTG is determined by these counters, the dtg2_vs_in_dly and dtg2_hs_in_dly register settings influence both HS_OUT, VS_OUT and composite sync output timing. The dtg2_vdly<1,2> and dtg2_hdly settings, on the other hand, only affect HS_OUT and VS_OUT, because they are downstream of the pixel counter. Likewise, dtg2_hlength and dtg2_vlength<1,2> only affect these dedicated sync output signals.

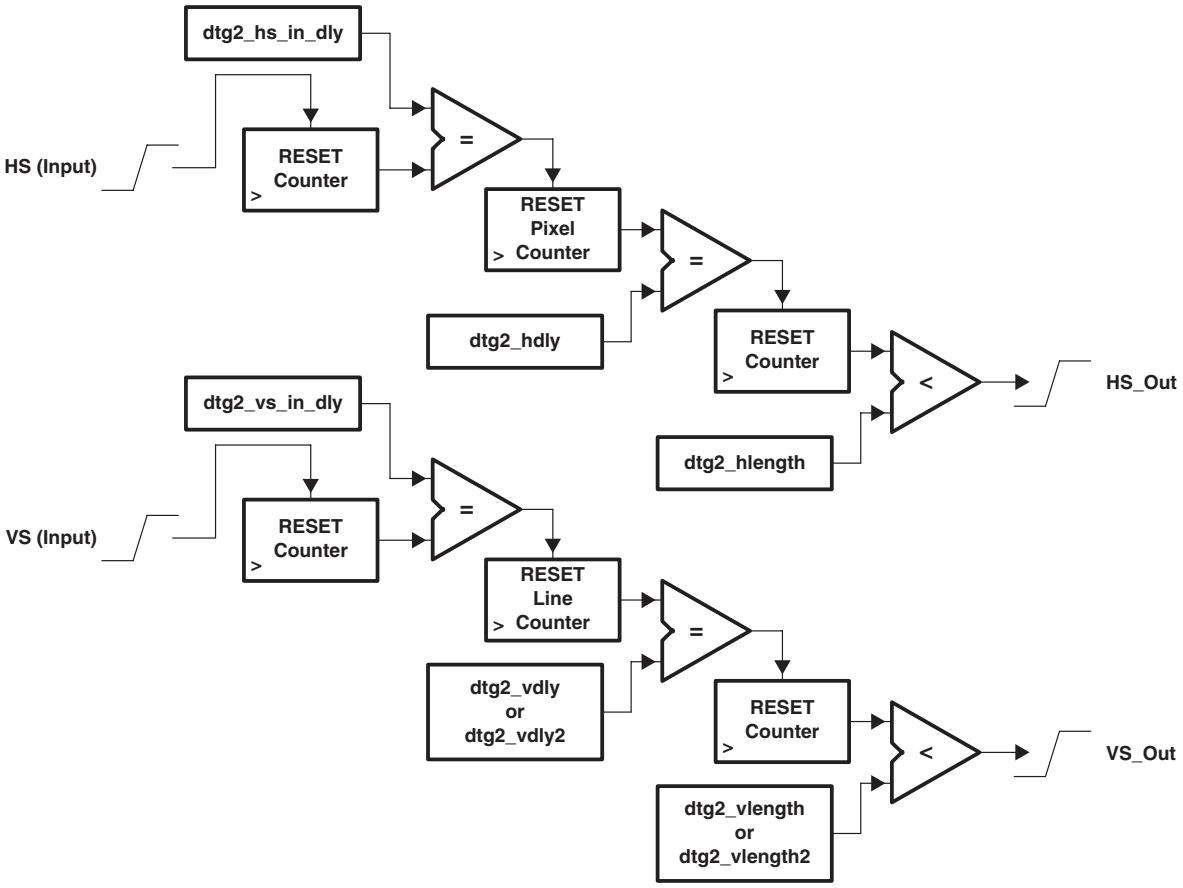


Figure 4-15. THS8200 DTG VS/HS Output Generation

Note that both independent sets of delay registers allow accommodation of different input timing references in slave mode. When the device is configured in master mode, the delay registers can compensate for different external (frame memory) synchronization requirements.

4.7.2.3 Output Synchronization: Composite Sync

The composite sync is generated from a programmed sequence of (line type, breakpoint) combinations, either user-programmed (in generic mode) or preset (in preset mode). The line type determines the waveform shape at the output of the DAC(s) with programmable amplitudes and timings.

On each line, at the horizontal reference point of the DTG, the DTG decides where to start/stop the DTG-generated data and where to pass input video data. For example, during an active video line, ancillary data can be embedded in the digital stream outside the active video portion of the line, that we might want to convert to analog. Alternatively, during a nonactive video line, where normally the predefined line type would be inserted, ancillary data might need to be passed during the active video portion of the line.

The amplitudes of positive, negative sync excursions and of the negative serration, pre- and post-equalization and broad pulses are independently programmable between G/Y and BPb, RPr channels. Therefore sync insertion can be programmed on only the G/Y output or on all DAC outputs.

In order to limit the number of selection bits to select the line type, and because of the fact that we can define a set of line types that is mutually exclusive for SDTV and HDTV video modes, there are two DTG video modes: SDTV and HDTV. There is a third DTG mode (VESA) which does not use the line type/breakpoint state machine and only generates Hsync/Vsync outputs.

4.7.2.4 Output Synchronization: Hsync/Vsync Outputs

These are the HS_OUT and VS_OUT signals, of which the width, position and polarity are programmable in all DTG modes.

4.7.3 DTG Line Type Overview

4.7.3.1 HDTV Mode

When an HDTV mode is selected in dtg1_mode (preset or generic), a tri-level sync is inserted on the analog output at the start of every video line. The amplitudes during negative and positive excursions are programmable, as well as the horizontal timing parameters (width, position) of both excursions.

The transition time for negative-to-blank and blank-to-positive excursions during VBI is fixed to 2T, generating a tri-level sync negative-to-positive excursion of 4T. The line type is programmed in registers dtg2_linetype<n> and is output by the DTG from the vertical field/frame position corresponding to the line number programmed in register dtg2_breakpoint<n>, until the line number listed in the next breakpoint register is reached. An example for 1080I is shown in Figure 4-25.

The DTG overrides the input video data except where specified below for the specific line types.

The horizontal timings shown in Figure 4-16 and Figure 4-17 correspond to the dtg1_spec_<x> registers. Note that the f spec is fixed.

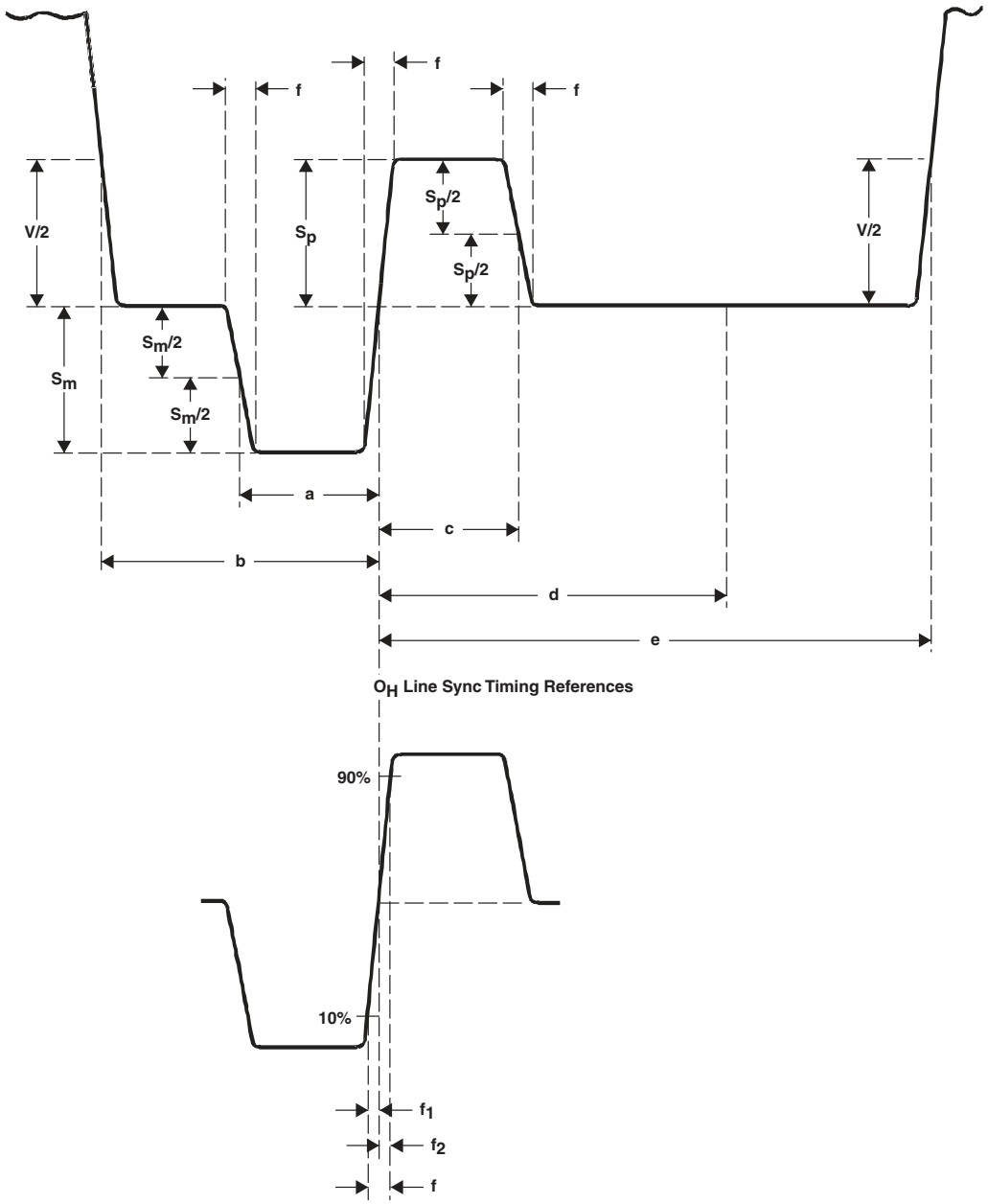


Figure 4-16. Tri-Level Line-Synchronizing Signal Waveform

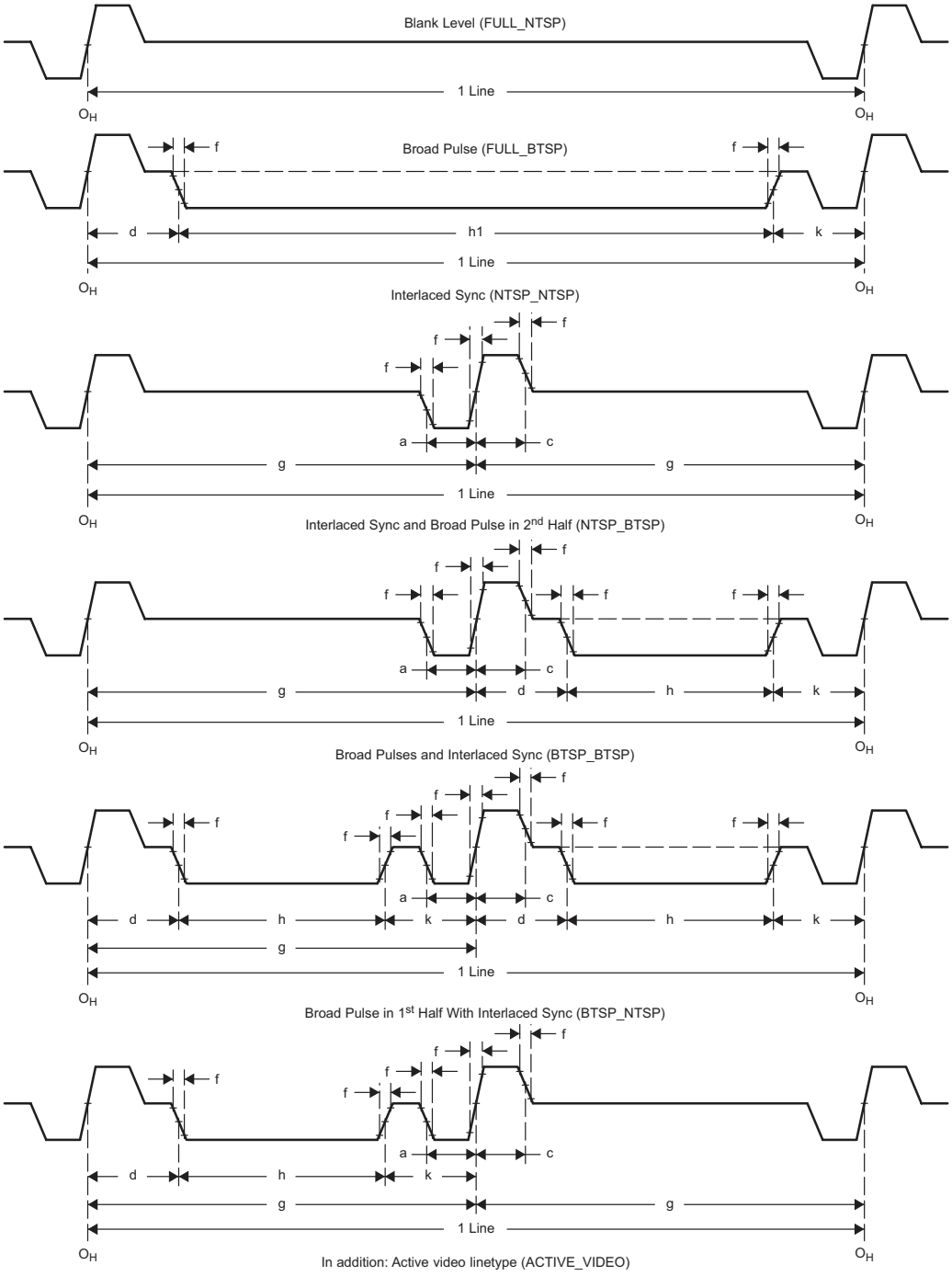
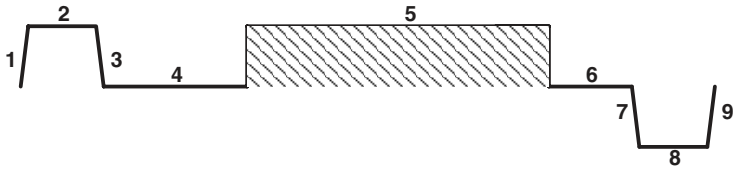


Figure 4-17. THS8200 VBI Line Types in HDTV Mode

4.7.3.2 Active Video

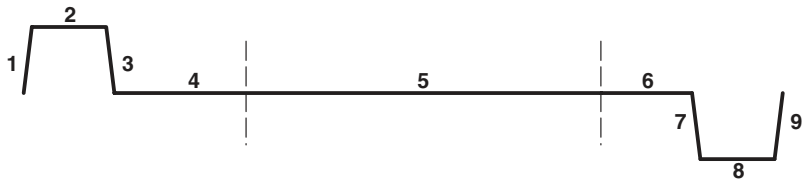


STATE	DURATION
1	Fixed at 2T
2	dtg1_spec_c-4
3	Fixed at 4T
4	dtg1_spec_e dtg1_spec_c-2
5	dtg1_total_pixels dtg1_spec_e dtg1_spec_b
6	dtg1_spec_b dtg1_spec_a-2
7	Fixed at 4T
8	dtg1_spec_a-4
9	Fixed at 2T

Figure 4-18. HDTV Line Type ACTIVE_VIDEO

4.7.3.3 FULL NTSP (Full Normal Tri-Level Sync Pulse)

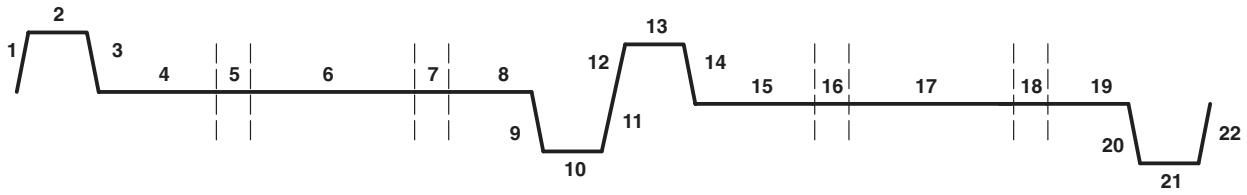
Device input data is passed during state #5 if dtg1_pass_through is on.



STATE	DURATION
1	Fixed at 2T
2	dtg1_spec_c-4
3	Fixed at 4T
4	dtg1_spec_e dtg1_spec_c-2
5	dtg1_total_pixels dtg1_spec_e dtg1_spec_b
6	dtg1_spec_b dtg1_spec_a-2
7	Fixed at 4T
8	dtg1_spec_a-4
9	Fixed at 2T

Figure 4-19. HDTV Line Type FULL_NSTP

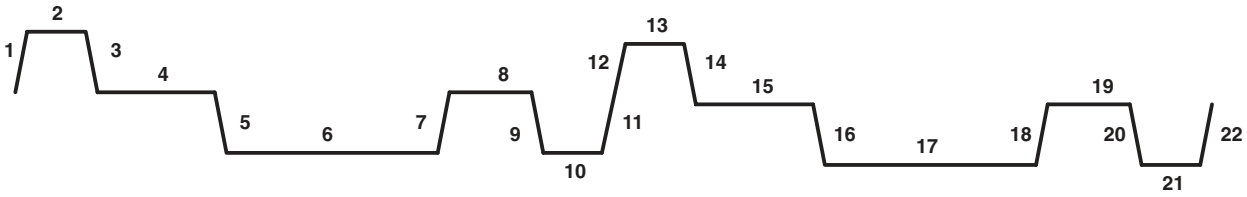
4.7.3.4 NTSP NTSP (Normal Tri-Level Sync Pulse/Normal Tri-Level Sync Pulse)



STATE	DURATION
1/12	Fixed at 2T
2/13	dtg1_spec_c-4
3/14	Fixed at 4T
4/15	dtg1_spec_d_lsb dtg1_spec_c-4
5/16	Fixed at 4T
6/17	dtg1_total_pixels/2 dtg1_spec_k dtg1_spec_d-4
7/18	Fixed at 4T
8/19	dtg1_spec_k—dtg1_spec_a-12
9/20	Fixed at 4T
10/21	dtg1_spec_a-4
11/22	Fixed at 2T

Figure 4-20. HDTV Line Type NTSP_NTSP

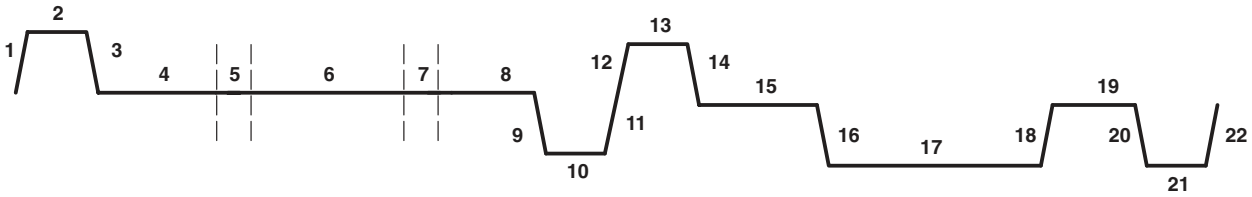
4.7.3.5 BTSP BTSP (Broad Pulse and Tri-Level Sync Pulse/Broad Pulse and Tri-Level Sync Pulse)



STATE	DURATION
1/12	Fixed at 2T
2/13	dtg1_spec_c-4
3/14	Fixed at 4T
4/15	dtg1_spec_d_lsb dtg1_spec_c-4
5/16	Fixed at 4T
6/17	dtg1_total_pixels/2 dtg1_spec_k dtg1_spec_d-4
7/18	Fixed at 4T
8/19	dtg1_spec_k dtg1_spec_a-12
9/20	Fixed at 4T
10/21	dtg1_spec_a-4
11/22	Fixed at 2T

Figure 4-21. HDTV Line Type BTSP_BTSP

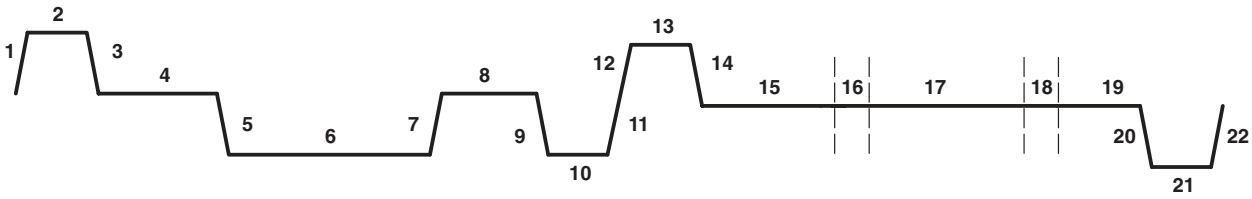
4.7.3.6 NTSP BTSP (Normal Tri-Level Sync Pulse/ Broad Pulse and Tri-Level Sync Pulse)



STATE	DURATION
1/12	Fixed at 2T
2/13	dtg1_spec_c-4
3/14	Fixed at 4T
4/15	dtg1_spec_d dtg1_spec_c-4
5/16	Fixed at 4T
6/17	dtg1_total_pixels/2 dtg1_spec_k dtg1_spec_d-4
7/18	Fixed at 4T
8/19	dtg1_spec_k dtg1_spec_a-12
9/20	Fixed at 4T
10/21	dtg1_spec_a-4
11/22	Fixed at 2T

Figure 4-22. HDTV Line Type NTSP_BTSP

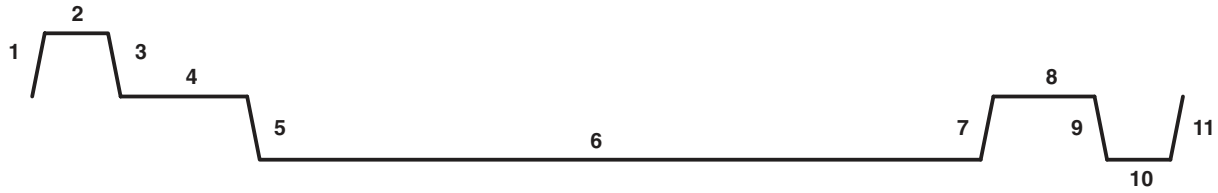
4.7.3.7 BTSP NTSP (Broad Pulse and Tri-Level Sync Pulse/Normal Tri-Level Sync Pulse)



STATE	DURATION
1/12	Fixed at 2T
2/13	dtg1_spec_c-4
3/14	Fixed at 4T
4/15	dtg1_spec_d dtg1_spec_c-4
5/16	Fixed at 4T
6/17	dtg1_total_pixels/2 dtg1_spec_k dtg1_spec_d-4
7/18	Fixed at 4T
8/19	dtg1_spec_k dtg1_spec_a-12
9/20	Fixed at 4T
10/21	dtg1_spec_a-4
11/22	Fixed at 2T

Figure 4-23. HDTV Line Type BTSP_NTSP

4.7.3.8 Full BTSP (Full Broad Pulse and Tri-Level Sync Pulse)



STATE	DURATION
1/12	Fixed at 2T
2/13	dtg1_spec_c-4
3/14	Fixed at 4T
4/15	dtg1_spec_d dtg1_spec_c-4
5/16	Fixed at 4T
6/17	dtg1_total_pixels/2 dtg1_spec_k dtg1_spec_d-4
7/18	Fixed at 4T
8/19	dtg1_spec_k dtg1_spec_a-12
9/20	Fixed at 4T
10/21	dtg1_spec_a-4
11/22	Fixed at 2T

Figure 4-24. HDTV Line Type FULL_BTSP

Example: 1080I/P

THS8200 is put into 1080I mode by programming dtg1_mode = 0001. Figure 4-25 shows the required output format of both fields for 1080I and 1080P.

When in 1080I preset mode, the (line type, breakpoint) table and frame and field size registers are filled out as follows internally:

Breakpoints	Line Type
6	BTSP_BTSP
7	NTSP_NTSP
21	FULL_NTSP
561	ACTIVE_VIDEO
563	FULL_NTSP
564	NTSP_BTSP
568	BTSP_BTSP
569	BTSP_NTSP
584	FULL_NTSP
1124	ACTIVE_VIDEO
1126	FULL_NTSP

frame_size = 10001100101; 1125d

field_size = 01000110011; 563d

From line 1 to 5, line type BTSP_BTSP is generated. When the line counter reaches line 6, the DTG switches to line type NTSP_NTSP, etc. Note that the dtg1_spec_<x> registers need to be filled out with the correct values to set the horizontal line timings.

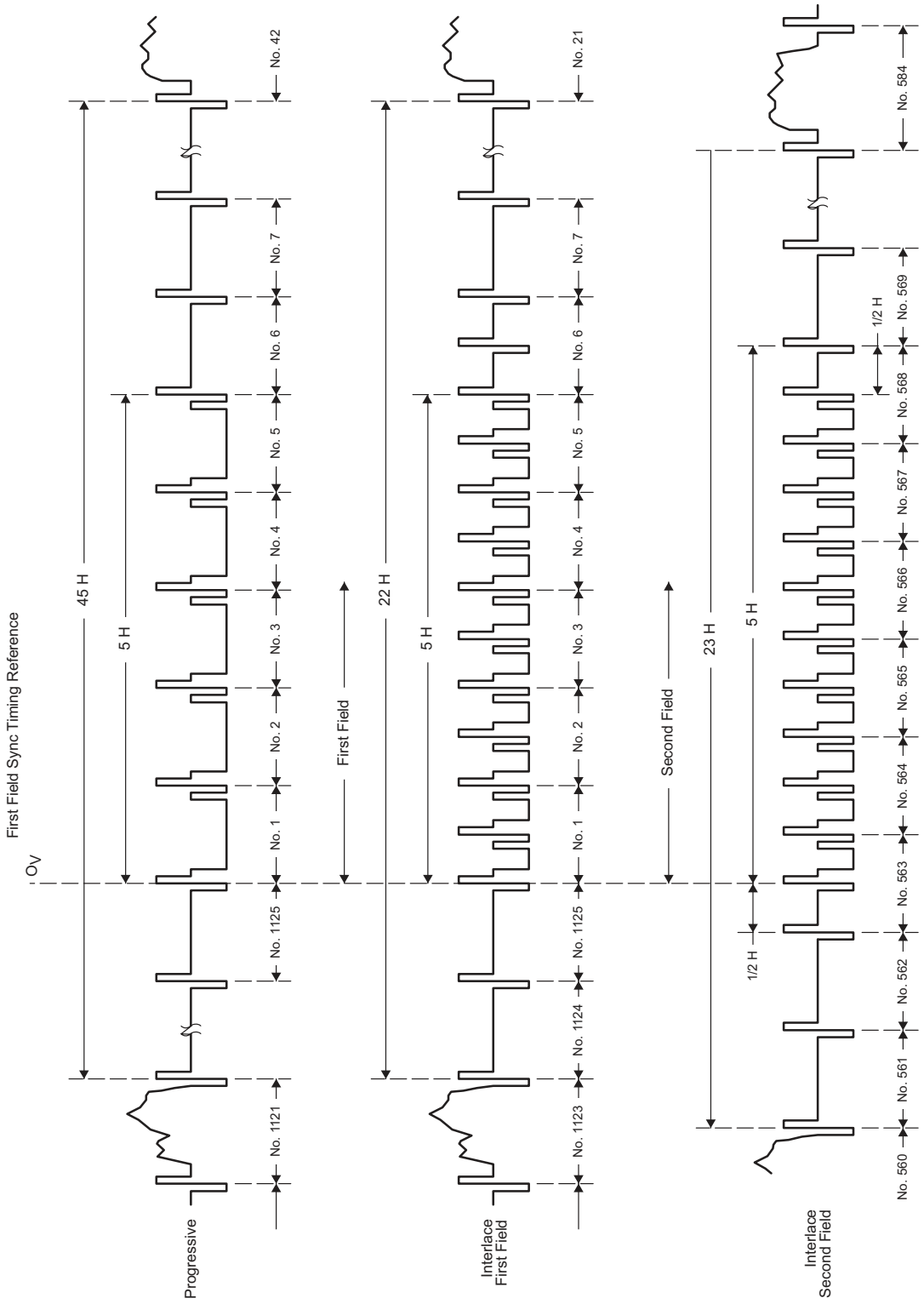


Figure 4-25. Field/Frame Synchronizing Signal Waveform (1080I and 1080P Formats)

4.7.3.9 SDTV Mode

In SDTV mode, the start of a video line is signaled by the leading edge of a negative-going bi-level sync.

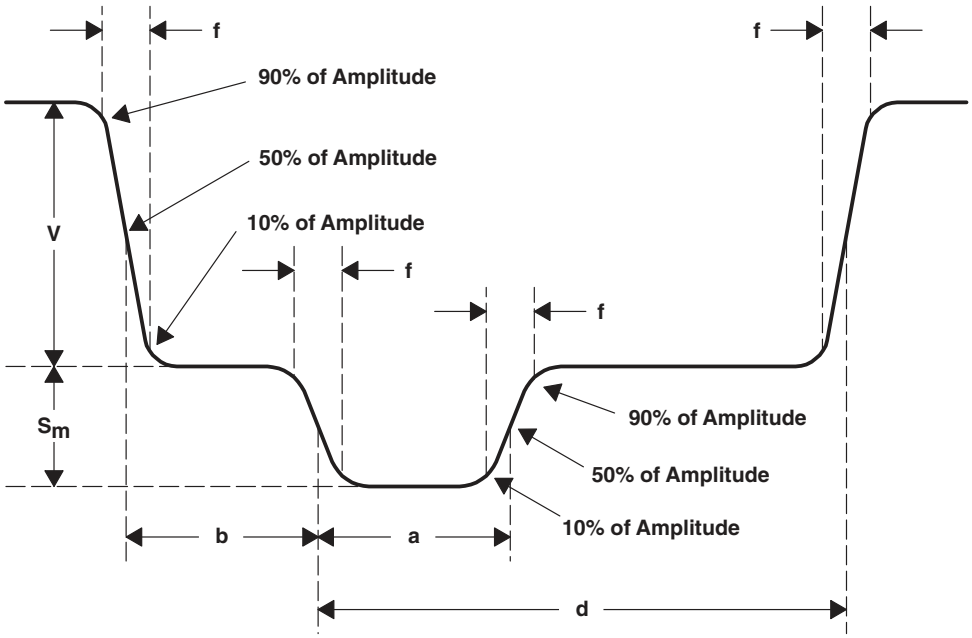
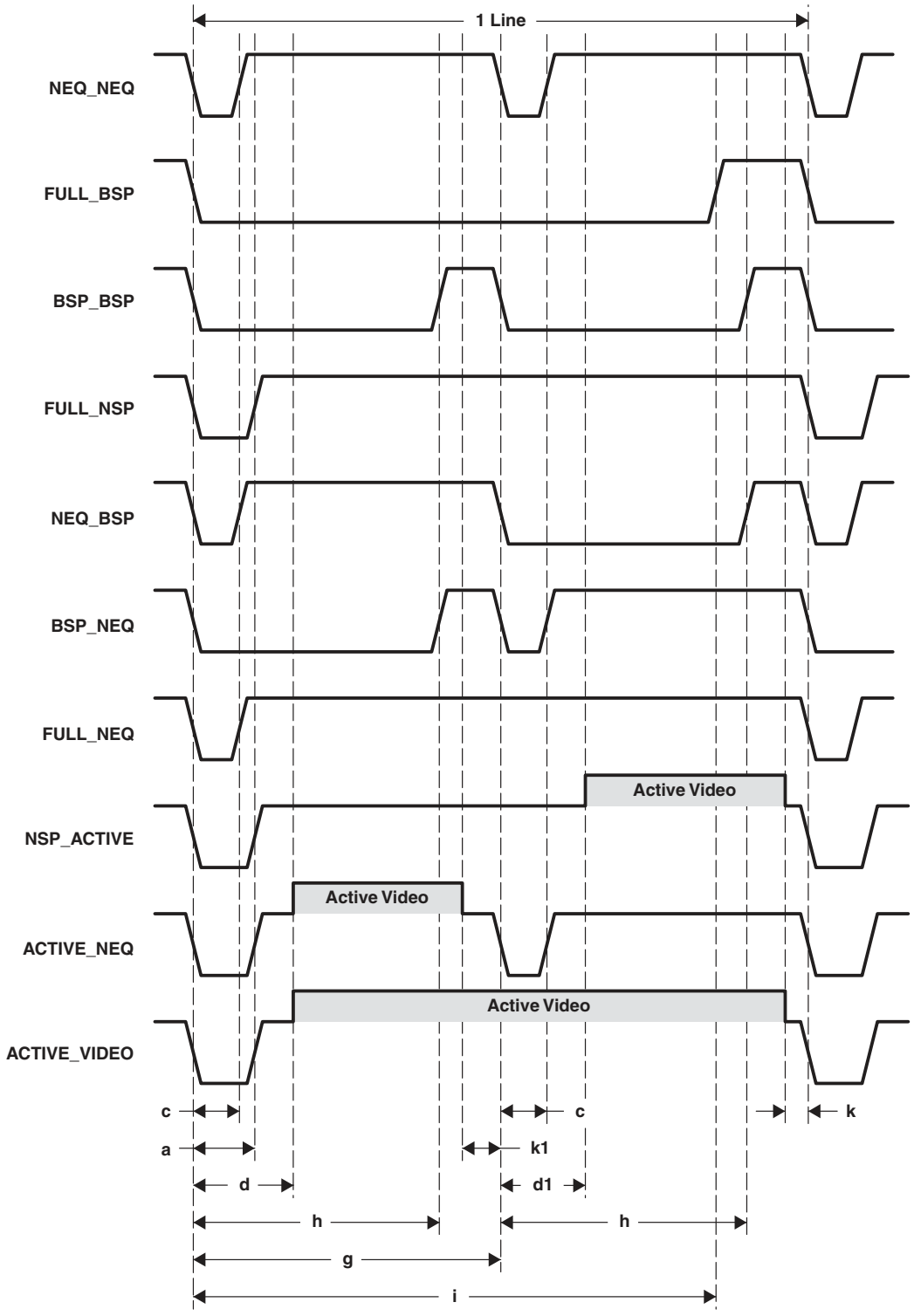


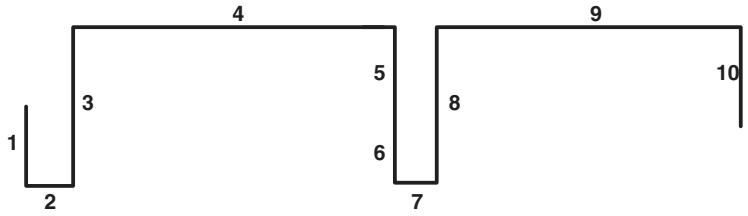
Figure 4-26. Horizontal Synchronization Signal Waveform



NOTE: All Rise/Fall times are equal to f = 2T

Figure 4-27. THS8200 VBI Line Types in SDTV Mode

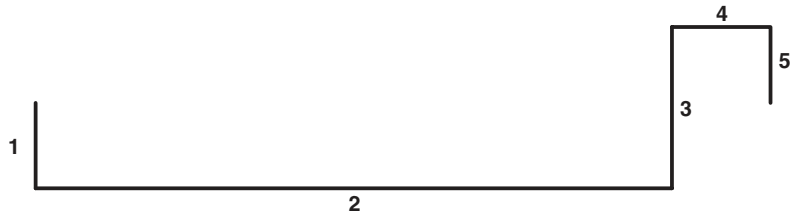
4.7.3.10 NEQ_NEQ (Negative Equalization Pulse/Negative Equalization Pulse)



STATE	DURATION
1	Fixed at 1T
2	dtg1_spec_c
3	Fixed at 2T
4	dtg1_spec_g dtg1_spec_c-4
5	Fixed at 1T
6	Fixed at 1T
7	dtg1_spec_c
8	Fixed at 2T
9	dtg1_spec_g dtg1_spec_c-4
10	Fixed at 1T

Figure 4-28. SDTV Line Type NEQ_NEQ

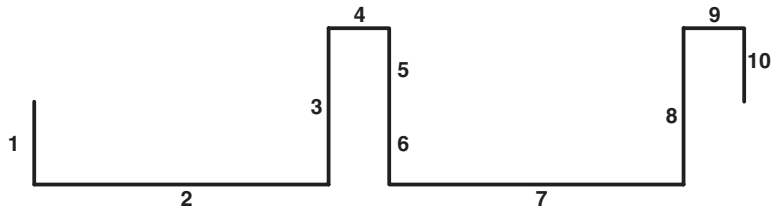
4.7.3.11 FULL_BSP (Full Broad Sync Pulse)



STATE	DURATION
1	Fixed at 1T
2	dtg1_spec_i
3	Fixed at 2T
4	dtg1_total_pixels dtg1_spec_i-4
5	Fixed at 1T

Figure 4-29. SDTV Line Type FULL_BSP

4.7.3.12 BSP_BSP (Broad Sync Pulse/Broad Sync Pulse)

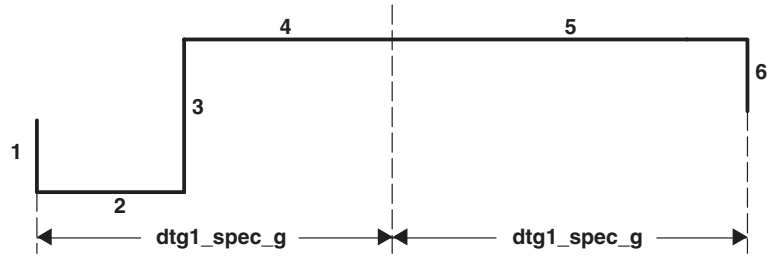


STATE	DURATION
1	Fixed at 1T
2	dtg1_spec_h
3	Fixed at 2T
4	dtg1_spec_g dtg1_spec_h-4
5	Fixed at 1T
6	Fixed at 1T
7	dtg1_spec_h
8	Fixed at 2T
9	dtg1_spec_g dtg1_spec_h-4
10	Fixed at 1T

Figure 4-30. SDTV Line Type BSP_BSP

4.7.3.13 FULL_NSP (Full Normal Sync Pulse)

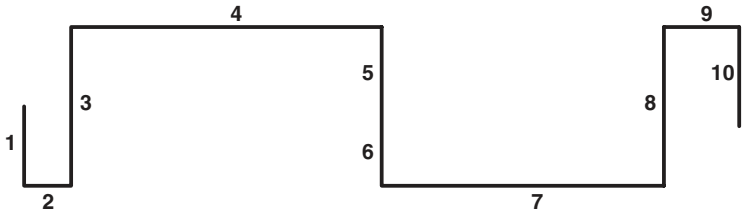
Device input data is passed during states number 4 and number 5 if dtg1_pass_through is on.



STATE	DURATION
1	Fixed at 1T
2	dtg1_spec_a
3	Fixed at 2T
4	dtg1_spec_g dtg1_spec_a-4
5	dtg1_spec_g
6	Fixed at 1T

Figure 4-31. SDTV Line Type FULL_NSP

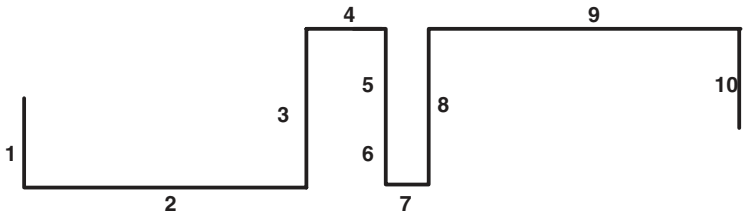
4.7.3.14 NEQ_BSP (Negative Equalization Pulse/Broad Sync Pulse)



STATE	DURATION
1	Fixed at 1T
2	dtg1_spec_c
3	Fixed at 2T
4	dtg1_spec_g dtg1_spec_c-4
5	Fixed at 1T
6	Fixed at 1T
7	dtg1_spec_h
8	Fixed at 2T
9	dtg1_spec_g dtg1_spec_h-4
10	Fixed at 1T

Figure 4-32. SDTV Line Type NEQ_BSP

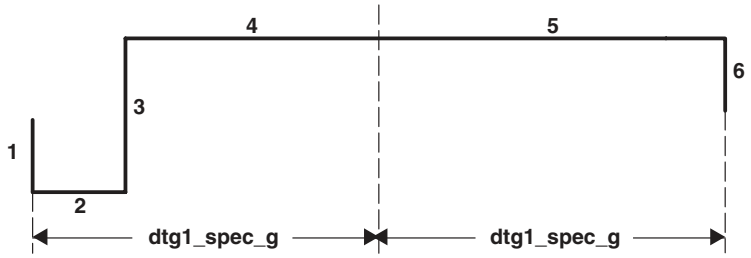
4.7.3.15 BSP_NEQ (Broad Sync Pulse/Negative Equalization Pulse)



STATE	DURATION
1	Fixed at 1T
2	dtg1_spec_h
3	Fixed at 2T
4	dtg1_spec_g dtg1_spec_h-4
5	Fixed at 1T
6	Fixed at 1T
7	dtg1_spec_c
8	Fixed at 2T
9	dtg1_spec_g dtg1_spec_c-4
10	Fixed at 1T

Figure 4-33. SDTV Line Type BSP_NEQ

4.7.3.16 FULL_NEQ (Full Negative Equalization Pulse)

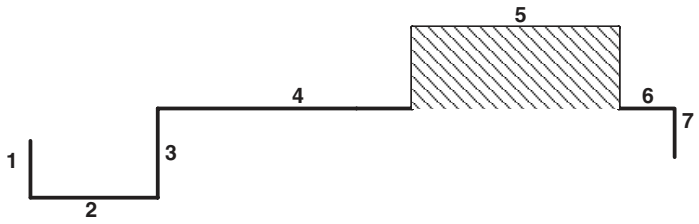


STATE	DURATION
1	Fixed at 1T
2	dtg1_spec_c
3	Fixed at 2T
4	dtg1_spec_g dtg1_spec_c-4
5	dtg1_spec_g
6	Fixed at 1T

Figure 4-34. SDTV Line Type FULL_NEQ

4.7.3.17 NSP_ACTIVE (Normal Sync Pulse/Active Video)

Video data is always passed during state number 5.

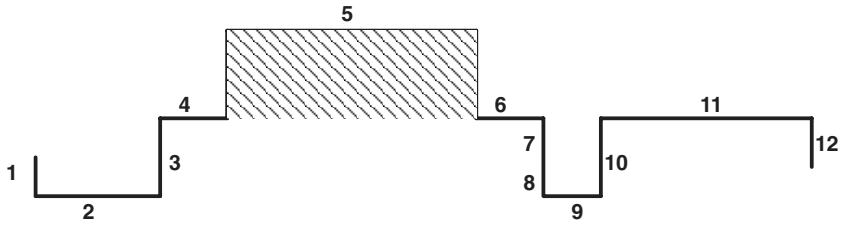


STATE	DURATION
1	Fixed at 1T
2	dtg1_spec_a
3	Fixed at 2T
4	dtg1_spec_g dtg1_spec_a+ dtg1_spec_d1-3
5	dtg1_spec_g dtg1_spec_d1 dtg1_spec_k
6	dtg1_spec_k1
7	Fixed at 1T

Figure 4-35. SDTV Line Type NSP_ACTIVE

4.7.3.18 ACTIVE_NEQ (Active Video/Negative Equalization Pulse)

Video data is always passed during state number 5.

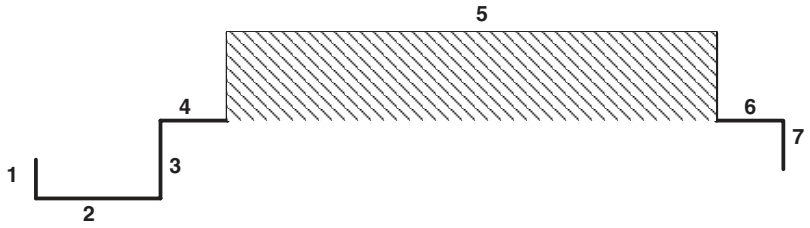


STATE	DURATION
1	Fixed at 1T
2	dtg1_spec_a
3	Fixed at 2T
4	dtg1_spec_d dtg1_spec_a-3
5	dtg1_spec_g dtg1_spec_d dtg1_spec_k1
6	dtg1_spec_k-1
7	Fixed at 1T
8	Fixed at 1T
9	dtg1_spec_c
10	Fixed at 2T
11	dtg1_spec_g dtg1_spec_c-4
12	Fixed at 1T

Figure 4-36. SDTV Line Type ACTIVE_NEQ

4.7.3.19 ACTIVE VIDEO

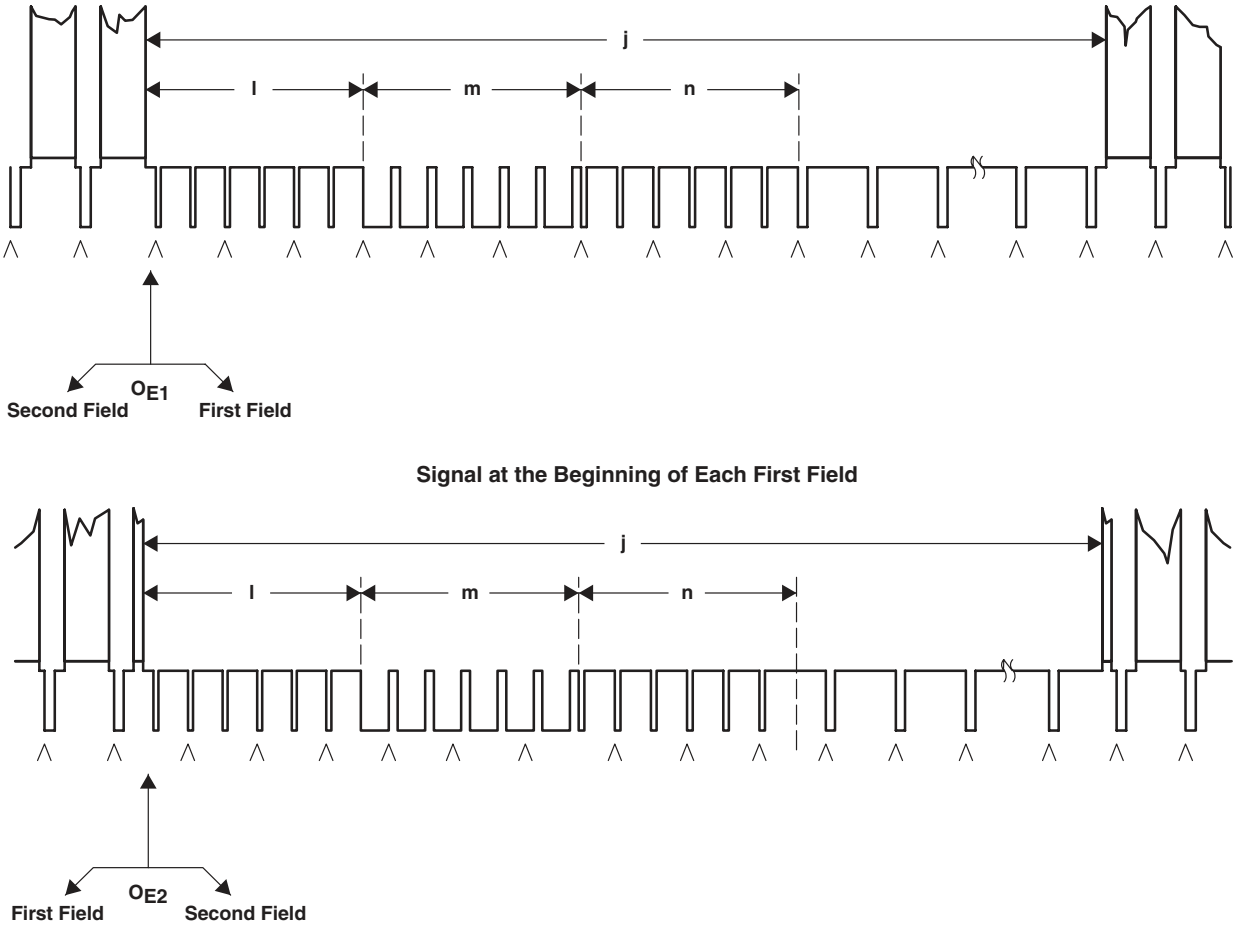
Video data is always passed during state number 5.



STATE	DURATION
1	Fixed at 1T
2	dtg1_spec_a
3	Fixed at 2T
4	dtg1_spec_d dtg1_spec_a-3
5	dtg1_total_pixels dtg1_spec_d dtg1_spec_k
6	dtg1_spec_k-1
7	Fixed at 1T

Figure 4-37. SDTV Line Type ACTIVE_VIDEO

Example:525I



NOTE: l = m = n = 3
j = 20

Figure 4-38. Field/Frame Synchronizing Signal Waveform (525I Format)

When the 525I preset is selected, the following line type sequence is active:

Breakpoints	Line Type
4	NEQ_NEQ
7	BSP_BSP
10	NEQ_NEQ
20	FULL_NSP
263	ACTIVE_VIDEO
264	ACTIVE_NEQ
266	NEQ_NEQ
267	NEQ_BSP
269	BSP_BSP
270	BSP_NEQ
272	NEQ_NEQ
273	FULL_NEQ
282	FULL_NSP
283	NSP_ACTIVE
526	ACTIVE_VIDEO

frame_size = 1000001101; 525d

field_size = 00100000111; 263d

It can be seen this corresponds to the frame format shown, with 263 lines in digital field1 and 262 lines in digital field2.

4.8 D/A Conversion

THS8200 contains 3 DACs with an internal resolution of 11 bits, and maximum speed of 205 MSPS. This allows operation with all (H)DTV formats including 1080P, and PC graphics formats up to UXGA at 75 Hz.

The DAC output compliance can be selected between two full-scale ranges using the data_fsadj register. DIGMUX selects DTG output data during nonvideo line types, except when dtg1_passthrough is active: in this case video input data still is passed during the active video portion of certain line types, as identified in Section 4.7.3 on the DTG line types.

THS8200 supports output in either RGB or YPbPr color spaces. When using RGB output, the dtg2_rgb_mode_on register needs to be set. In this case an offset is added to all DAC output channels in order to provide headroom for the negative sync. Nominally the blanking level is at 350 mV, and the 700 mV swing extends upwards. Therefore peak white corresponds to 1.05 V. When YPbPr mode is selected on this register, the offset is only added to the Y channel output; Pb and Pr outputs now have a video range from 0 to 700 mV with 0 V corresponding to internal DAC input code 0 (note that due to the CSM block this could correspond to another device input code). The Cb and Cr chroma difference channels are thus assumed to be offset binary encoded, not 2s complement.

Finally, the DTG mode determines whether the DIGMUX switches in output data from the DTG. For example, in VESA mode the DACs are always driven by the video input bus. When the DTG overrides the video input bus in SDTV or HDTV modes, the actual amplitude levels output by the DACs during this time are user-programmable via the dtg1_<y,cbcr>_blank , dtg1_<y, cbcr>_sync_low, and dtg1_<y, cbcr>_high registers.

We next outline some of the analog component video output formats that can be generated from THS8200.

4.8.1 RGB Output Without Sync Signal Insertion/General-Purpose Application DAC

In this mode, no sync signal is inserted on any of the analog outputs. HS_OUT and VS_OUT signals are generated for output video synchronization. This mode is commonly used in computer graphics video output.

Two levels of full-scale output can be selected by software. For video applications, the nominal voltage levels are 0.7 V and 1.305 V.

For component video applications, the nominal voltage level is 0.7 V; 1.305 V is used in NTSC/PAL composite video display. For composite video applications, the digital video stream must be encoded in an external digital NTSC/PAL encoder. The THS8200 only converts the digital composite signal to analog composite video.Figure 4-39 illustrates analog outputs without sync insertion.

When the THS8200 is programmed in this mode, it can also be used as a general-purpose DAC due to the linear response to the DAC input codes. Optionally, the CSM block can be bypassed to avoid any processing on the device input codes.

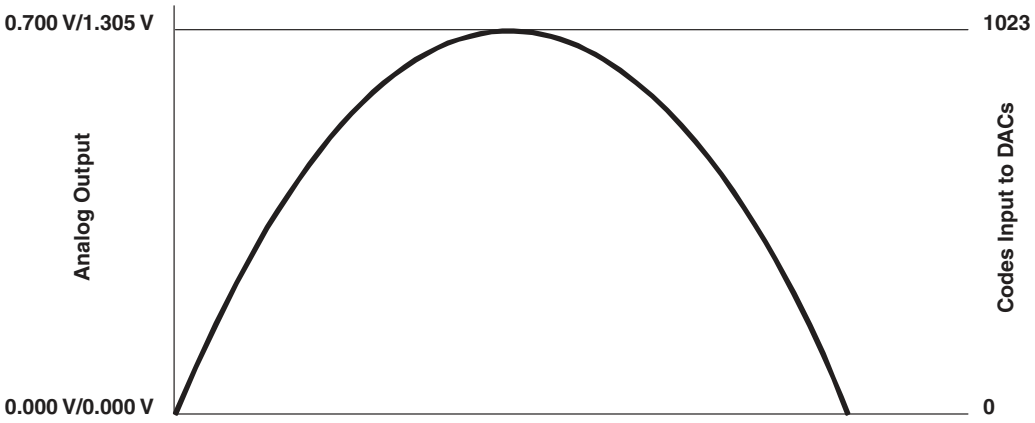


Figure 4-39. RGB Without Sync Insertion or Composite Video Output

Figure 4-40 shows the linear DAC I/O relationship for either of the two nominal full-scale settings.

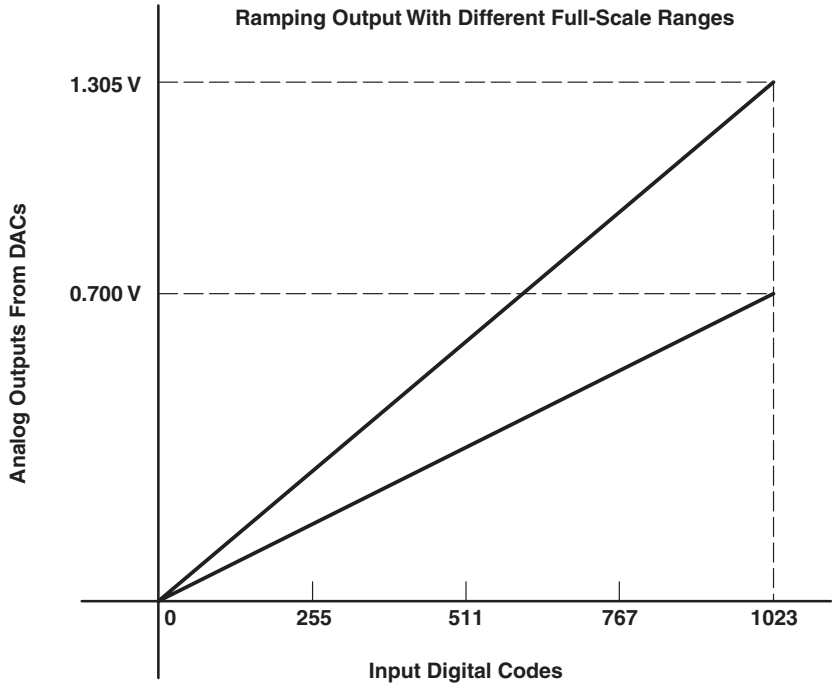


Figure 4-40. Ramping Output With Different Full-Scale Ranges

4.8.2 SMPTE-Compatible RGB Output With Sync Signal Inserted on G (Green) Channel

In this mode, a tri-level (HDTV modes)/bi-level (SDTV modes) sync signal is inserted into the G channel. The nominal analog output voltage range, which is from the sync tip to the peak of active video, is from 0.0 V to 1.050 V. During the active video period, the peak-to-peak ac value (dynamic range) is 700 mV (from 350 mV to 1050 mV). The blank levels on all three channels correspond to the bottom code 64 and are at 350 mV. Figure 4-41 and Figure 4-42 illustrate the analog video output signals, both the output from the G channel with a tri-level or a bi-level sync pulse inserted, as well as the outputs from R and B channels. No sync signal is inserted during the sync period on R and B channels.

Alternatively, sync can be inserted on all three channels on THS8200 by appropriately programming the sync amplitude levels. On those channels where no sync is inserted, the blank levels are maintained at a 350-mV dc level.

The range of active video codes on the R, G, and B channels is from 64 to 940. By definition, code 64 corresponds to blank-level output, and code 940 corresponds to peak analog output. Input codes outside this region can either be clipped by THS8200 or can be passed, depending on the CSM setting. When passed, the user should make sure not to overdrive the DAC outputs outside the DAC output compliance range if instantaneously high output codes would occur.

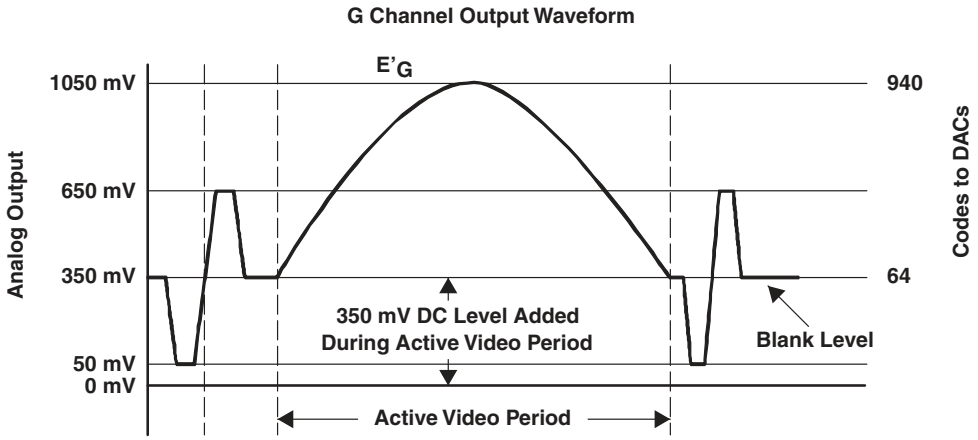


Figure 4-41. G-Channel Output Waveform

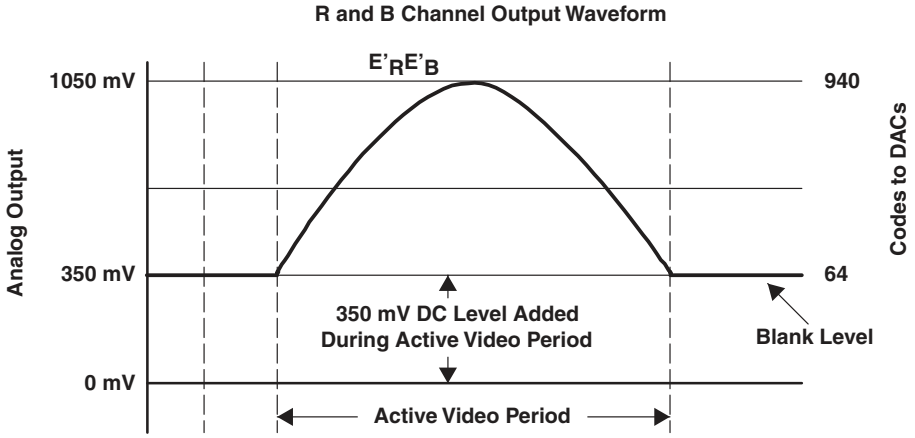


Figure 4-42. R- and B-Channel Output Waveform

4.8.3 SMPTE-Compatible Analog-Level Output With Sync Inserted on All RGB Channels

This is another SMPTE-compatible RGB output. This mode is very similar to the mode described in Section 4.8.2, except the sync signals are inserted on all three channels. Now all three channels have the same analog output format, during both the active video period and the sync period.

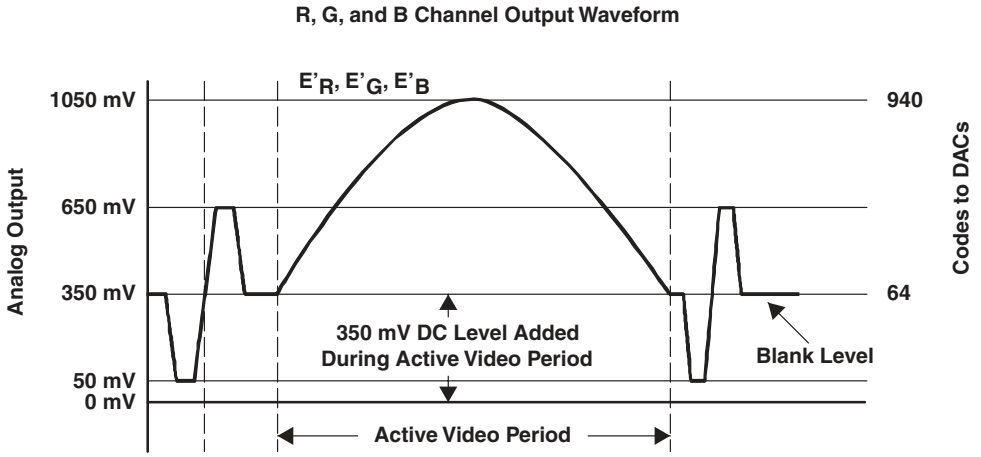


Figure 4-43. R-, G-, and B-Channel Output Waveform

4.8.4 SMPTE-Compatible YPbPr Output With Sync Signal Inserted on Y Channel Only

In this mode, the output color space is YCrCb. The sync signal is inserted on the Y channel only.

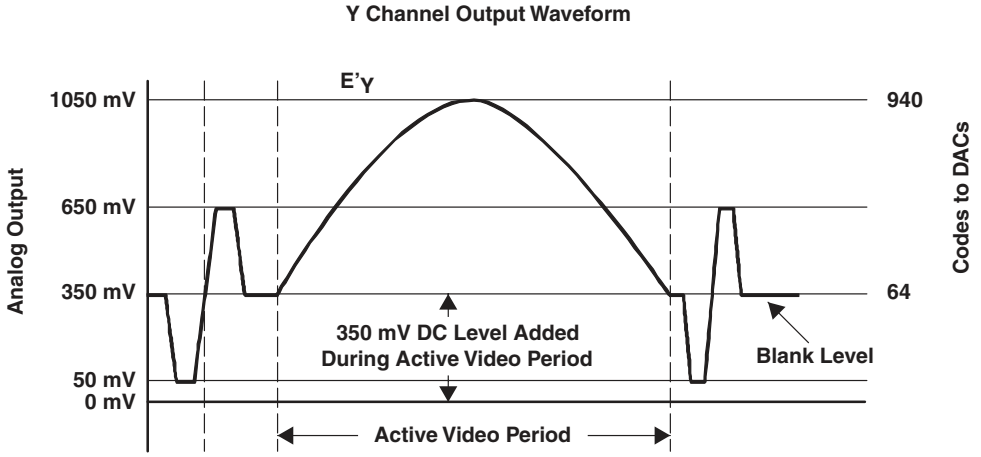


Figure 4-44. Y-Channel Output Waveform

The input code range of the Y channel is from 64 to 940, but the range of input codes of Cr and Cb is from 64 to 960.

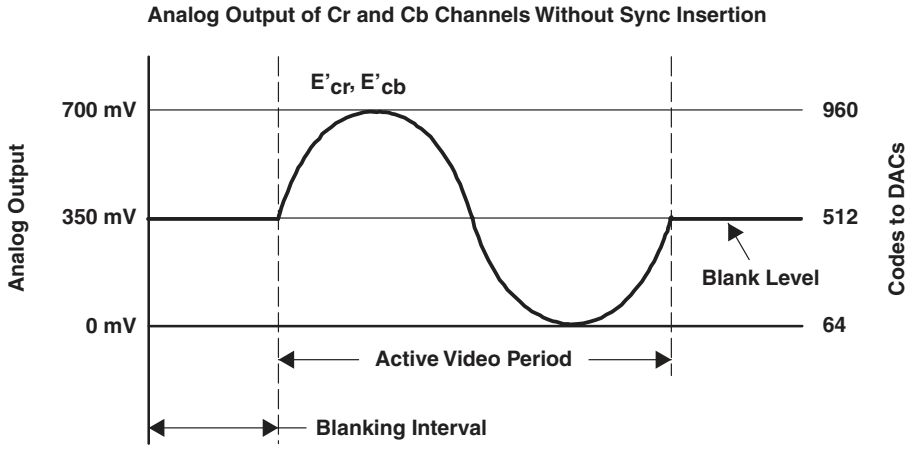


Figure 4-45. Analog Output of Cr and Cb Channels Without Sync Insertion

The blanking level of all channels is at 350 mV. Note that for the Pb and Pr output channels, there is no dc offset added, so DAC input code 0 now corresponds to 0 V dc output. Whether or not offset is added to the DAC outputs is determined from the setting of the dtg2_rgb_mode_on register.

4.8.5 SMPTE-Compatible YPbPr Output With Sync Signal Inserted on All Channels

In this mode, sync signals are inserted on all three channels Y, Cr, and Cb. The Y channel output is identical to that of Section 4.8.4. The Pb and Pr channel outputs are shown below. The range of input codes to the Y channel is from 64 to 940. The range of input codes to the CrCb channels is from 64 to 960.

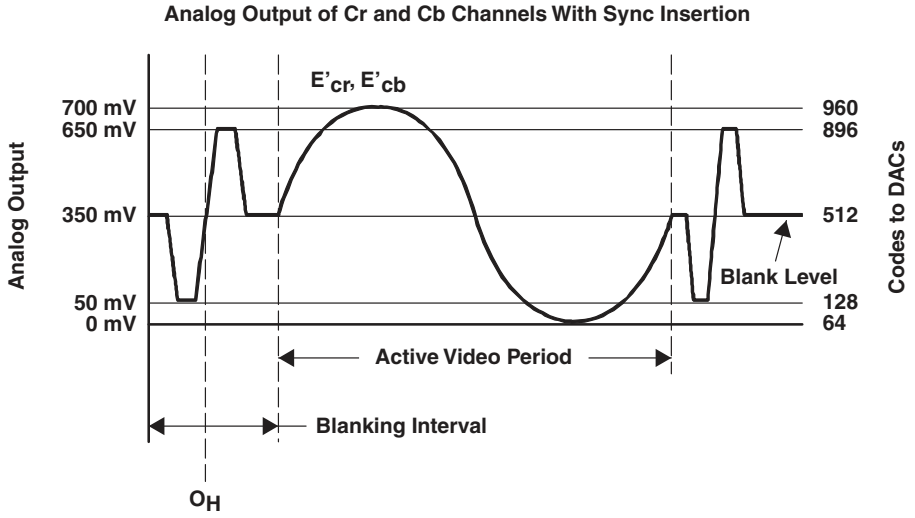


Figure 4-46. Analog Output of Cr and Cb Channels With Sync Insertion

The ac dynamic range during the active video period is the same on all channels, 700 mV. This means that two different code ranges are mapped to the same analog output range. Because three DACs in the THS8200 share a common full-scale adjust resistor, therefore, different input codes to the DAC result in different analog outputs. In order to map two code ranges into a same analog output, the input code range must be scaled in the CSM block.

4.8.6 Summary of Supported Video Formats

	RGB WITHOUT SYNC	RGB SYNC ON G	RGB SYNC ON ALL	YPbPr SYNC ON Y	YPbPr SYNC ON ALL
Range of input codes	0 to 1023	64 to 940	64 to 940	64 to 940 on Y; 64 to 960 on Cr and Cb	64 to 940 on Y; 64 to 960 on Cr and Cb
Peak level	700 mV or 1305 mV	1050 mV	1050 mV	1050 mV	1050 mV
Blank level	0 V	350 mV	350 mV	350 mV	350 mV
DC level shift during active video period	0	350 mV	350 mV	350 mV	350 mV

4.9 Test Functions

The user can activate a 75% SMPTE color bar test pattern when the device is configured in VESA mode using the vesa_colorbars register setting. The width of each color bar can be programmed using the dtg1_vesa_cbar_size register.

The digital logic in front of the DACs can be completely bypassed and the DACs can be driven directly with levels programmed from the I^2C interface by activating the dac_i2c_cntl register. In this case the dac<n>_cntl registers set the DAC input codes. A fast or slow ramp signal can be internally generated and sent to the DACs using tst_fastramp and tst_slowramp registers. This could be useful for a static DAC linearity test.

Alternatively, the input bus can directly drive the DACs when the tst_digbypass register is activated for tests at full speed.

The delay of the Y channel can be changed in YCbCr modes with respect to Cb and Cr channels by programming the tst_ydelay register.

Finally, there is a digital output port with data encoded according to ITU-R.BT656. This is a loop-through of the original input bus, prior to any THS8200 internal processing, and thus only provides standard data when input to the THS8200 is provided in a 10-bit ITU-R BT.656 format. This output bus could be used to connect to a separate NTSC/PAL video encoder. The data_clk656_on register activates the clock output on this bus and the data_tristate656 register disables the output bus. It is recommended to disable this output when not in use.

4.10 Power Down

THS8200 implements two power-down modes: dac_pwdn powers down the DAC channels but keeps all digital logic active; chip_pwdn powers down the digital logic except the I^2C interface. Activating both registers enforces a complete analog/digital power down except for the I^2C interface.

4.11 CGMS Insertion

The THS8200 can embed data within the vertical blanking interval, encoded according to the EIA-805 data insertion standard. CGMS is an implementation of the EIA-805 standard that defines data insertion in component video interface (CVI) video signals.

The THS8200 supports CGMS data insertion on line 41 of every frame in the 525P format. The data is inserted on the Y channel only; Pb and Pr channels remain at the blanking level. CGMS data insertion is enabled by activating the cgms_en register and programming the cgms_header and cgms_payload registers appropriately. The user needs to program header and payload data in the correct format, as no additional data encoding is done prior to insertion into the analog DAC output. The THS8200 only performs a play-out function for the programmed data. The CGMS encoding block assumes that a full 10-bit video range is used in order to determine the 70% of peak-white amplitude of a logic 1 bit, as prescribed by EIA-805. The CSM does not affect the amplitude of the CGMS data insertion.

CGMS is inserted on line 41 as prescribed by EIA 770 standards for progressive format display of SDTV. Fourteen bits can be inserted on this line, consisting of 6 bits header and 8 bits payload. The user can directly program these bits into the corresponding THS8200 registers. Care should be taken to format this data according to CGMS semantics; the user is referred to the original standards to determine header/payload data programming. To avoid the transmission of invalid data, the data transmitted is updated only when the CGMS register with the highest subaddress is programmed with cgms_en active.

CGMS insertion is possible in either 1× or 2× interpolated video modes of the THS8200. While EIA-805 allows the inserted data to change on every frame, and also allows data packets that would span multiple lines (and therefore also multiple frames, since only 1 line/frame is used for insertion), the THS8200 does not support multiline data insertion because it is not required for CGMS.

4.12 I^2C Interface

The THS8200 contains a slave-only I^2C interface on which both write and read are supported. The register map shows which registers support read/write (R/W) and which are read-only (R). The device supports normal and fast I^2C modes (SCL up to 400 kHz). The I^2C interface is also operational when no input clock is received on CLKIN.

To discriminate between write and read operations, the device is addressed at separate device addresses. There is an automatic internal sub-address increment counter to efficiently write/read multiple bytes in the register map during one write/read operation. Furthermore, bit1 of the I^2C device address is dependent upon the setting of the I2CA pin, as follows:

- If address-selecting pin I2CA = 0, then
  - write address is 40h (0100 0000)
  - read address is 41h (0100 0001)
- If address-selecting pin I2CA = 1, then
  - write address is 42h (0100 0010)
  - read address is 43h (0100 0011)

The I^2C interface supports fast I^2C, i.e., SCL up to 400 kHz.

WRITE FORMAT

S	Slave address(w)	A	Sub-address	A	Data0	A	.....	DataN-1	A	P

S	Start condition
Slave address(w)	0100 0000 (0x40) if I2CA = 0, or 0100 0010 (0x42) if I2CA = 1
A	Acknowledge, generated by the THS8200
Sub-address	Sub-address of the first register to write, length: 1 byte
Data0	First byte of the data
DataN-1	Nth byte of the data
P	Stop condition

READ FORMAT

First write the sub-address, where the data must be read out to the THS8200 in the format as follows:

S	Slave address(w)	A	Sub-address	A	P

S	Slave address(r)	A	DataN	AM	Data(N+1)	AM	.....	NAM	P

S	Start condition
Slave address(r)	0100 0001 (0x41) if I2CA = 0, or 0100 0011 (0x43) if I2CA = 1
A	Acknowledge, generated by the THS8200; if the transmission is successful, then A = 0, else A = 1
AM	Acknowledge, generated by a master
NAM	Not acknowledge, generated by a master

Sub-address	Sub-address of the first register to read, length: 1 byte
Data0	First byte of the data read
DataN+1	Nth byte of the data read
P	Stop condition

In both write and read operations, the sub-address is incremented automatically when multiple bytes are written/read. Therefore, only the first sub-address needs to be supplied to the THS8200.

5 I²C Register Map

R/W registers can be written and read.

R registers are read-only.

REGISTER NAME	R/W	SUB-ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		0x00	Reserved							
		0x01								
SYSTEM										
version	R	0x02	ver7	ver6	ver5	ver4	ver3	ver2	ver1	ver0
chip_ctl	R/W	0x03	vesa_clk	dll_bypass	vesa_color bars	dll_freq_ sel	dac_pwdn	chip_pwdn	chip_ms	arst_ func_n
COLOR SPACE CONVERSION										
csc_r11	R/W	0x04	csc_ric1(5:0)						csc_rfc1(9:8)	
csc_r12	R/W	0x05	csc_rfc1(7:0)							
csc_r21	R/W	0x06	csc_ric2(5:0)						csc_rfc2(9:8)	
csc_r22	R/W	0x07	csc_rfc2(7:0)							
csc_r31	R/W	0x08	csc_ric3(5:0)						csc_rfc3(9:8)	
csc_r32	R/W	0x09	csc_rfc3(7:0)							
csc_g11	R/W	0x0a	csc_gic1(5:0)						csc_gfc1(9:8)	
csc_g12	R/W	0x0b	csc_gfc1(7:0)							
csc_g21	R/W	0x0c	csc_gic2(5:0)						csc_gfc2(9:8)	
csc_g22	R/W	0x0d	csc_gfc2(7:0)							
csc_g31	R/W	0x0e	csc_gic3(5:0)						csc_gfc3(9:8)	
csc_g32	R/W	0x0f	csc_gfc3(7:0)							
csc_b11	R/W	0x10	csc_bic1(5:0)						csc_bfc1(9:8)	
csc_b12	R/W	0x11	csc_bfc1(7:0)							
csc_b21	R/W	0x12	csc_bic2(5:0)						csc_bfc2(9:8)	
csc_b22	R/W	0x13	csc_bfc2(7:0)							
csc_b31	R/W	0x14	csc_bic3(5:0)						csc_bfc3(9:8)	
csc_b32	R/W	0x15	csc_bfc3(7:0)							
csc_offs1	R/W	0x16	csc_offset1(9:2)							
csc_offs12	R/W	0x17	csc_offset1(1:0)		csc_offset2(9:4)					
csc_offs23	R/W	0x18	csc_offset2(3:0)				csc_offset3(9:6)			
csc_offs3	R/W	0x19	csc_offset3(5:0)						csc_ bypass	c_uof_cnt l
TEST										
tst_cntl1	R/W	0x1a	st_ digbpass	tst_offset	Reserved					
tst_cntl2	R/W	0x1b	tst_ydelay(1:0)		Reserved	Reserved	Reserved	Reserved	tst_ fastramp	tst_ slowramp
DATA PATH										
data_cntl	R/W	0x1c	data_ clk6 56_on	data_fsadj	data_ifir12 _bypass	data_ifir35 _bypass	data_ tristate656	data_dman_cntl(2:0)		
DISPLAY TIMING GENERATION, PART 1										
dtg1_y_ sync1_lsb	R/W	0x1d	dtg1_y_blank(7:0)							
dtg1_y_ sync2_lsb	R/W	0x1e	dtg1_y_sync_low(7:0)							
dtg1_y_ sync3_lsb	R/W	0x1f	dtg1_y_sync_high(7:0)							

REGISTER NAME	R/W	SUB-ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
dtg1_cbcr_ sync1_lsb	R/W	0x20	dtg1_cbcr_blank(7:0)							
dtg1_cbcr_ sync2_lsb	R/W	0x21	dtg1_cbcr_sync_low(7:0)							
dtg1_cbcr_ sync3_lsb	R/W	0x22	dtg1_cbcr_sync_high(7:0)							
dtg1_y_ sync_msb	R/W	0x23	Reserved	Reserved	dtg1_y_blank(9:8)		dtg1_y_sync_low(9:8)		dtg1_y_sync_high(9:8)	
dtg1_cbcr_ sync_msb	R/W	0x24	Reserved	Reserved	dtg1_cbcr_blank(9:8)		dtg1_cbcr_sync_low (9:8)		dtg1_cbcr_ sync_high(9:8)	
dtg1_spec_ a	R/W	0x25	dtg1_spec_a(7:0)							
dtg1_spec_ b	R/W	0x26	dtg1_spec_b(7:0)							
dtg1_spec_ c	R/W	0x27	dtg1_spec_c(7:0)							
dtg1_spec_ d_lsb	R/W	0x28	dtg1_spec_d(7:0)							
dtg1_spec_ d1	R/W	0x29	dtg1_spec_d1(7:0)							
dtg1_spec_ e_lsb	R/W	0x2a	dtg1_spec_e(7:0)							
dtg1_spec_ deh_msb	R/W	0x2b	dtg1_ spe c_d(8)	dtg1_spec _e(8)	Reserved	Reserved	Reserved	Reserved	dtg1_spec_h(9:8)	
dtg1_spec_ h_lsb	R/W	0x2c	dtg1_spec_h(7:0)							
dtg1_spec_ i_msb	R/W	0x2d	Reserved	Reserved	Reserved	Reserved	dtg1_spec_i(11:8)			
dtg1_spec_ i_lsb	R/W	0x2e	dtg1_spec_i(7:0)							
dtg1_spec_ k_lsb	R/W	0x2f	dtg1_spec_k(7:0)							
dtg1_spec_ k_msb	R/W	0x30	Reserved	Reserved	Reserved	Reserved	Reserved	dtg1_spec_k(10:8)		
dtg1_spec_ k1	R/W	0x31	dtg1_spec_k1(7:0)							
dtg1_spec_ g_lsb	R/W	0x32	dtg1_spec_g(7:0)							
dtg1_spec_ g_msb	R/W	0x33	Reserved	Reserved	Reserved	Reserved	dtg1_spec_g(11:8)			
dtg1_total_ pixels_msb	R/W	0x34	Reserved	Reserved	Reserved	dtg1_total_pixels(12:8)				
dtg1_total_ pixels_lsb	R/W	0x35	dtg1_total_pixels(7:0)							
dtg1_fieldflip_ linecnt_ msb	R/W	0x36	dtg1_field _flip	Reserved	Reserved	Reserved	Reserved	dtg1_linecnt(10:8)		
dtg1_ linecnt_lsb	R/W	0x37	dtg1_linecnt(7:0)							
dtg1_mode	R/W	0x38	dtg1_on	Reserved	Reserved	dtg1_pass _through	dtg1_mode(3:0)			
dtg1_frame _field_size_ msb	R/W	0x39	Reserved	dtg1_frame_size(10:8)			Reserved	dtg1_field_size(10:8)		
dtg1_frame size_lsb	R/W	0x3a	dtg1_frame_size(7:0)							
dtg1_field_ size_lsb	R/W	0x3b	dtg1_field_size(7:0)							
dtg1_vesa_ cbar_size	R/W	0x3c	dtg1_vesa_cbar_size(7:0)							
DAC										

REGISTER NAME	R/W	SUB-ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
dac_cntl_ msb	R/W	0x3d	Reserved	dac_i2c_ cntl	dac1_cntl(9:8)		dac2_cntl(9:8)		dac3_cntl(9:8)	
dac1_cntl_ lsb	R/W	0x3e	dac1_cntl(7:0)							
dac2_cntl_ lsb	R/W	0x3f	dac2_cntl(7:0)							
dac3_cntl_ lsb	R/W	0x40	dac3_cntl(7:0)							
CLIP/SHIFT/MULTIPLIER										
csm_clip_ gy_low	R/W	0x41	csm_clip_gy_low(7:0)							
csm_clip_ bcb_low	R/W	0x42	csm_clip_bcb_low(7:0)							
csm_clip_ rcr_low	R/W	0x43	csm_clip_rcr_low(7:0)							
csm_clip_ gy_high	R/W	0x44	csm_clip_gy_high(7:0)							
csm_clip_ bcb_high	R/W	0x45	csm_clip_bcb_high(7:0)							
csm_clip_ rcr_high	R/W	0x46	csm_clip_rcr_high(7:0)							
csm_shift_ gy	R/W	0x47	csm_shift_gy(7:0)							
csm_shift_ bcb	R/W	0x48	csm_shift_bcb(7:0)							
csm_shift_ rcr	R/W	0x49	csm_shift_rcr(7:0)							
csm_gy_ cntl_mult_ msb	R/W	0x4a	csm_mult _ gy_on	csm_shift_ gy_on	csm_gy_ high_clip_ on	csm_gy_ low_clip_ on	csm_of_ cntl	csm_mult_gy(10:8)		
csm_mult_ bcb_rcr_ msb	R/W	0x4b	Reserved	csm_mult_bcb(10:8)				Reserved	csm_mult_rcr(10:8)	
csm_mult_ gy_lsb	R/W	0x4c	csm_mult_gy(7:0)							
csm_mult_ bcb_lsb	R/W	0x4d	csm_mult_bcb(7:0)							
csm_mult_ rcr_lsb	R/W	0x4e	csm_mult_rcr(7:0)							
csm_rcr_ bcb_cntl	R/W	0x4f	csm_mult _ rcr_on	csm_mult_ bcb_on	csm_shift_ rcr_on	csm_shift_ bcb_on	csm_rcr_ high_clip_ on	csm_rcr_ low_clip_ on	csm_bcb_ high_clip_ on	csm_bcb _ low_clip_ on
DISPLAY TIMING GENERATION, PART 2										
dtg2_bp1_ 2_msb	R/W	0x50	Reserved	dtg2_bp1(10:8)			Reserved	dtg2_bp2(10:8)		
dtg2_bp3_ 4_msb	R/W	0x51	Reserved	dtg2_bp3(10:8)			Reserved	dtg2_bp4(10:8)		
dtg2_bp5_ 6_msb	R/W	0x52	Reserved	dtg2_bp5(10:8)			Reserved	dtg2_bp6(10:8)		
dtg2_bp7_ 8_msb	R/W	0x53	Reserved	dtg2_bp7(10:8)			Reserved	dtg2_bp8(10:8)		
dtg2_bp9_ 10_msb	R/W	0x54	Reserved	dtg2_bp9(10:8)			Reserved	dtg2_bp10(10:8)		
dtg2_bp11_ 12_msb	R/W	0x55	Reserved	dtg2_bp11(10:8)			Reserved	dtg2_bp12(10:8)		
dtg2_bp13_ 14_msb	R/W	0x56	Reserved	dtg2_bp13(10:8)			Reserved	dtg2_bp14(10:8)		
dtg2_bp15_ 16_msb	R/W	0x57	Reserved	dtg2_bp15(10:8)			Reserved	dtg2_bp16(10:8)		
dtg2_bp1_ lsb	R/W	0x58	dtg2_bp1(7:0)							
dtg2_bp2_ lsb	R/W	0x59	dtg2_bp2(7:0)							
dtg2_bp3_ lsb	R/W	0x5a	dtg2_bp3(7:0)							

REGISTER NAME	R/W	SUB-ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
dtg2_bp4_ lsb	R/W	0x5b	dtg2_bp4(7:0)							
dtg2_bp5_ lsb	R/W	0x5c	dtg2_bp5(7:0)							
dtg2_bp6_ lsb	R/W	0x5d	dtg2_bp6(7:0)							
dtg2_bp7_ lsb	R/W	0x5e	dtg2_bp7(7:0)							
dtg2_bp8_ lsb	R/W	0x5f	dtg2_bp8(7:0)							
dtg2_bp9_ lsb	R/W	0x60	dtg2_bp9(7:0)							
dtg2_bp10_ lsb	R/W	0x61	dtg2_bp10(7:0)							
dtg2_bp11_ lsb	R/W	0x62	dtg2_bp11(7:0)							
dtg2_bp12_ lsb	R/W	0x63	dtg2_bp12(7:0)							
dtg2_bp13_ lsb	R/W	0x64	dtg2_bp13(7:0)							
dtg2_bp14_ lsb	R/W	0x65	dtg2_bp14(7:0)							
dtg2_bp15_ lsb	R/W	0x66	dtg2_bp15(7:0)							
dtg2_bp16_ lsb	R/W	0x67	dtg2_bp16(7:0)							
dtg2_ linetype1	R/W	0x68	dtg2_linetype1(3:0)				dtg2_linetype2(3:0)			
dtg2_ linetype2	R/W	0x69	dtg2_linetype3(3:0)				dtg2_linetype4(3:0)			
dtg2_ linetype3	R/W	0x6a	dtg2_linetype5(3:0)				dtg2_linetype6(3:0)			
dtg2_ linetype4	R/W	0x6b	dtg2_linetype7(3:0)				dtg2_linetype8(3:0)			
dtg2_ linetype5	R/W	0x6c	dtg2_linetype9(3:0)				dtg2_linetype10(3:0)			
dtg2_ linetype6	R/W	0x6d	dtg2_linetype11(3:0)				dtg2_linetype12(3:0)			
dtg2_ linetype7	R/W	0x6e	dtg2_linetype13(3:0)				dtg2_linetype14(3:0)			
dtg2_ linetype8	R/W	0x6f	dtg2_linetype15(3:0)				dtg2_linetype16(3:0)			
dtg2_ hlength_lsb	R/W	0x70	dtg2_hlength(7:0)							
dtg2_ hlength_lsb _hdly_msb	R/W	0x71	dtg2_hlength(9:8)		Reserved	dtg2_hdly(12:8)				
dtg2_hdly_ lsb	R/W	0x72	dtg2_hdly(7:0)							
dtg2_ vlength1_ls b	R/W	0x73	dtg2_vlength1(7:0)							
dtg2_vlength1 _ msb_ vdly1_msb	R/W	0x74	dtg2_vlength1(9:8)		Reserved	Reserved	Reserved	dtg2_vdly1(10:8)		
dtg2_vdly1 _ lsb	R/W	0x75	dtg2_vdly1(7:0)							
dtg2_ vlength2_ls b	R/W	0x76	dtg2_vlength2(7:0)							
dtg2_vlength2 _ msb_ vdly2_msb	R/W	0x77	dtg2_vlength2(9:8)		Reserved	Reserved	Reserved	dtg2_vlength2(9:8)		
dtg2_vdly2 _ lsb	R/W	0x78	dtg2_vdly2(7:0)							
dtg2_hs_ in_dly_msb	R/W	0x79	Reserved	Reserved	Reserved	dtg2_hs_in_dly(12:8)				
dtg2_hs_ in_dly_lsb	R/W	0x7a	dtg2_hs_in_dly(7:0)							
dtg2_vs_in _dly_msb	R/W	0x7b	Reserved	Reserved	Reserved	Reserved	Reserved	dtg2_vs_in_dly(10:8)		

REGISTER NAME	R/W	SUB-ADDRESS	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
dtg2_vs_in _dly_lsb	R/W	0x7c	dtg2_vs_in_dly(7:0)							
dtg2_pixel_ cnt_msb	R	0x7d	dtg2_pixel_cnt(15:8)							
dtg2_pixel_ cnt_lsb	R	0x7e	dtg2_pixel_cnt(7:0)							
dtg2_line_ cnt_msb	R	0x7f	dtg2_ip_ fmt	Reserved				dtg2_line_cnt(10:8)		
dtg2_line_ cnt_msb	R	0x80	dtg2_line_cnt(7:0)							
		0x81	Reserved							
dtg2_cntl	R/W	0x82	dtg2_fid_ de_cntl	dtg2_rgb_ mode_on	dtg2_emb edded_ timing	dtg2_ vsout_pol	dtg2_h sout_pol	dtg2_fid_ pol	dtg2_vs_ pol	dtg2_hs_ pol
CGMS CONTROL										
cgms_cntl_ header	R/W	0x83	Reserved	cgms_en	cgms_header(5:0)					
cgms_payload _ msb	R/W	0x84	Reserved	Reserved	cgms_payload(13:8)					
cgms_payload _ lsb	R/W	0x85	cgms_payload(7:0)							
misc_ppl_ lsb	R	0x86	misc_ppl(7:0)							
misc_ppl_ msb	R	0x87	misc_ppl(7:0)							
misc_lpf_ lsb	R	0x88	misc_lpf(7:0)							
misc_lpf_ msb	R	0x89	misc_lpf(15:8)							

5.1 Register Descriptions

Between { } are shown the name(s), subaddress(es) and bit position(s) where each register can be found in the register map.

The default register value is shown between [ ] in binary format, and hexadecimal (h) and/or decimal (d) notation where listed.

5.1.1 System Control (Sub-Addresses 0x02−0x03)

ver(7:0): **Device version**

{version 0x02(7..0)} [0000 0000]

The user can read this register to find out which version of THS8200 is in the system.

vesa_clk: **Clock mode selection**

{chip_ctl 0x03(7)} [0]

0 : Normal operation

1 : All clocks become identical, except for the half-rate clock, and the DLL is bypassed. This is used in VESA mode to support a direct 205-MHz input clock. No internal 2× interpolation is available. This mode should be used for all formats that require a >80 MSPS pixel clock because the internal DLL for 2× clock generation is specified only up to 80 MSPS.

The half-rate clock is still internally generated if needed to allow, e.g., 148-MHz 20-bit input (1080P).

dll_bypass: **DLL bypass**

{chip_ctl 0x03(6)} [0]

0 : DLL used for clock generation; normal operation with internally generated 2× clock. This mode should be selected for most video formats when a 1× clock is available on the device clock input, and either 1× or 2× DAC operation is desired internally (as selected by register data_ifir35_bypass)

1 : DLL bypassed for clock generation. In this case the clock input on the CLKIN pin is used directly as the 2× clock, rather than the internally generated signal from the DLL. This mode is meant for test purposes only.

vesa_colorbars: **Color bar test pattern**

{chip_ctl 0x03(5)} [0]

0 : normal operation

1 : Device generates color bar pattern; external video inputs are ignored. The color bar pattern is only supported in VESA PC graphics mode, with the device configured in master mode (chip_ms = 1).

dll_freq_sel: **dll_freq_sel:**

{chip_ctl 0x03(4)} [0]

Sets a frequency range for the DLL 2× clock generation. The DLL should not be used at >80 MHz. In this case the vesa_clk register should be enabled. As a consequence, 2× video interpolation is not available for formats with >80 MHz pixel clock.

0 : high frequency range: pixel clock from 40−80 MHz

1 : low frequency range: pixel clock from 10−40 MHz

dac_pwdn: **dac_pwdn:**

{chip_ctl 0x03(3)} [0]

0 : normal operation

1 : DACs go into power-down state.

chip_pwdn: **Chip power down**

{chip_ctl 0x03(2)} [0]

0 : normal operation

1 : power down of all digital logic except I^2C

chip_ms: **Chip mode select**

{chip_ctl 0x03(1)} [0]

0 : slave mode. Device synchronizes to incoming video sync signals, either embedded in ITU-R.BT656 interface or received from dedicated timing signals.

1 : master mode. Device requests video data and generates video input timing signals to external (memory) device, according to the programmed frame/field format. Master mode is only available when the DTG is operating in VESA mode (PC graphics signals).

arst_func_n: **Chip software reset**

{chip_ctl 0x03(0)} [1]

0 : functional block goes into reset state. I^2C registers retain values.
Note: the user needs to issue a software reset after input video is disconnected from the input bus and reconnected (e.g. after a video format change), in order to synchronize the internal display timing generator to the input video source properly.

1 : normal operation

5.1.2 Color Space Conversion Control (Sub-Addresses 0x04−0x19)

Signed magnitude: MSB is sign bit, remaining bits are binary representation of magnitude. This is not a 2s complement notation.

Magnitude: Binary representation of magnitude.

csc_ric1(5:0): R/Cr input channel – G/Y output channel coefficient, integer part

{csc_r11 0x04(7:2)} [00 0000]

6-bit integer portion of coefficient that is multiplied with R/Cr input, to produce G/Y output (signed magnitude format)

csc_rfc1(9:0): R/Cr input channel – G/Y output channel, fractional part

{csc_r11 0x04(1:0) and csc_r12 0x05(7:0)} [00 0000 0000]

10-bit fractional portion of coefficient that is multiplied with R/Cr input, to produce G/Y output (magnitude format)

csc_ric2(5:0): R/Cr input channel – B/Cb output channel, integer part

{csc_r21 0x06(7:2)} {csc_r21 0x06(7:2)}

6-bit integer portion of coefficient that is multiplied with R/Cr input, to produce B/Cb output (signed magnitude format)

csc_rfc2(9:0): R/Cr input channel – B/Cb output channel, fractional part

{csc_r21 0x06(1:0) and csc_r22 0x07(7:0)} [00 0000 0000]

10-bit fractional portion of coefficient that is multiplied with R/Cr input, to produce B/Cb output (magnitude format)

csc_ric3(5:0): R/Cr input channel – R/Cr output channel, integer part

{csc_r31 0x08(7:2)} [000000]

6-bit integer portion of coefficient that is multiplied with R/Cr input, to produce R/Cr output (signed magnitude format)

csc_rfc3(9:0): R/Cr input channel − R/Cr output channel, fractional part

{csc_r31 0x08(1:0) and csc_r32 0x09(7:0)} [00 0000 0000]

10-bit fractional portion of coefficient that is multiplied with R/Cr input, to produce R/Cr output (magnitude format)

csc_gic1(5:0): G/Y input channel – G/Y output channel, integer part

{csc_g11 0x0A(7:2)} [00 0000]

6-bit fractional portion of coefficient that is multiplied with R/Cr input, to produce R/Cr output (magnitude format)

csc_gfc1(9:0): G/Y input channel – G/Y output channel, fractional part

{csc_g11 0x0A(1:0) and csc_g12 0x0B(7:0)} [00 0000 0000]

10-bit fractional portion of coefficient that is multiplied with G/Y input, to produce G/Y output (magnitude format)

csc_gic2(5:0): **G/Y input channel – B/Cb output channel, integer part**

{csc_g21 0x0C(7:2)} [00 0000]

6-bit integer portion of coefficient that is multiplied with G/Y input, to produce G/Y output (magnitude format)

csc_gfc2(9:0): **G/Y input channel – B/Cb output channel, fractional part**

{csc_g21 0x0C(1:0) and csc_g22 0x0D(7:0)} [00 0000 0000]

10-bit fractional portion of coefficient that is multiplied with G/Y input, to produce B/Cb output (magnitude format)

csc_gic3(5:0): **G/Y input channel – R/Cr output channel, integer part**

{csc_g31 0x0E(7:2)} {csc_g31 0x0E(7:2)}

6-bit integer portion of coefficient that is multiplied with G/Y input, to produce R/Cr output (signed magnitude format)

csc_gfc3(9:0) **G/Y input channel – R/Cr output channel, fractional part**

{csc_g31 0x0E(1:0) and csc_g32 0x0F(7:0)} [00 0000 0000]

10-bit fractional portion of coefficient that is multiplied with G/Y input, to produce R/Cr output (magnitude format)

csc_bic1(5:0): **B/Cb input channel – G/Y output channel, integer part**

{csc_b11 0x10(7:2)} [00 0000]

6-bit integer portion of coefficient that is multiplied with B/Cb input, to produce G/Y output (signed magnitude format)

csc_bfc1(9:0): **B/Cb input channel – G/Y output channel, fractional part**

{csc_b11 0x10(1:0) and csc_b12 0x11(7:0)} [00 0000 0000]

10-bit fractional portion of coefficient that is multiplied with B/Cb input, to produce G/Y output (magnitude format)

csc_bic2(5:0): **B/Cb input channel – B/Cb output channel, integer part**

{csc_b21 0x12(7:2)} [00 0000]

6-bit integer portion of coefficient that is multiplied with B/Cb input, to produce B/Cb output (signed magnitude format)

csc_bfc2(9:0): **B/Cb input channel – B/Cb output channel, fractional part**

{csc_b21 0x12(1:0) and csc_b22 0x13(7:0)} [00 0000 0000]

10-bit fractional portion of coefficient that is multiplied with B/Cb input, to produce B/Cb output (magnitude format)

csc_bic3(5:0): **B/Cb input channel – R/Cr output channel, integer part**

{csc_b31 0x14(7:2)} [00 0000]

6-bit integer portion of coefficient that is multiplied with B/Cb input, to produce R/Cr output (signed magnitude format)

csc_bfc3(9:0): **B/Cb input channel – R/Cr output channel, fractional part**

{csc_b31 0x14(1:0) and csc_b32 0x15(7:0)} [00 0000 0000]

10-bit fractional portion of coefficient that is multiplied with B/Cb input, to produce R/Cr output (magnitude format)

csc_offset1(9:0): **DAC channel 1 offset**

{csc_offs1 0x16(7:0) and csc_offs12 0x17(7:6)} [00 0000 0000]

Offset value for G/Y output (signed magnitude format)

csc_offset2(9:0): **DAC channel 2 offset**

{csc_offs12 0x17(5:0) and csc_offs23 0x18(7:4)} [00 0000 0000]

Offset value for B/Cb output (signed magnitude format)

csc_offset3(9:0): **DAC channel 3 offset**

{csc_offs23 0x18(3:0) and csc_offs3 0x19(7:2)} [00 0000 0000]

Offset value for R/Cr output (signed magnitude format)

csc_bypass: **Bypass for CSC block**

{csc_offs3 0x19(1)} [1]

0 : Color space conversion (CSC) not bypassed

1 : CSC bypassed

csc_uof_cntl: **Under-/overflow control for CSC block**

{csc_offs3 0x19(1)} [0]

Controls over-/underflow protection logic on color space converter

0 : Under-/overflow protection off

1 : Under-/overflow protection on

5.1.3 Test Control (Sub-Addresses 0x1A−0x1B)

tst_digbypass: **Bypass to DAC inputs**

{tst_cntl1 0x1A(7)} [0]

0 : Normal operation; nonbypass

1 : Digital logic bypassed to directly control DACs from input bus

tst_offset: **Bypass for DAC offsets**

{tst_cntl1 0x1A(6)} [0]

0 : Normal operation; logic not bypassed

1 : Programmed offsets are always added to DAC codes regardless of mode or dtg_state

tst_ydelay(1:0): **Y delay path control**

{tst_cntl2 0x1B(7:6)} [00]

Adjusts the delay of the Y channel during YCbCr modes

tst_fastramp: **DAC test control, fast ramp**

{tst_cntl2 0x1B(1)} [0]

0 : Normal operation

1 : DAC outputs a ramp at 2× clock rate.

tst_slowramp: **DAC test control, slow ramp**

{tst_cntl2 0x1B(0)} [0]

0 : Normal operation

1 : DAC outputs a ramp at 2× clock rate divided by 64,000. This mode has a higher priority than the one set by tst_fastramp

5.1.4 Data Path Control (Sub-Address 0x1C)

data_clk656_on: **ITU-R.BT656 output clock control**

{data_cntl 0x1C(7)} [0]

0 : D1CLKO output off

1 : D1CLKO output on

data_fsadj: **Full-scale adjust control**

{data_cntl 0x1C(6)} [0]

Selects which full-scale setting to use. See FSADJ<n> terminal description for nominal full-scale adjust resistor values.

0 : Use full-scale setting from resistor connected to FSADJ2 terminal

1 : Use full-scale setting from resistor connected to FSADJ1 terminal

data_ifir12_bypass: **Bypass control 4:2:2 to 4:4:4**

{data_cntl 0x1C(5)} [0]

0 : Interpolation filters before the CSC are in the data path, enabling 4:2:2 to 4:4:4 conversion internally. This mode should be used when the input data is in 4:2:2 format

1 : Interpolation filters before the CSC are bypassed. This mode should be used when the input data is in 4:4:4 format.

data_ifir35_bypass: **Bypass control 2x interpolation**

{data_cntl 0x1C(4)} [0]

0 : interpolation filters after the CSC are in the data path; enabling 1× to 2× interpolation of the video data.

1 : interpolation filters after the CSC are bypassed. This mode should be used when 1× DAC operation is desired.

data_tristate656: **ITU-R.BT656 output bus**

{data_cntl 0x1C(3)} [0]

0 : the ITU-R.BT656 output bus is active.

1 : the ITU-R.BT656 output bus is in the high-impedance state.

data_dman_cntl(2:0): Data manager control

{data_cntl 0x1C(2:0)} [011]

Selects the format for the input data manager, as follows:

dman_cntl	MODE
000	30-bit YCbCr/RGB 4:4:4
001	16-bit RGB 4:4:4
010	15-bit RGB 4:4:4
011	20-bit YCbCr 4:2:2
100	10-bit YCbCr 4:2:2 (ITU mode)
Others	(Reserved)

5.1.5 Display Timing Generator Control, Part 1 (Sub-Addresses 0x1D−0x3C)

dtg1_y_blank(9:0): Y channel blanking level amplitude control

{dtg1_y_sync_msb 0x23(5:4) and dtg1_y_sync1_lsb 0x1D(7:0)} [10 0000 0000]

Sets the amplitude of the blanking level for the Y channel

dtg1_y_sync_low(9:0): Y channel low sync level amplitude control

{dtg1_y_sync_msb 0x23(3:2) and dtg1_y_sync2_lsb 0x1E(7:0)} [00 0000 0000]

Sets the amplitude of the negative sync and equalization/serration/broad pulses for the Y channel

dtg1_y_sync_high(9:0): Y channel high sync level amplitude control

{dtg1_y_sync_msb 0x23(1:0) and dtg1_y_sync3_lsb 0x1F(7:0)} [11 0000 0000]

Sets the amplitude of the positive sync for the Y channel

dtg1_cbcr_blank(9:0): Cb/Cr channel blanking level amplitude control

{dtg1_cbcr_sync_msb 0x24(5:4) and dtg1_cbcr_sync1_lsb 0x20(7:0)} [10 0000 0000]

Sets the amplitude of the blanking level for the Cb and Cr channels

dtg1_cbcr_sync_low (9:0): Cb/Cr channel low sync level amplitude control

{dtg1_cbcr_sync_msb 0x24(3:2) and dtg1_cbcr_sync2_lsb 0x21(7:0)} [00 0000 0000]

Sets the amplitude of the negative sync and equalization/serration/broad pulses for the Cb and Cr channels

dtg1_cbcr_sync_high(9:0): Cb/Cr channel high sync level amplitude control

{dtg1_cbcr_sync_msb 0x24(1:0) and dtg1_cbcr_sync3_lsb 0x22(7:0)} [11 0000 0000]

Sets the amplitude of the positive sync for the Cb and Cr channels

dtg1_spec_a(7:0): Negative HSync width

{dtg1_spec_a 0x25(7:0)} [0010 1100] = [44d]

Width of negative excursion of tri-level (HDTV mode) or bi-level (SDTV mode) sync

dtg1_spec_b(7:0):	**End of active video to 0H**
{dtg1_spec_b 0x26(7:0)}	[0101 1000] = [88d]

Distance from end of active video to start of negative sync (SDTV mode) or to negative-to-positive transition of tri-level sync (HDTV mode)

dtg1_spec_c(7:0):	**Positive Hsync width (HDTV)/Equalization pulse (SDTV) width**
{dtg1_spec_c 0x27(7:0)}	[0010 1100] = [44d]

Width of positive excursion of tri-level (HDTV mode). Width of equalization pulses (SDTV mode)

dtg1_spec_d(8:0):	**Sync to active video(SDTV)/sync to broad pulse(HDTV)**
{dtg1_spec_deh_msb 0x2B(7) and dtg1_spec_d_lsb 0x28(7:0)}	[0 1000 0100] = [132d]

Distance from leading edge of Hsync to start of active video (SDTV mode) or from negative-to-positive transition of tri-level sync to start of broad pulse (HDTV mode)

dtg1_spec_d1(7:0):	**Center equalization pulse to active video (SDTV)**
{dtg1_spec_d1 0x29(7:0)}	[0000 0000]

Distance from equalization pulse at center of line to active video (SDTV mode)

dtg1_spec_e(8:0):	**Sync to active video (HDTV)/Color bar start (VESA)**
{dtg1_spec_deh_msb 0x2B(6) and dtg1_spec_e_lsb 0x2A(7:0)}	[0 1100 0000] = [192d]

Distance from negative-to-positive transition of tri-level sync to start of active video (HDTV mode). In case color bars are activated in VESA mode, this parameter specifies the start of the color bar with respect to the horizontal sync

dtg1_spec_h(9:0):	**Broad pulse duration (SDTV)**
{dtg1_spec_deh_msb 0x2B(1:0) and dtg1_spec_h_lsb 0x2C(7:0)}	[00 0000 0000]

Duration of broad pulse (SDTV mode)

dtg1_spec_i(11:0):	**Full-line broad pulse duration (SDTV)**
{dtg1_spec_i_msb 0x2D(3:0) and dtg1_spec_i_lsb 0x2E(7:0)}	[0000 0000 0000]

Duration of full-line broad pulse (SDTV mode)

dtg1_spec_k(10:0):	**End of active video to sync (SDTV)/end of broad pulse to sync (HDTV)**
{dtg1_spec_k_msb 0x30(2:0) and dtg1_spec_k_lsb 0x2F(7:0)}	[000 0101 1000] = [88d]

Distance from end of active video to leading edge of sync (SDTV) or from end of broad pulse to negative-to-positive transition of tri-level sync (HDTV)

dtg1_spec_k1(7:0):	**End of active video in first half of line to center equalization pulse (SDTV)**

{dtg1_spec_k1 0x31(7:0)} [00000000]

Distance from end of active video in first half of line to center equalization pulse for SDTV line type ACTIVE_NEQ

dtg1_spec_g(11:0): **1/2 of line length (SDTV)**

{dtg1_spec_g_msb 0x33(3:0) and dtg1_spec_g_lsb 0x32(7:0)} [0000 0101 1000] = [88d]

Half the line length. Only used in the calculations of SDTV line types.

dtg1_total_pixels(12:0): **Total pixels per line (SDTV/HDTV/VESA)**

{dtg1_total_pixels_msb 0x34(4:0) and dtg1_total_pixels_lsb 0x35(7:0)} [0 0101 0010 0000] = [1312d]

Total number of pixels per line. Used in all DTG modes.

dtg1_field_flip: **FID/F polarity select**

{dtg1_fieldflip_linecnt_msb 0x36(7)} [0]

0 : DTG is initialized to field1 at active VS edge when a 0 is received on FID signal or F bit

1 : DTG is initialized to field1 at active VS edge when a 1 is received on FID signal or F bit

dtg1_linecnt(10:0): **DTG start line number**

{dtg1_fieldflip_linecnt_msb 0x36(2:0) and dtg1_linecnt_lsb 0x37(7:0)} [000 0000 0001]

Sets the starting line number for the DTG when Vsync input or V-bit is asserted (vertical display control)

dtg1_on: **DTG on/off**

{dtg1_mode 0x38(7)} [1]

0 : DTG output held to dtg_y_blank value

1 : DTG on

dtg1_pass_through: **DTG pass-through**

{dtg1_mode 0x38(4)} [0]

0 : Video data blocked during certain line types

1 : Video data passed during certain line types

See DTG Line Types Overview (Section 4.7.3) for details.

dtg1_mode(3:0): **DTG mode selection**

{dtg1_mode 0x38(3:0)} [0110]

Selects the operation mode of the DTG according to the following table. Each setting is either an SDTV, HDTV or VESA format, as shown:

dtg1_mode	MODE
0000	ATSC mode 1080P (SMPTE 274M progressive) [HDTV]
0001	ATSC mode 1080I (SMPTE274M interlaced) [HDTV]
0010	ATSC mode 720P (SMPTE296M progressive) [HDTV]
0011	Generic mode for HDTV [HDTV]
0100	ATSC mode 480I (SDTV 525 lines interlaced) [SDTV]
0101	ATSC mode 480P (SDTV 525 lines progressive) [SDTV]
0110	VESA master [VESA]
0111	VESA slave [VESA]
1000	SDTV 625 interlaced [SDTV]
1001	Generic mode for SDTV [SDTV]
Others	[Null]

dtg1_frame_size(10:0): **Generic mode frame size**

{dtg1_frame_field_size_msb 0x39(6:4) and dtg1_framesize_lsb 0x3A(7:0)} [011 0000 0000]

Determines number of lines per frame when in generic mode

dtg1_field_size(10:0): **Generic mode field size**

{dtg1_frame_field_size_msb 0x39(2:0) and dtg1_fieldsize_lsb 0x3B(7:0)} [000 0010 0000]

Determines number of lines in field 1 when in generic mode. This number should be programmed higher than frame_size for progressive scan formats.

dtg1_vesa_cbar_size(7:0): **Color bar pattern, width**

{dtg1_vesa_cbar_size 0x3C(7:0)} [1000 0000]

Sets the width of each color bar in the color bar test pattern. This test pattern is only available when the DTG is in VESA mode.

5.1.6 DAC Control (Sub-Addresses 0x3D−0x40)

dac_i2c_cntl: **DAC I^2C control**

{dac_cntl_msb 0x3D(6)} [0]

0 : DAC normal operation

1 : DAC inputs are fixed to values of <dac_cntl> registers

dac1_cntl(9:0): **DAC1 input value**

{dac_cntl_msb 0x3D(5:4) and dac1_cntl_lsb 0x3E(7:0)} [00 0000 0000]

Direct input to G/Y DAC

dac2_cntl(9:0): **DAC2 input value**

{dac_cntl_msb 0x3D(3:2) and dac2_cntl_lsb 0x3F(7:0)} [00 0000 0000]

Direct input to B/Cb DAC

dac3_cntl(9:0): **DAC3 input value**

{dac_cntl_msb 0x3D(1:0) and dac3_cntl_lsb 0x40(7:0)} [00 0000 0000]

Direct input to R/Cr DAC

5.1.7 Clip/Scale/Multiplier Control (Sub-Addresses 0x41−0x4F)

csm_clip_gy_low(7:0): G/Y low clipping value

{csm_clip_gy_low 0x41(7:0)} [0100 0000]

Sets the value at which low end clipping occurs on G/Y channel, if clipping is enabled. Range is 0−255.

csm_clip_bcb_low(7:0): B/Cb low clipping value

{csm_clip_bcb_low 0x42(7:0)} [0100 0000]

Sets the value at which low end clipping occurs on B/Cb channel, if clipping is enabled. Range is 0−255.

csm_clip_rcr_low(7:0): R/Cr low clipping value

{csm_clip_rcr_low 0x43(7:0)} [0100 0000]

Sets the value at which low end clipping occurs on R/Cr channel, if clipping is enabled. Range is 0−255.

csm_clip_gy_high(7:0): G/Y high clipping value

{csm_clip_gy_high 0x44(7:0)} [0101 0011]

Sets the value at which high end clipping occurs on G/Y channel, if clipping is enabled.
High clip value = 1023-csm_clip_gy_high

csm_clip_bcb_high(7:0): B/Cb high clipping value

{csm_clip_bcb_high 0x45(7:0)} [0011 1111]

Sets the value at which high end clipping occurs on B/Cb channel, if clipping is enabled.
High clip value = 1023−csm_clip_bcb_high

csm_clip_rcr_high(7:0): R/Cr high clipping value

{csm_clip_rcr_high 0x46(7:0)} [0011 1111]

Sets the value at which high end clipping occur on R/Cr channel, if clipping is enabled.
High clip value = 1023−csm_clip_rcr_highs

csm_shift_gy(7:0): G/Y shift value

{csm_shift_gy 0x47(7:0)} [0100 0000]

Value that G/Y data is shifted downwards. Range 0−255. Note: it is possible to shift the data so much that a roll over condition occurs.

csm_shift_bcb(7:0): B/Cb shift value

{csm_shift_bcb 0x48(7:0)} [0100 0000]

Value that B/Cb data is shifted downwards. Range: 0−255. Note: It is possible to shift the data so much that a roll over condition occurs.

csm_shift_rcr(7:0): R/Cr shift value

{csm_shift_rcr 0x49(7:0)} [0100 0000]

Value that B/Cb data is shifted downwards. Range: 0−255. Note: It is possible to shift the data so much that a roll over condition occurs.

csm_mult_gy_on: **G/Y scaling on/off**

{csm_gy_cntl_mult_msb 0x4A(7)} [0]

0 : Scaling for G/Y channel off

1 : Scaling for G/Y channel on

csm_shift_gy_on: **G/Y shifting on/off**

{csm_gy_cntl_mult_msb 0x4A(6)} [0]

0 : Shifting for G/Y channel off

1 : Shifting for G/Y channel on

csm_gy_high_clip_on: **G/Y high-end clipping on/off**

{csm_gy_cntl_mult_msb 0x4A(5)} [0]

0 : G/Y data clipping at high end off

1 : G/Y data clipping at high end on

csm_gy_low_clip_on: **G/Y low-end clipping on/off**

{csm_gy_cntl_mult_msb 0x4A(4)} [0]

0 : G/Y data clipping at low end off

1 : G/Y data clipping at low end on

csm_of_cntl: **CSM overflow control**

{csm_gy_cntl_mult_msb 0x4A(3)} [1]

Controls overflow protection of the CSM multiplier

0 : Overflow protection off

1 : Overflow protection on

Numerical format of the CSM mult registers:

The 11-bit value is a binary weighted value in the range 0−1.999.

Thus: csm_mult_<gy,rcr,bcb>(10:0) = [(multiplier in range 0..1.999)/1.999] × 2047.

csm_mult_gy(10:0): **G/Y scaling value**

{csm_gy_cntl_mult_msb 0x4A(2:0) [000 0000 0000]
and
csm_mult_gy_lsb 0x4C(7:0)}

Multiplication factor for G/Y channel in CSM. Range: 0−1.999.

Note: it is possible to scale the input so much that a rollover occurs.

csm_mult_bcb(10:0): **B/Cb scaling value**

{csm_mult_bcb_rcr_msb 0x4B(6:4) [000 0000 0000]
and
csm_mult_bcb_lsb 0x4D(7:0)}

Multiplication factor for B/Cb channel in CSM. Range: 0−1.999.

Note: it is possible to scale the input so much that a rollover occurs.

csm_mult_rcr(10:0): **R/Cr scaling value**

{csm_mult_bcb_rcr_msb 0x4B(2:0) and csm_mult_rcr_lsb 0x4E(7:0)} [000 0000 0000]

Multiplication factor for R/Cr channel in CSM. Range: 0−1.999.

Note: it is possible to scale the input so much that a rollover occurs.

csm_mult_rcr_on: **R/Cr scaling on/off**

{csm_rcr_bcb_cntl 0x4F(7)} [0]

0 : Scaling for R/Cr channel off

1 : Scaling for R/Cr channel on

csm_mult_bcb_on: **B/Cb scaling on/off**

{csm_rcr_bcb_cntl 0x4F(6)} [0]

0 : Scaling for B/Cb channel of

1 : Scaling for B/Cb channel on

csm_shift_rcr_on: **R/Cr shifting on/off**

{csm_rcr_bcb_cntl 0x4F(5)} [0]

0 : Shifting for R/Cr channel off

1 : Shifting for R/Cr channel on

csm_shift_bcb_on: **B/Cb shifting on/off**

{csm_rcr_bcb_cntl 0x4F(4)} [0]

0 : Shifting for B/Cb channel off

1 : Shifting for B/Cb channel on

csm_rcr_high_clip_on: **R/Cr high-end clipping on/off**

{csm_rcr_bcb_cntl 0x4F(3)} [0]

0 : R/Cr data clipping at high end off

1 : R/Cr data clipping at high end on

csm_rcr_low_clip_on: **R/Cr low-end clipping on/off**

{csm_rcr_bcb_cntl 0x4F(2)} [0]

0 : R/Cr data clipping at low end off

1 : R/Cr data clipping at low end on

csm_bcb_high_clip_on: **B/Cb high-end clipping on/off**

{csm_rcr_bcb_cntl 0x4F(1)} [0]

0 : B/Cb data clipping at high end off

1 : B/Cb data clipping at high end on

csm_bcb_low_clip_on: **B/Cb low-end clipping on/off**

{csm_rcr_bcb_cntl 0x4F(0)} [0]

0 : B/Cb data clipping at low end off

1 : B/Cb data clipping at low end on

5.1.8 Display Timing Generator Control, Part 2 (Sub-Addresses 0x50−0x82)

dtg2_bp<n>(10:0): **breakpoint<n> line number**

{see register map table} [000 0000 0000]

DTG outputs line type dtg2_linetype<n> until line number of dtg2_bp<n+1> is reached. (n = 1..16)

dtg2_linetype<n>(3:0): **Line type for dtg2_bp<n>**

{see register map table} [0000]

The DTG outputs a line format corresponding to the table below until the next breakpoint line number is reached. (n = 1..16)

LINE TYPE	MODE
0000	ACTIVE_VIDEO
0001	FULL_NTSP
0010	FULL_BTSP
0011	NTSP_NTSP
0100	BTSP_BTSP
0101	NTSP_BTSP
0110	BTSP_NTSP
0111	ACTIVE_NEQ
1000	NSP_ACTIVE
1001	FULL_NSP
1010	FULL_BSP
1011	FULL_NEQ
1100	NEQ_NEQ
1101	BSP_BSP
1110	BSP_NEQ
1111	NEQ_BSP

dtg2_hlength(9:0): **HS_OUT duration**

{dtg2_hlength_lsb_hdly_msb 0x71(7:6) and dtg2_hlength_lsb 0x70(7:0)} [00 0110 0000]

Sets the duration of the HS_OUT output signal

dtg2_hdly(12:0): **HS_OUT delay**

{dtg2_hlength_lsb_hdly_msb 0x71(4:0) and dtg2_hdly_lsb 0x72(7:0)} [0 0000 0000 0010]

Sets the pixel value that the HS_OUT signal is asserted on.

Note: when programmed to a value higher than the total number of pixels per line, there will be no HS_OUT output.

dtg2_vlength1(9:0): **VS_OUT duration, field 1**

{dtg2_vlength1_msb_vdly1_msb 0x74(7:6) and dtg2_vlength1_lsb 0x73(7:0)} [00 0000 0011]

Sets the duration of the VS_OUT output signal during progressive scan video modes or during the vertical blank interval of field 1 in interlaced video modes.

dtg2_vdly1(10:0): **VS_OUT delay, field 1**

{dtg2_vlength1_msb_vdly1_msb 0x74(2:0) and dtg2_vdly1_lsb 0x75(7:0)} [000 0000 0011]

Sets the line number that the VS_OUT signal is asserted on for progressive video modes or for field 1 of interlaced video modes.

Note: when programmed to a value higher than the total number of lines per frame, there is no VS_OUT output.

dtg2_vlength2(9:0): **VS_OUT duration, field 2**

{dtg2_vlength2_msb_vdly2_msb 0x77(7:6) and dtg2_vlength2_lsb 0x76(7:0)} [00 0000 0000]

Sets the duration of the VS_OUT output signal during the vertical blank interval of field 2 in interlaced video modes. In progressive video modes, this register must be set to all 0.

dtg2_vdly2(10:0): **VS_OUT delay, field 2**

{dtg2_vlength2_msb_vdly2_msb 0x77(2:0) and dtg2_vdly2_lsb 0x78(7:0)} [111 1111 1111]

Sets the line number that the VS_OUT signal is asserted on for field 2 of interlaced scan video modes. For progressive scan video modes, this register must be set to all 1.

dtg2_hs_in_dly(12:0): **DTG horizontal delay**

{dtg2_hs_in_dly_msb 0x79(4:0) and dtg2_hs_in_dly_lsb 0x7A(7:0)} [0 0000 0011 1101]

Sets the number of pixels that the DTG startup is horizontally delayed with respect to HS input for dedicated timing modes or EAV input for embedded timing modes.

Note: It is possible to delay startup past the end of a line when this delay is programmed higher than the total number of pixels per line.

dtg2_vs_in_dly(10:0): **DTG vertical delay**

{dtg2_vs_in_dly_msb 0x7B(2:0) and dtg2_vs_in_dly_lsb 0x7C(7:0)} [000 0000 0011]

Sets the number of lines that the DTG startup is vertically delayed with respect to VS input for dedicated timing modes or the line counter value for embedded timing.

Note: It is possible to delay startup past the end of a frame when this delay is programmed higher than the total number of lines per frame.

dtg2_pixel_cnt(15:0): **Pixel count readback**

{dtg2_pixel_cnt_msb 0x7D(7:0) and dtg2_pixel_cnt_lsb 0x7E(7:0)}

Reports the number of clock 1x rising edges between consecutive Hsync input pulses

dtg2_ip_fmt: **Interlaced/progressive-scan indicator**

{dtg2_line_cnt_msb 0x7F(7)}

Indicates whether current video frame is progressive (0) or interlaced (1)

dtg2_line_cnt(10:0): **Line count readback**

{dtg2_lined_cnt_msb 0x7F(2:0) and dtg2_line_cnt_lsb 0x80(7:0)}

Reports the number of Hsync input pulses between consecutive dtg_start signals (i.e., over one frame period)

dtg2_fid_de_cntl: **FID (field-ID)/DE (data enable)input selection for FID terminal**

{dtg2_cntl 0x82(7)} [0]

Controls interpretation of signal on FID terminal

0 : Signal interpeted as FieldID

1 : If the DTG is programmed to the VESA mode, the FID pin becomes a data-enable input pin. Data enable is assumed high during the active video window, and low outside this area. This is compatible with the DE signal from TI DVI receivers. Data is passed through the THS8200 only when data enable is high. Otherwise, the input data is overridden by the THS8200 internally programmed blanking value. If the DTG is programmed in the SDTV or HDTV video mode with dedicated timing signals, a 1 in this register location causes the THS8200 to generate an internal FieldID value from the relative alignment of Hsync and Vsync inputs, rather than using the signal on the FID input pin (which is ignored). This is for EIA-861 compliant operation for video-over-DVI 1.0 (with HDCP) where there is no dedicated FID signal available but the even/odd field ID is determined from Hsync/Vsync alignment.

dtg2_rgb_mode_on: **RGB/YPbPr mode selection**

{dtg2_cntl 0x82(6)} [1]

This selection affects the relative blank vs video level position: on R,G,B, and Y channels an offset is added to the DAC outputs

0 : YPbPr mode (blanking at bottom range for Y – mid-range for Pb, Pr channels)

1 : RGB mode (blanking at bottom ranges for all channels)

dtg2_embedded_timing: **Video sync input source**

{dtg2_cntl 0x82(5)} [0]

0 : Timing of video input bus is derived from HS, VS, and FID dedicated inputs

1 : Timing of video input bus is assumed embedded in video data using SAV/EAV code sequences.

dtg2_vsout_pol: **VS_OUT polarity**

{dtg2_cntl 0x82(4)} [1]

0 : Positive polarity

1 : Negative polarity

dtg2_hsout_pol: **HS_OUT polarity**

{dtg2_cntl 0x82(3)} [1]

0 : Negative polarity

1 : Positive polarity

dtg2_fid_pol: **FID polarity**

{dtg2_cntl 0x82(2)} [1]

0 : Negative polarity

1 : Positive polarity

dtg2_vs_pol:	**VS_IN polarity**
{dtg2_cntl 0x82(1)}	[1]
0 : Negative polarity	
1 : Positive polarity	

dtg2_hs_pol:	**HS_IN polarity**
{dtg2_cntl 0x82(0)}	[1]
0 : Negative polarity	
1 : Positive polarity	

misc_ppl(15:0):	**HS high**
{misc_ppl_msb 0x87(7:0) and misc_ppl_lsb 0x86(7:0)}	
Reports the number of clock cycles HS was held high	

misc_lpf(15:0):	**VS high**
{misc_lpf_msb 0x89(7:0) and misc_lpf_lsb 0x88(7:0)}	
Reports the number of HS counts that VS was held high.	

5.1.9 CGMS Control (Sub-Addresses 0x83−0x85)

cgms_en:	CGMS enable
{cgms_cntl_header 0x83(6)}	[0]
0 : No CGMS data inserted	
1 : CGMS data inserted on line 41 in SDTV mode	

cgms_header:	CGMS header
{cgms_cntl_header 0x83(5:0)}	[00 0000]

cgms_payload(13:0):	CGMS payload
{cgms_payload_msb 0x84(5:0) and cgms_payload_lsb 0x85(7:0)}	[00 0000 0000 0000]
CGMS payload data	

5.2 THS8200 Preset Mode Line Type Definitions

The following are the (line type, breakpoint) combinations that are preprogrammed when selecting the corresponding DTG preset setting.

5.2.1 SMPTE_274P (1080P)

Breakpoints	**Line Type**
6	FULL_BTSP
42	FULL_NTSP
1122	ACTIVE_VIDEO
1126	FULL_NTSP
frame_size = 10001100101; 1125d	
field_size = 11111111111; not needed	

5.2.2 274M Interlaced (1080I)

Breakpoints	Line Type
6	BTSP_BTSP
7	NTSP_NTSP
21	FULL_NTSP
561	ACTIVE_VIDEO
563	FULL_NTSP
564	NTSP_BTSP
568	BTSP_BTSP
569	BTSP_NTSP
584	FULL_NTSP
1124	ACTIVE_VIDEO
1126	FULL_NTSP

frame_size = 10001100101; 1125d

field_size = 01000110011; 563d

5.2.3 296M Progressive (720P)

Breakpoints	Line Type
6	FULL_BTSP
26	FULL_NTSP
746	ACTIVE_VIDEO
751	FULL_NTSP

frame_size = 01011101110; 750d

field_size = 11111111111; not needed

5.2.4 SDTV 525 Interlaced Mode

Breakpoints	Line Type
4	NEQ_NEQ
7	BSP_BSP
10	NEQ_NEQ
20	FULL_NSP
263	ACTIVE_VIDEO
264	ACTIVE_NEQ
266	NEQ_NEQ
267	NEQ_BSP
269	BSP_BSP
270	BSP_NEQ
272	NEQ_NEQ
273	FULL_NEQ
282	FULL_NSP

283	NSP_ACTIVE
526	ACTIVE_VIDEO

frame_size = 1000001101; 525d

field_size = 00100000111; 263d

5.2.5 SDTV 525 Progressive Mode

Breakpoints	Line Type
10	FULL_NSP
16	FULL_BSP
46	FULL_NSP
526	ACTIVE_VIDEO

frame_size = 01000001101; 525d

field_size = 11111111111; not needed

5.2.6 SDTV 625 Interlaced Mode

Breakpoints	Line Type
3	BSP_BSP
4	BSP_NEQ
6	NEQ_NEQ
23	FULL_NSP
24	NSP_ACTIVE
311	ACTIVE_VIDEO
313	NEQ_NEQ
314	NEQ_BSP
316	BSP_BSP
318	NEQ_NEQ
319	FULL_NEQ
336	FULL_NSP
623	ACTIVE_VIDEO
624	ACTIVE_NEQ
626	NEQ_NEQ

frame_size = 01001110001; 625d

field_size = 00100111000; 312d

6 Application Information

6.1 Video vs Computer Graphics Application

THS8200 is a highly integrated and flexible universal analog component video/graphics generator that can be used in any application requiring D/A conversion of video/graphics signals.

In a typical video application (e.g., DVD player, set-top box), the THS8200 receives its input from an MPEG decoder or media processor engine and converts the signal into the analog domain, thereby generating the correct timing/frame format for the selected format.

Its ITU-R.BT656 output port could be used to connect to an NTSC/PAL video encoder, such as the Texas Instruments TVP6000, for regular composite/S-video output.

Note that because the DAC speed is rated up to 205 MSPS, all popular SDTV and HDTV formats, including 1080I and 720P, are supported in both 1× and 2× interpolated modes. The 1080P is supported at the 1× rate.

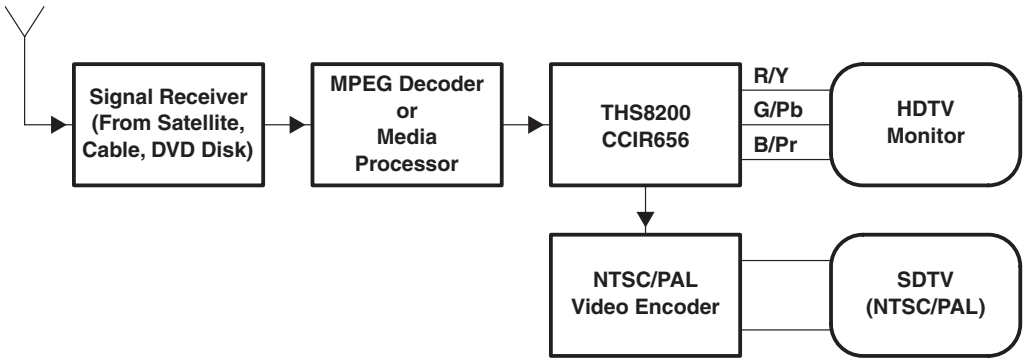


Figure 6-1. Typical Video Application

Because of its programmable Hsync/Vsync outputs, the on-chip support for RGB as well as YCbCr color spaces and its internal color space conversion circuit, and the DAC operational speed of 205 MSPS, all PC graphics formats are supported as well, up to UXGA at 75 Hz. Video interpolation is now bypassed so that the full 205 MSPS can be used for the 1× pixel clock.

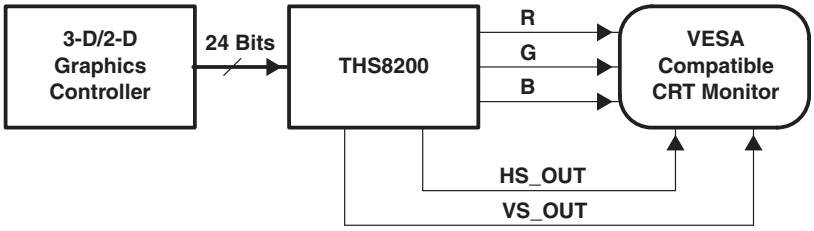


Figure 6-2. Computer Graphics Application

6.2 DVI to Analog YPbPr/RGB Application

Together with a DVI receiver, this device forms a two-chip solution to convert video or graphics formats sent over a DVI interface to an analog RGB or YPbPr format using embedded composite sync or separate Hsync, Vsync. THS8200 connects gluelessly to a DVI receiver using its data input bus and HS_IN and VS_IN terminals. TI DVI 1.0 (with HDCP) receivers provide a data enable (DE) signal that is high during

the active video window. The THS8200 can be configured to interpret this DE signal on its FID terminal to automatically insert a user-programmable blanking-level amplitude outside the active video window on its analog outputs; this blanking level can be correctly positioned for either RGB or YPbPr analog outputs. The user can optionally perform color space conversion in the THS8200 and adjust offset and gain ranges through the device's CSM block.

When sending (interlaced) video over DVI, the EIA-861 specification describes a method to derive the fieldID signal—not directly available from a DVI1.0 (with HDCP) receiver—from the relative alignment of the Hsync and Vsync signals. The THS8200 can be configured to derive internally the correct even/odd field identification from Hsync/Vsync alignment according to this specification, instead of using the FieldID signal on its FID input terminal. This avoids the need for additional glue logic in a DVI application.

6.3 Master vs Slave Timing Modes

In slave timing mode, the THS8200 output display timing is synchronized to the video data source. Display timing output signals are based on input sync signals, either fed to the device on the dedicated Hsync, Vsync, and FieldID (HS_IN, VS_IN, and FID) input terminals or based on SAV/EAV codes embedded in the input video data.

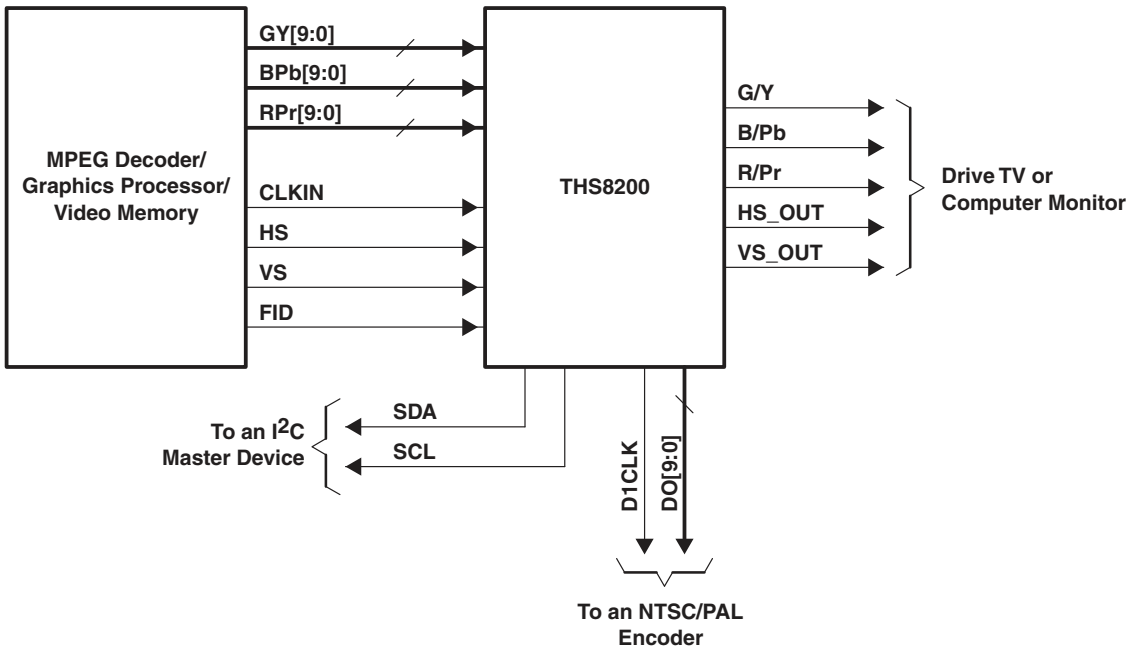


Figure 6-3. Slave Operation Mode of THS8200

In master timing mode, the THS8200 generates two sets of output synchronization signals.

- HS_IN and VS_IN now become output signals to the video source (FID unused).
- HS_OUT and VS_OUT are still output signals to display device.

The intended purpose is that THS8200 requests video data from a source that requires external timing, such as video memory.

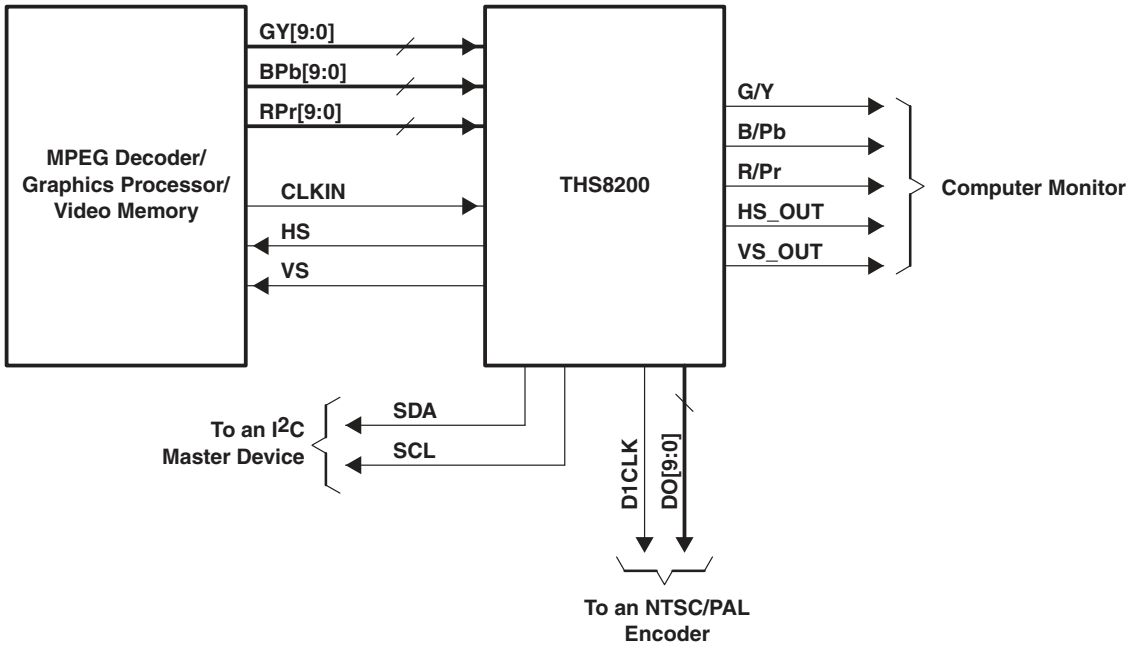


Figure 6-4. Master Operation Mode of THS8200

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted) (1)

			VALUE	UNIT
	Supply voltage range	AV_{DD} to AV_{SS}, VDD_IO to GND_IO	−0.5 to 4.5	V
		DV_{DD} to DV_{SS}, VDD_DLL to DVSS	−0.5 to 2.5	
	Digital input voltage range to DV_{SS}		−0.5 to VDD_IO + 0.5	V
T_A	Operating free-air temperature range		−40 to 85	°C
T_{stg}	Storage temperature range		−55 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

Over operating free-air temperature range, T_A

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
POWER SUPPLY						
Supply voltage	AV_{DD}		3	3.3	3.6	V
	DV_{DD}, VDD_DLL		1.65	1.8	2	
	VDD_IO		1.65	1.8/3.3	3.6	
DIGITAL AND REFERENCE INPUTS						
V_{IH}	High-level input voltage	VDD_IO = 1.8 V	0.95		VDD_IO	V
		VDD_IO = 3.3 V	2.3		VDD_IO	
V_{IL}	Low-level input voltage	VDD_IO = 1.8 V	DV_{SS}		0.4	V
		VDD_IO = 3.3 V	DV_{SS}		1.15	
f_{clk}	Clock frequency		10		205	MHz
$t_{w(CLKH)}$	Pulse duration, clock high		40%		60%	
$t_{w(CLKL)}$	Pulse duration, clock low		40%		60%	
R_{FS}	FSADJ resistor	V_{OC} = 700 mV		2.99		kΩ
		V_{OC} = 1 V		2.08		

7.3 ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
IAV_{DD}	Operating analog supply current	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, VDD_DLL = 1.8 V, VDD_IO = 3.3 V, CLK = 80 MHz	Video + no bias (700 mV)		94	98	mA
			Video + bias (1.05 V)		94	98	
			Generic + no bias (1.25 V)		162	170	
		AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, VDD_DLL = 1.8 V (DLL bypassed), VDD_IO = 1.8 V, CLK = 200 MHz	Video + no bias (700 mV)		94	98	
			Video + bias (1.05 V)		94	98	
			Generic + no bias (1.25 V)		162	170	
IDV_{DD}	Operating digital supply current	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, VDD_DLL = 1.8 V, VDD_IO = 3.3 V, CLK = 80 MHz	Video + no bias (700 mV)		38	45	mA
			Video + bias (1.05 V)		38	45	
			Generic + no bias (1.25 V)		38	45	
		AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, VDD_DLL = 1.8 V (DLL bypassed), VDD_IO = 1.8 V, CLK = 200 MHz	Video + no bias (700 mV)		89	95	
			Video + bias (1.05 V)		89	95	
			Generic + no bias (1.25 V)		89	95	
IVDD_IO	Operating IO supply current	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, VDD_DLL = 1.8 V, VDD_IO = 3.3 V, CLK = 80 MHz	Video + no bias (700 mV)		1.7	2.7	mA
			Video + bias (1.05 V)		1.7	2.7	
			Generic + no bias (1.25 V)		1.7	2.7	
		AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, VDD_DLL = 1.8 V (DLL bypassed), VDD_IO = 1.8 V, CLK = 200 MHz	Video + no bias (700 mV)		1.7	2.7	
			Video + bias (1.05 V)		1.7	2.7	
			Generic + no bias (1.25 V)		1.7	2.7	
IVDD_DLL	Operating DLL supply current	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, VDD_DLL = 1.8 V, VDD_IO = 3.3 V, CLK = 80 MHz	Video + no bias (700 mV)		4.9	5.6	mA
			Video + bias (1.05 V)		4.9	5.6	
			Generic + no bias (1.25 V)		4.9	5.6	
		AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, VDD_DLL = 1.8 V (DLL bypassed), VDD_IO = 1.8 V, CLK = 200 MHz	Video + no bias (700 mV)		4.9	5.6	
			Video + bias (1.05 V)		4.9	5.6	
			Generic + no bias (1.25 V)		4.9	5.6	
P_D	Power disspiation	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, VDD_DLL = 1.8 V, VDD_IO = 3.3 V, CLK = 80 MHz	Video + no bias (700 mV)		398	430	mW
			Video + bias (1.05 V)		398	430	
			Generic + no bias (1.25 V)		641	660	
		AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, VDD_DLL = 1.8 V (DLL bypassed), VDD_IO = 1.8 V, CLK = 200 MHz	Video + no bias (700 mV)		489	500	
			Video + bias (1.05 V)		489	500	
			Generic + no bias (1.25 V)		700	735	
DIGITAL INPUTS - DC CHARACERISTICS							
I_{IH}	High-level input current	VDD_IO = 3.3 V, Digital inputs and CLK at 0 V for I_{IL}; Digital inputs and CLK at 3.6 V for I_{IH}				1	µA
I_{IL}	Low-level input current					−1	µA
$I_{IL(CLK)}$	Low-level input current, CLK					1	µA
$I_{IH(CLK)}$	High-level input current, CLK					−1	µA
C_I	Input capacitance	T_A = 25°C			5		pF
t_s	GY, RCr, BCb data inputs setup time	VDD_IO = 1.8 V		1.5			nA
		VDD_IO = 3.3 V		1.5			

(1) T_A = 25°C for typical parameters.

ELECTRICAL CHARACTERISTICS *(continued)*

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_H	GY, RCr, BCb data inputs hold time	VDD_IO = 1.8 V		0.5			nA
		VDD_IO = 3.3 V		0.5			
t_s	HS_IN, VS_IN, FID inputs setup time	VDD_IO = 3.3 V(2)		1.5			nA
t_H	HS_IN, VS_IN, FID inputs hold time	VDD_IO = 3.3 V(2)		0.5			nA
$t_{d(D)}$	Digital process delay(3)	10-bit/20-bit 4:2:2 with CSM, CSC, 2x interpolation active			73(4)		pixels
		30-bit 4:4:4			33(4)		
		VESA clock mode (DLL, CSM, CSC, FIRs bypassed)			9		
ANALOG (DAC) OUTPUTS							
	DAC resolution			10 (11 bit internal)	10 (11 bit internal)		bits
INL	Integral nonlinearity	Best-fit VDD_IO = 3.3 V, CLK = 500 kHz	Video (0.7 + 0.35 V bias)	–3		3	LSB
			Generic (1.25 + 0 V bias)	–10		10	
DNL	Differential nonlinearity	VDD_IO = 3.3 V, CLK = 500 kHz	Video (0.7 + 0.35 V bias)		0.2/−0.3	1/−1	LSB
			Generic (1.25 + 0 V bias)		1/−1	1/−1	
PSRR	Power supply ripple rejection ratio of DAC output (full scale)	f = dc to 100 kHz(5)			42		dB
XTALK	Crosstalk between channels(6)	CLK = 205 MHz, -1 dB sine wave applied to active channels, offset bias applied to all channels when turned on, 37.5 Ω load on all channels	1 MHz sine wave, offset bias off		49		dB
			1 MHz sine wave, offset bias on		42		
			10 MHz sine wave, offset bias off		49		
			10 MHz sine wave, offset bias on		42		
			30 MHz sine wave, offset bias off		48		
			30 MHz sine wave, offset bias on		40.5		
K_{IMBAL}	Imbalance between DACs	CLK = 80 MHz(7)				±2%	
V_{OC}	DAC output compliance voltage (video only)	R_L = 37.5 Ω(8)	Video mode (bias offset can be added)		0.7	0.72	V
			Generic mode (bias offset cannot be added)		1.25	1.3	
C_O	DAC output capacitance (pin capacitance)				5		pF
t_{ri}	DAC output current rise time	10 to 90% of full-scale, CLK = 80 MHz			3.5	4.2	ns

(2) The HS_IN, VS_IN, and FID input setup/hold times are valid for 3.3-V I/O operation only. These sync inputs are not recommended for use with 1.8-V I/O logic levels.
(3) Defined as the delay on Y pixel data, starting from the rising edge of CLKIN, until the clock period.
(4) CSC contribution: 8 pixels, CSM contribution: 1 pixel, 2x interpolation filter contribution: 18 pixels
(5) PSRR is defined as 20*log (ripple voltage at DAC output/ripple voltage at AVDD input). Limits from characterization only.
(6) Crosstalk spec applies to each possible pair of the 3 DAC outputs. Limit from characterization only.
(7) The imbalance between DACs applies to all possible pairs of the three DACs.
(8) Nominal values at $R_{FS} = R_{FS(nom)}$, see Figure 7-12 . Limit from characterization only. Excludes bias offset.

ELECTRICAL CHARACTERISTICS *(continued)*

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{fi}	DAC output current fall time	10 to 90% of full-scale, CLK = 80 MHz		3.5	4.2	ns
t_d	Analog output delay	Measured from falling edge of CLKIN to 50% of full-scale transition(9)		6.5		ns
t_{sa}	Analog output settling time	Measured from 50% of full scale transition on output to output settling, within 2%(10)		6.6		ns
SFDR	Spurious-free dynamic range	1 MHz, −1 dB FS digital sine input		–55		dB
		10 MHz, −1 dB FS digital sine input		–43		
BW	Bandwidth (3 dB)			90		MHz
E_{glitch}	Glitch energy	Full-scale code transition at 205 MSPS		25		pVs

(9) This value excludes the digital process delay, $t_{D(D)}$. Limit from characterization only. Data is clocked in on the rising edge of CLKIN. Analog outputs become available on the falling edge of CLKIN.
(10) Limit from characterization only.

7.4 Power Requirements

7.4.1 Power for 700-mV DAC Output Compliance + 350-mV Bias at AVDD = 3.3 V, DVDD = 1.8 V, VDD_IO = 3.3 V, VDD_DLL = 3.3 V, 1-MHz Tone on All Channels

f (MHz)	POWER (mW), DLL BYPASSED	POWER (mW), DLL USED	IAVDD (mA)	IDVDD (mA)	IVDD_IO (mA)	IVDD_DLL (mA)
20	329.91	332.88	93.2	10.4	1.1	0.9
30	338.52	351.72	93.2	15	1.2	4
80	382.47	399.63	93.2	38.5	1.7	5.2
160	450.51		93.2	75.2	2.3	
200	476.01		93.2	89	2.5	

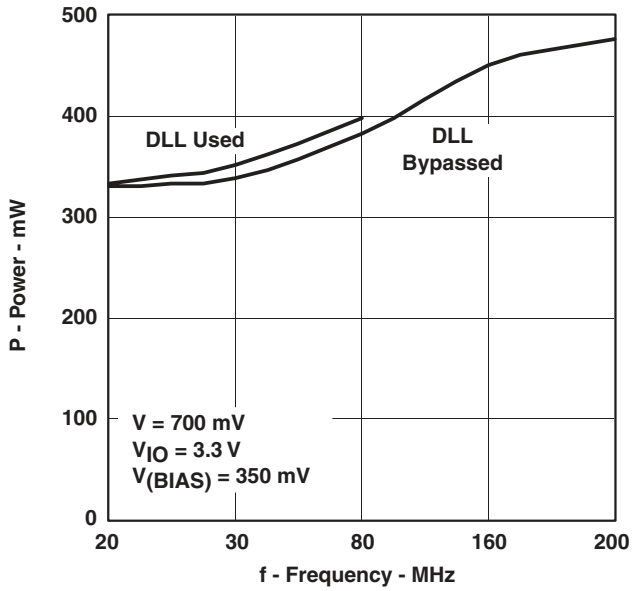


Figure 7-1. POWER vs FREQUENCY

7.4.2 Power for 700-mV DAC Output Compliance + 350-mV Bias at AVDD = 3.3 V,

DVDD = 1.8 V, VDD_IO = 1.8 V, VDD_DLL = 3.3 V, 1-MHz Tone on All Channels

f (MHz)	POWER (mW), DLL BYPASSED	POWER (mW), DLL USED	IAVDD (mA)	IDVDD (mA)	IVDD_IO (mA)	IVDD_DLL (mA)
20	328.26	331.23	93.2	10.4	1.1	0.9
30	336.72	349.92	93.2	15	1.2	4
80	379.92	397.08	93.2	38.5	1.7	5.2
160	447.06		93.2	75.2	2.3	
200	472.26		93.2	89	2.5	

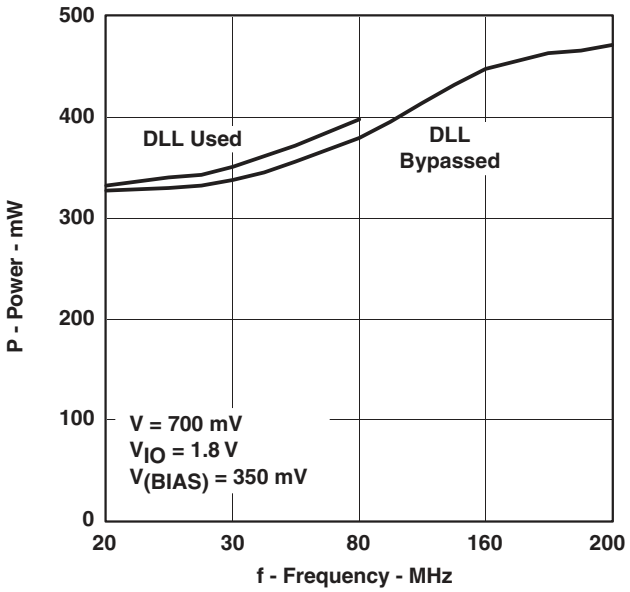


Figure 7-2. POWER vs FREQUENCY

7.4.3 Power for 1.25-V Output Compliance Without Bias at AVDD = 3.3 V, DVDD = 1.8 V, VDD_IO = 3.3 V, VDD_DLL = 3.3 V, 1-MHz Tone on All Channels

f (MHz)	POWER (mW), DLL BYPASSED	POWER (mW), DLL USED	IAVDD (mA)	IDVDD (mA)	IVDD_IO (mA)	IVDD_DLL (mA)
20	556.95	559.92	162	10.4	1.1	0.9
30	565.56	578.76	162	15	1.2	4
80	609.51	626.67	162	38.5	1.7	5.2
160	677.55		162	75.2	2.3	
200	703.05		162	89	2.5	

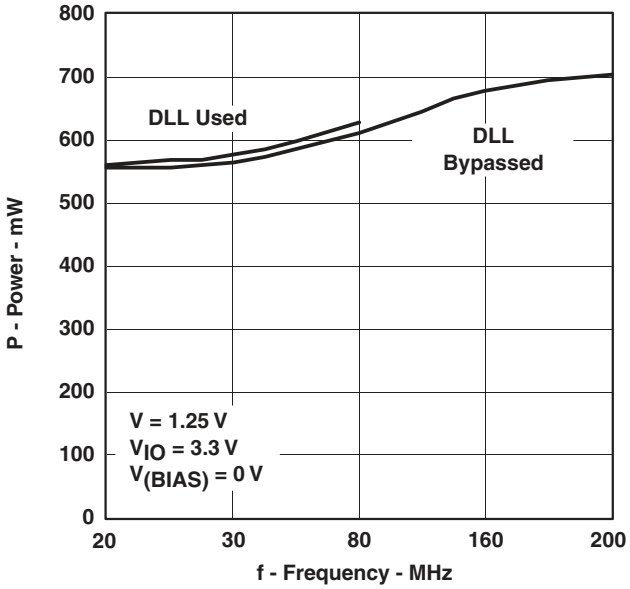


Figure 7-3. POWER vs FREQUENCY

7.4.4 Power for 1.25-V Output Compliance Without Bias at AVDD = 3.3 V, DVDD = 1.8 V, VDD_IO = 1.8 V, VDD_DLL = 3.3 V, 1-MHz Tone on All Channels

f (MHz)	POWER (mW), DLL BYPASSED	POWER (mW), DLL USED	IAVDD (mA)	IDVDD (mA)	IVDD_IO (mA)	IVDD_DLL (mA)
20	555.30	558.27	162	10.4	1.1	0.9
30	563.76	576.96	162	15	1.2	4
80	606.96	624.12	162	38.5	1.7	5.2
160	674.10		162	75.2	2.3	
200	699.30		162	89	2.5	

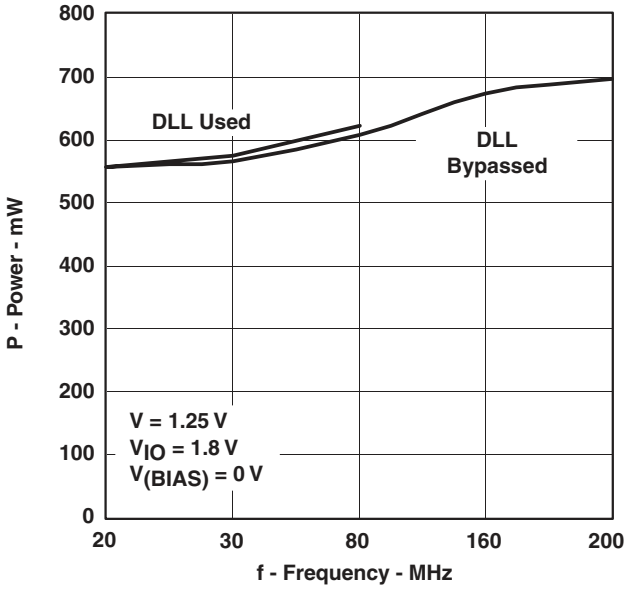


Figure 7-4. POWER vs FREQUENCY

7.5 Nonlinearity

7.5.1 Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) for 700 mV Without Bias

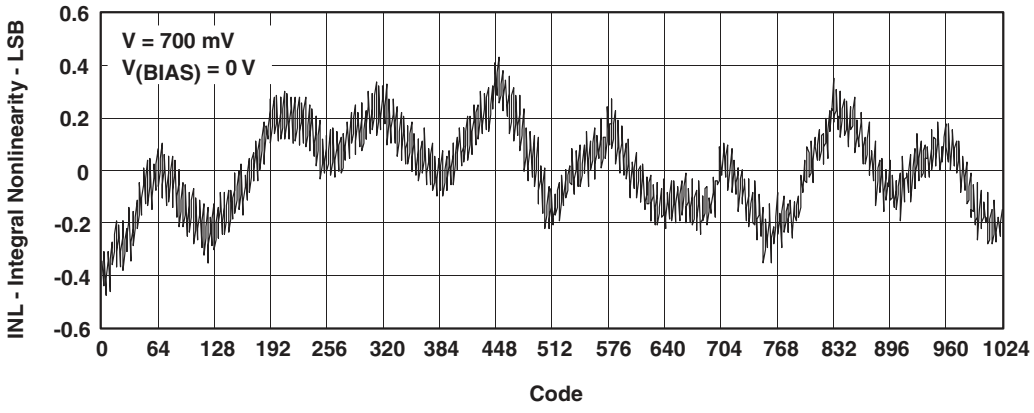


Figure 7-5. INTEGRAL NONLINEARITY vs CODE

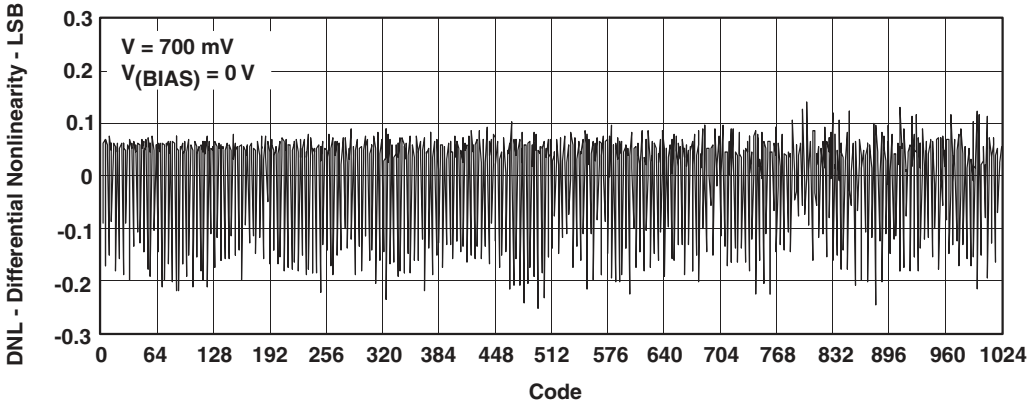


Figure 7-6. DIFFERENTIAL NONLINEARITY vs CODE

7.5.2 Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) for 700 mV + 350-mV Bias

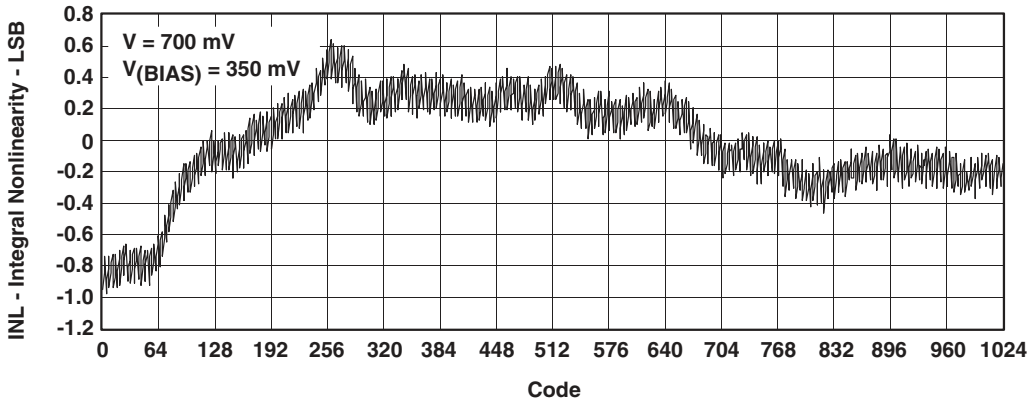


Figure 7-7. INTEGRAL NONLINEARITY vs CODE

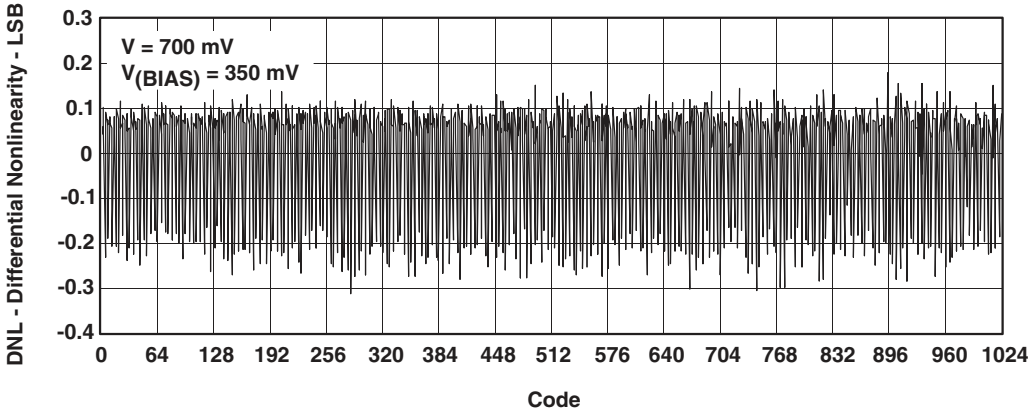


Figure 7-8. DIFFERENTIAL NONLINEARITY vs CODE

7.5.3 Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) for 1.25 V Without Bias

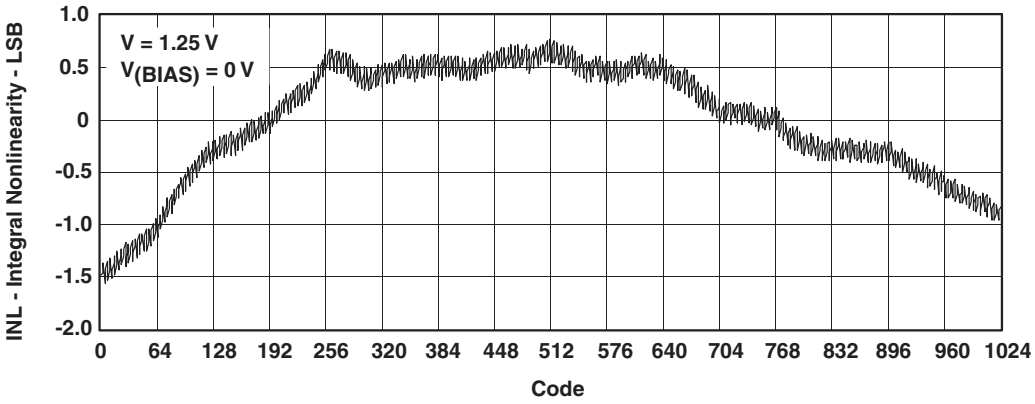


Figure 7-9. INTEGRAL NONLINEARITY vs CODE

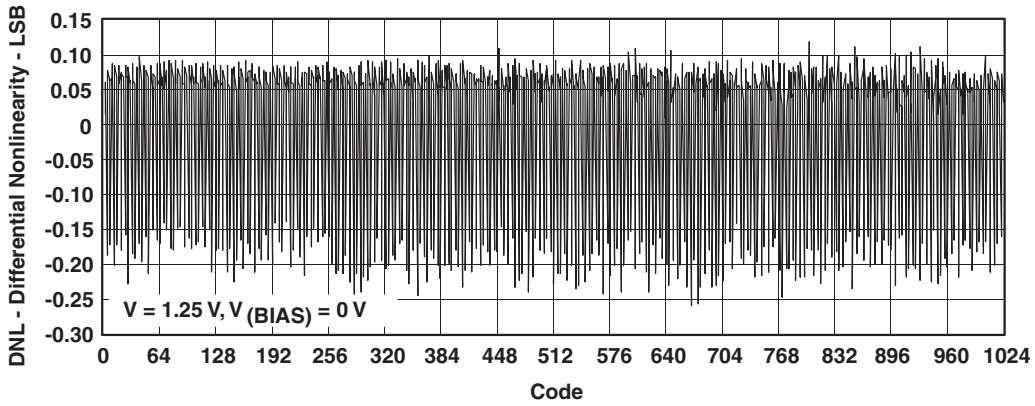


Figure 7-10. DIFFERENTIAL NONLINEARITY vs CODE

7.6 Analog Output Bandwidth (sinx/x corrected) at f_S = 205 MSPS

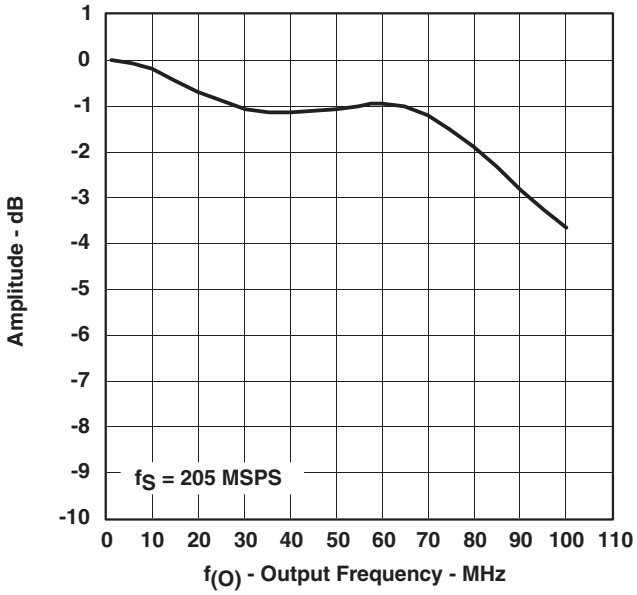


Figure 7-11. AMPLITUDE vs OUTPUT FREQUENCY

7.7 Output Compliance vs Full-Scale Adjustment Resistor Value

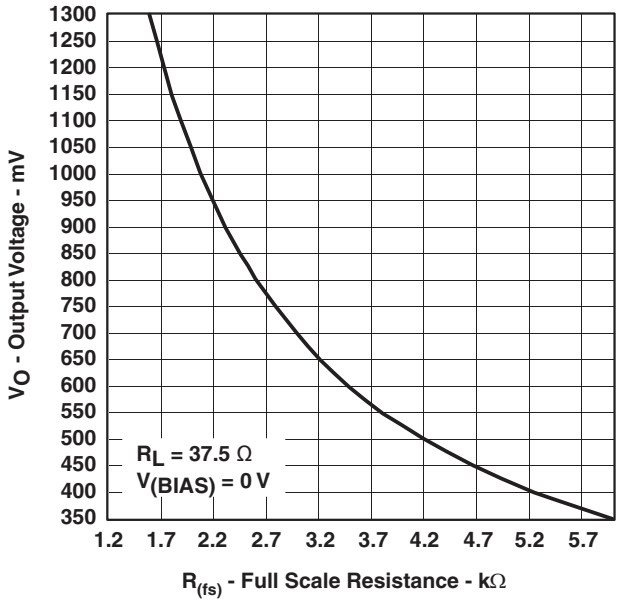


Figure 7-12. OUTPUT VOLTAGE vs FULL-SCALE RESISTANCE

7.8 Vertical Sync of the HDTV 1080I Format Preset in First and Second Field, and Horizontal Line Waveform Detail

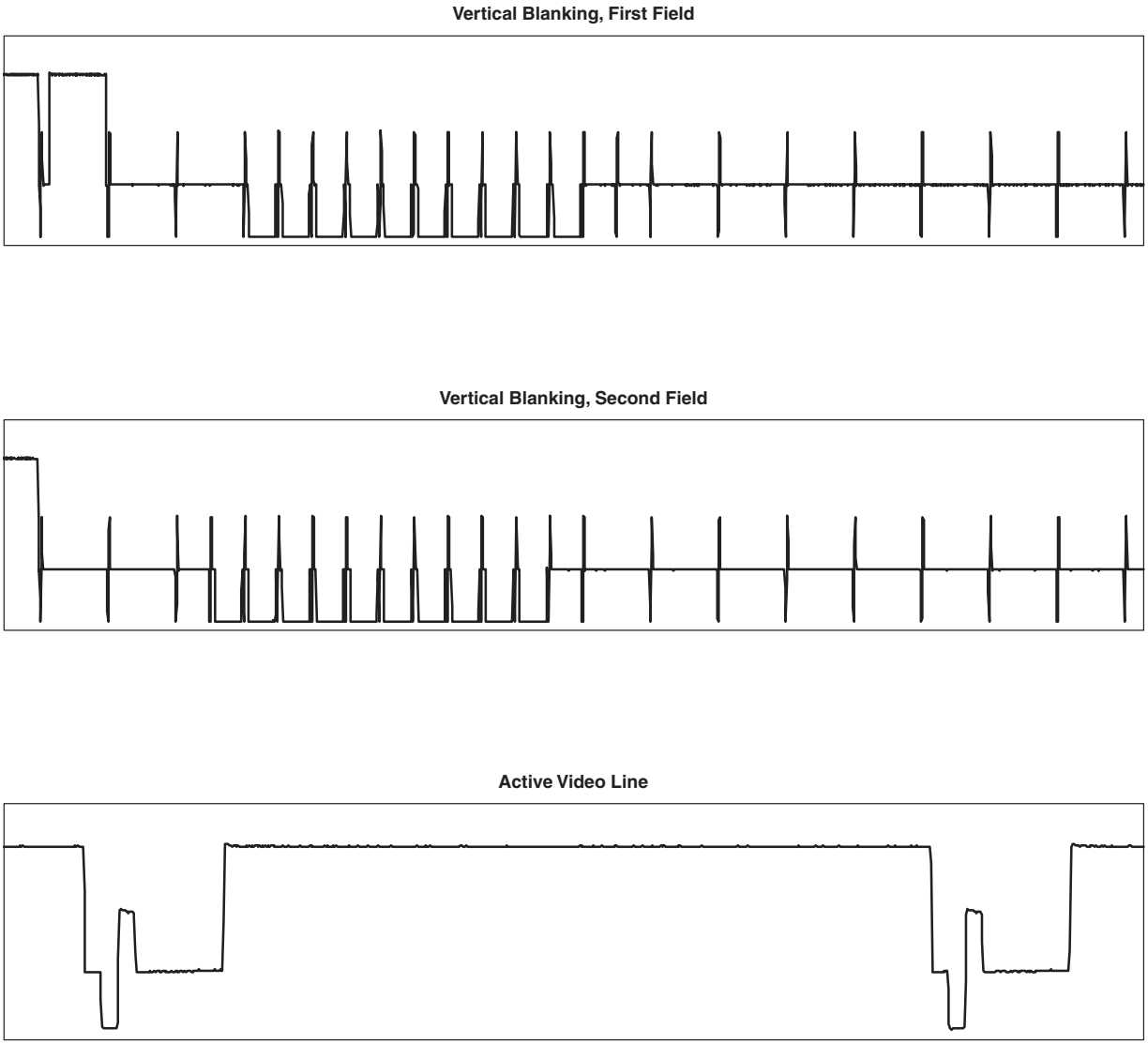


Figure 7-13. THS8200 Output Waveforms for 1080I: Vertical Blanking in First and Second Fields, and Active Video

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS8200IPFPEP	ACTIVE	HTQFP	PFP	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	THS8200IEP D	Samples
V62/10604-01XE	ACTIVE	HTQFP	PFP	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	THS8200IEP D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

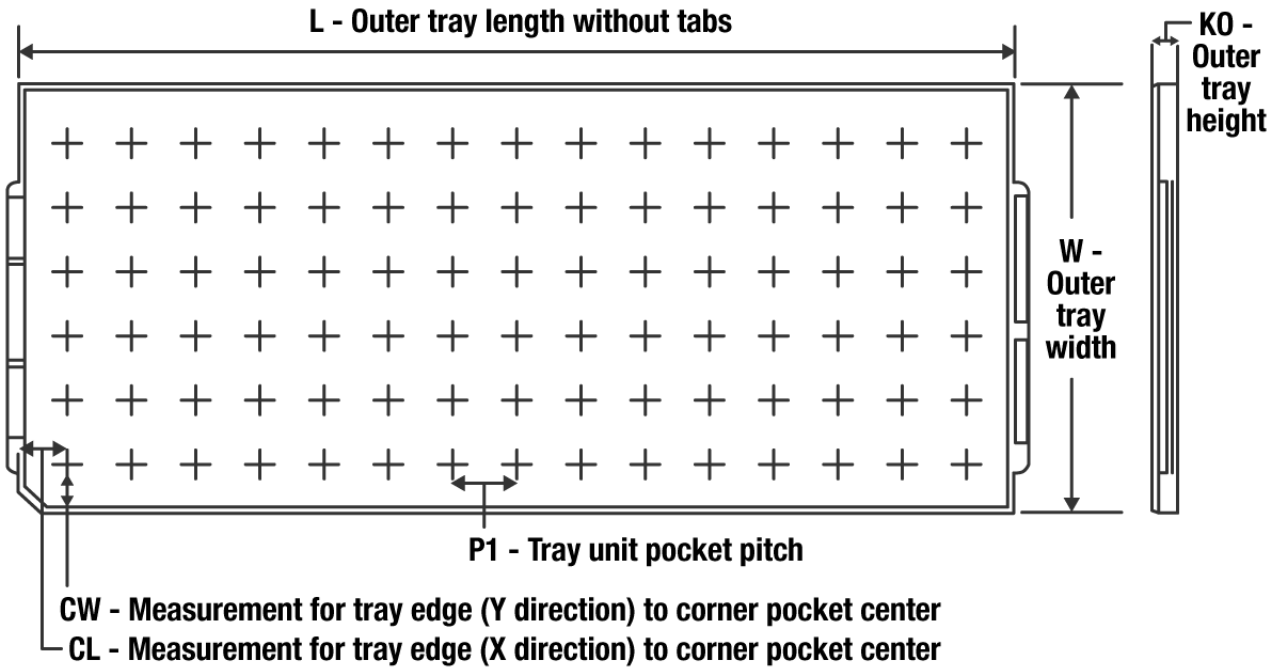
OTHER QUALIFIED VERSIONS OF THS8200-EP :

- Catalog: THS8200

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TRAY

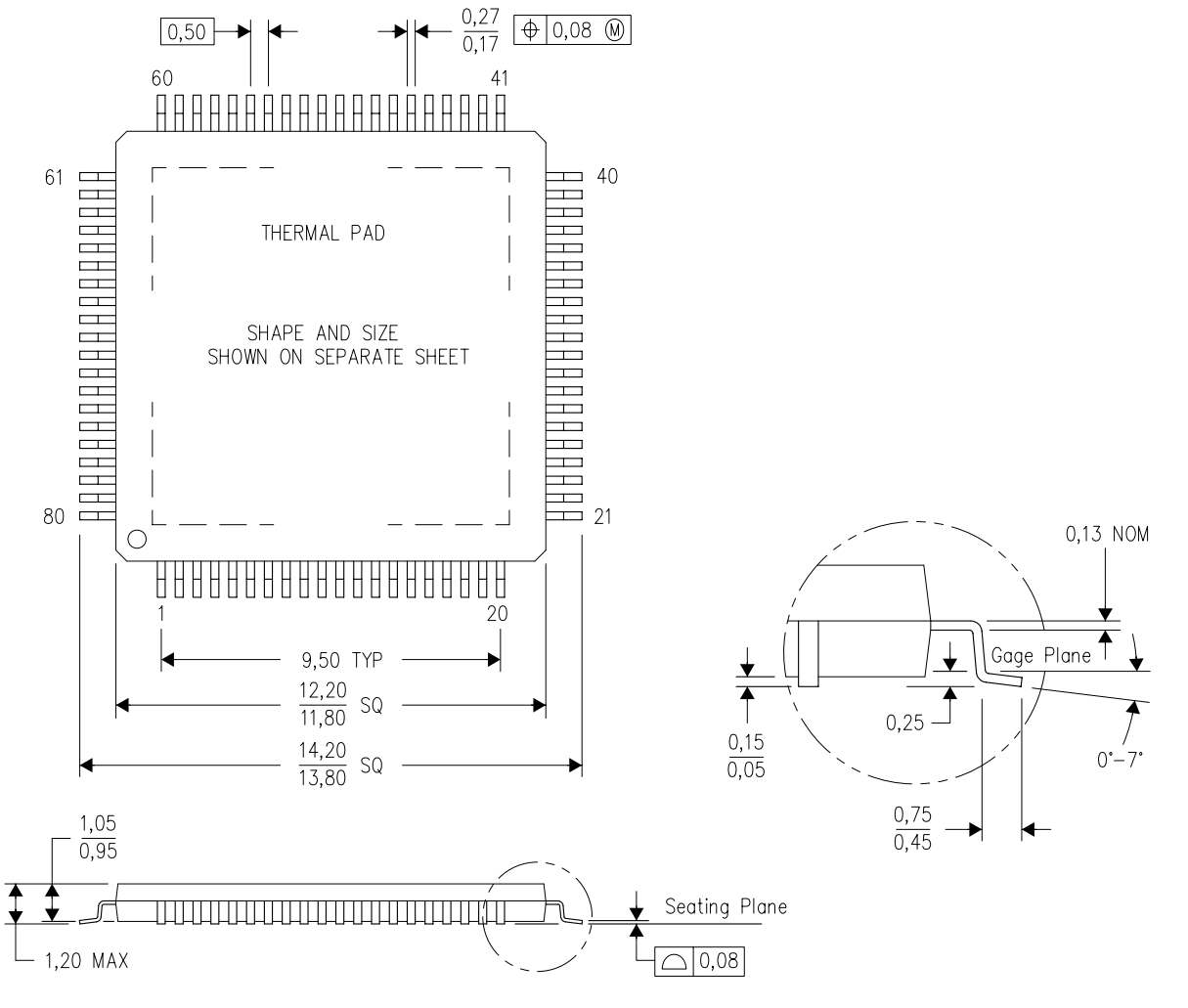


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
THS8200IPFPEP	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
V62/10604-01XE	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

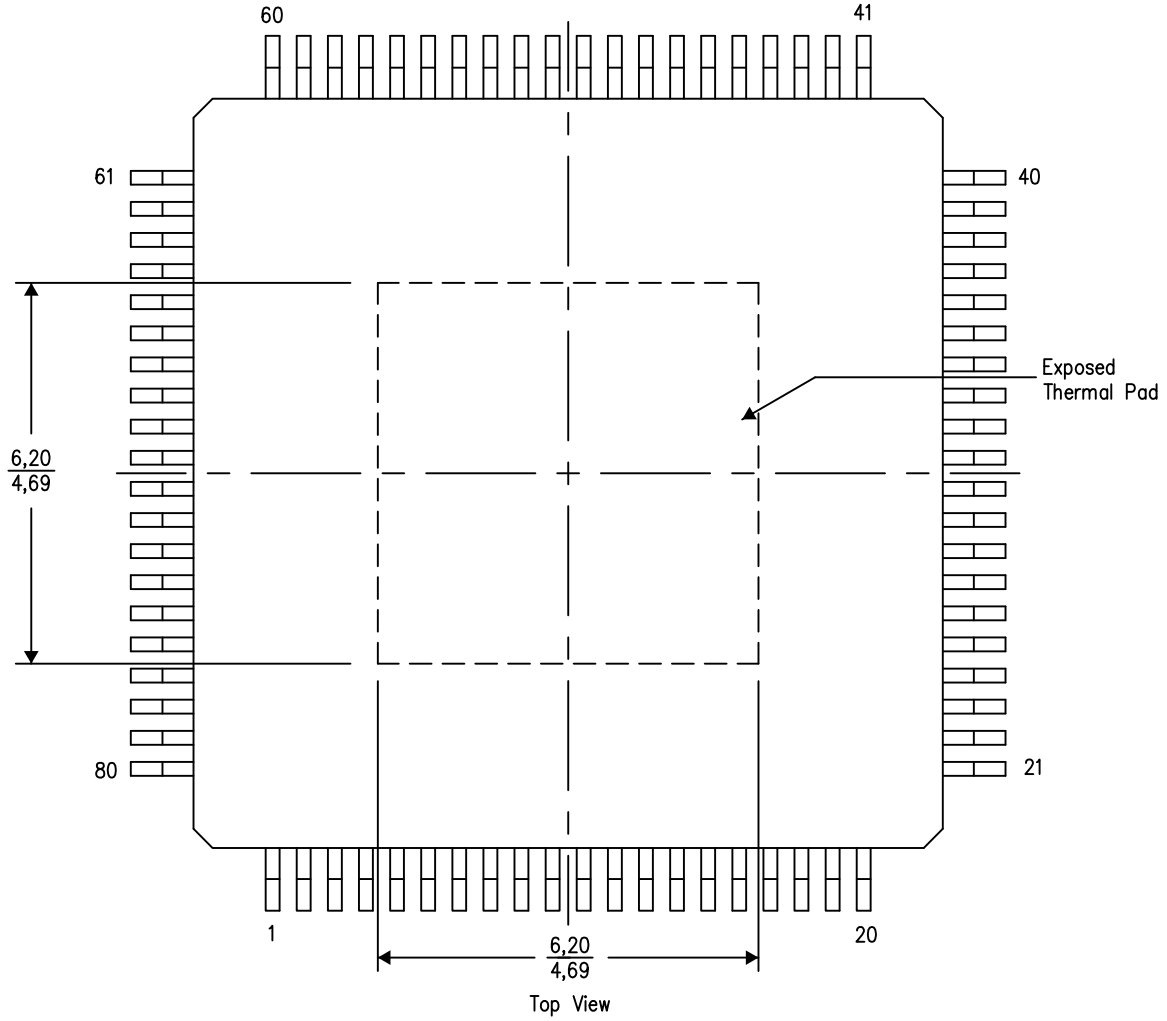
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206327–3/P 05/14

NOTE: A. All linear dimensions are in millimeters

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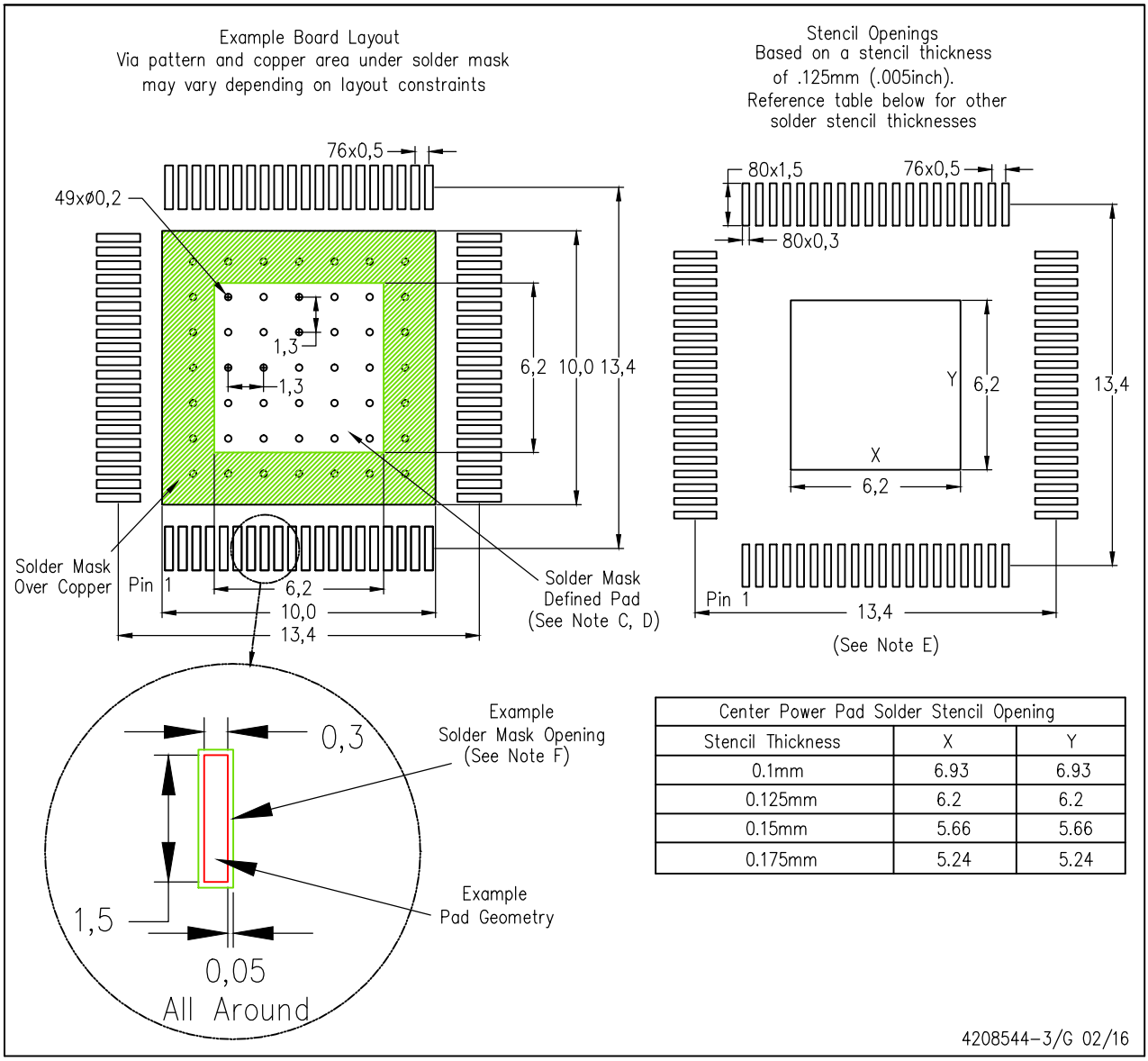
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.93	6.93
0.125mm	6.2	6.2
0.15mm	5.66	5.66
0.175mm	5.24	5.24

PowerPAD is a trademark of Texas Instruments.

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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