ATL431LI / ATL432LI High Bandwidth Low-Iq Programmable Shunt Regulator

1 Features

- Reference voltage tolerance at 25°C
  - 0.5% (B Grade)
  - 1% (A Grade)
- Minimum typical output voltage: 2.5 V
- Adjustable output voltage: V_{ref} to 36 V
- Operation from −40°C to +125°C (Q temp)
- Maximum temperature drift
  - 17 mV (I Temp)
  - 27 mV (Q Temp)
- 0.3-Ω Typical output impedance
- Sink-current capability
  - I_{min} = 0.08 mA (max)
  - I_{KA} = 15 mA (max)
- Reference input current I_{REF}: 0.4 µA (max)
- Deviation of reference input current over temperature, $I_{I(dev)}$: 0.3 µA (max)
- Packages: 1-mm x 1-mm X2SON or SOT23-3

2 Applications

- Adjustable voltage and current referencing
- Secondary side regulation in Flyback SMPS
- Zener diode replacement
- Voltage monitoring
- Precision constant current sink/source
- Comparator with integrated reference

3 Description

The ATL43xLI device is a three-terminal adjustable shunt regulator, with specified thermal stability over applicable automotive, commercial, and military temperature ranges. The output voltage can be set to any value between V_{ref} (approximately 2.5 V) and 36 V, with two external resistors. These devices have a typical output impedance of 0.3 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for Zener diodes in many applications, such as onboard regulation, adjustable power supplies, and switching power supplies. This device is a pin-to-pin alternative to the TL431LI and TL432LI, with lower minimum operating current to help reduce system power consumption. The ATL432LI device has exactly the same functionality and electrical specifications as the ATL431LI device, but has a different pinout for the DBZ package. The ATL431LI is also offered in a tiny X2SON (1.00 mm x 1.00 mm) package which makes it ideal for space constraint applications.

The ATL431LI device is offered in two grades, with initial tolerances (at 25°C) of 0.5%, and 1%, for the B and A grade, respectively. In addition, low output drift versus temperature ensures good stability over the entire temperature range.

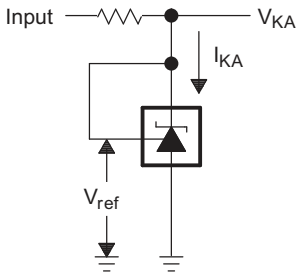
The ATL43xLIxQ devices are characterized for operation from –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
ATL43xLI	SOT-23 (3)	2.90 mm x 1.30 mm
ATL431LI	X2SON (4)	1.00 mm x 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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- Changed typical graph to match *Electrical Characteristics* ... 6
- Added *X2SON (DQN) Layout Example* ... 25
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Changes from Revision B (November 2018) to Revision C — **Page**

- Changed I_{min} description to match *Electrical Characteristics* ... 1
- Added X2SON package option ... 1
- Added X2SON pinout and specifications ... 3

Changes from Revision A (October 2018) to Revision B — **Page**

- Changed ATL43xLI from Product Preview to Production Data. ... 1

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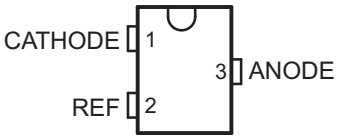
- Changed *Stability Boundary Conditions for All ATL431, ATL432 Devices Above 1 mA* graph ... 7
- Added *Stability Boundary Conditions for All ATL431, ATL432 Devices Below 1 mA* graph ... 7
- Added *Test Circuit for Stability Boundary Conditions* image ... 7

5 Device Comparison Table

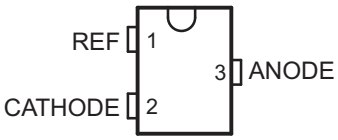
DEVICE PINOUT	INITIAL ACCURACY	OPERATING FREE-AIR TEMPERATURE (T_A)
ATL431LI ATL432LI	A: 1% B: 0.5%	I: -40°C to 85°C Q: -40°C to 125°C

6 Pin Configuration and Functions

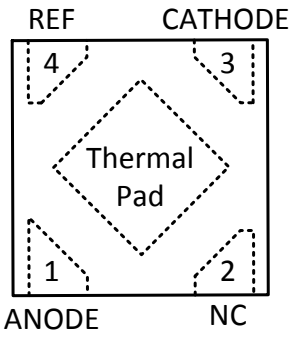
ATL431LI DBZ Package
3-Pin SOT-23
Top View



ATL432LI DBZ Package
3-Pin SOT-23
Top View



ATL431LI DQN Package
4-Pin X2SON
Top View



Pin Functions

NAME	PIN			TYPE	DESCRIPTION
	ATL431LIx	ATL431LIx	ATL432LIx		
	DBZ	DQN	DBZ		
ANODE	3	1	3	O	Common pin, normally connected to ground
CATHODE	1	3	2	I/O	Shunt Current/Voltage input
REF	2	4	1	I	Threshold relative to common anode
NC	N/A	2	N/A	—	No internal connection
Thermal Pad	N/A	Available	N/A	—	Connect to ground or to a floating copper plane for mechanical stability.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{KA}	Cathode Voltage(2)			37	V
I_{KA}	Continuos Cathode Current Range		–10	18	mA
$I_{I(ref)}$	Reference Input Current		–5	10	mA
T_J	Operating Junction Temperature Range		–40	150	C
T_{stg}	Storage Temperature Range		–65	150	C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ANODE, unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001pins(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22- VC101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Thermal Information

THERMAL METRIC(1)		ATL43xLI		UNIT
		DBZ	DQN	
		3 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	371.7	173.7	C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	145.9	185.5	C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	104.7	119.9	C/W
ψ_{JT}	Junction-to-top characterization parameter	23.9	13.1	C/W
ψ_{JB}	Juction-to-board characterization parameter	102.9	119.9	C/W
$R_{\theta JC(bottom)}$	Juction-to-case (bottom) thermal resistance	N/A	93.0	C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

7.4 Recommended Operating Conditions

See (1)

			MIN	MAX	UNIT
V_{KA}	Cathode Voltage		V_{REF}	36	V
I_{KA}	Continuous Cathode Current Range		0.08	15	mA
T_A	Operating Free-Air Temperature	ATL43xLIxI	–40	85	C
		ATL43xLIxQ	–40	125	C

(1) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

7.5 Electrical Characteristics

over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CIRCUIT	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{REF}	Reference Voltage	See Figure 17	$V_{KA} = V_{ref}$, I_{KA} = 1 mA	ATL43xLIAx devices	2475	2500	2525	mV
				ATL43xLIBx devices	2487	2500	2512	mV
$V_{I(dev)}$	Deviation of reference input voltage over full temperature range (1)	See Figure 17	$V_{KA} = V_{ref}$, I_{KA} = 1 mA	ATL43xLIxI devices		6	17	mV
				ATL43xLIxQ devices		10	27	mV
ΔV_{ref} / ΔV_{KA}	Ratio of change in reference voltage to the change in cathode voltage	See Figure 18	I_{KA} = 1 mA	ΔV_{KA} = 10 V - V_{ref}		–1.4	–2.7	mV/V
				ΔV_{KA} = 36 V - 10 V		–1	–2	mV/V
I_{ref}	Reference Input Current	See Figure 18	I_{KA} = 1 mA, R1 = 10kΩ, R2 = ∞			0.2	0.4	µA
$I_{I(dev)}$	Deviation of reference input current over full temperature range (1)	See Figure 18	I_{KA} = 1 mA, R1 = 10kΩ, R2 = ∞			0.1	0.3	µA
I_{min}	Minimum cathode current for regulation	See Figure 17	$V_{KA} = V_{ref}$			65	80	uA
I_{off}	Off-state cathode current	See Figure 19	V_{KA} = 36 V, V_{ref} = 0			0.1	1	µA
$\|Z_{KA}\|$	Dynamic Impedance (2)	See Figure 17	$V_{KA} = V_{ref}$, I_{KA} = 1 mA to 15 mA			0.3	0.65	Ω

(1) The deviation parameters $V_{I(dev)}$ and $I_{I(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. For more details on $V_{I(dev)}$ and how it relates to the average temperature coefficient, see Parameter Measurement Information.

(2) The dynamic impedance is defined by $|Z_{KA}| = \Delta V_{KA}/\Delta I_{KA}$. For more details on $|Z_{KA}|$ and how it relates to V_{KA}, see Parameter Measurement Information.

8 Typical Characteristics

Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

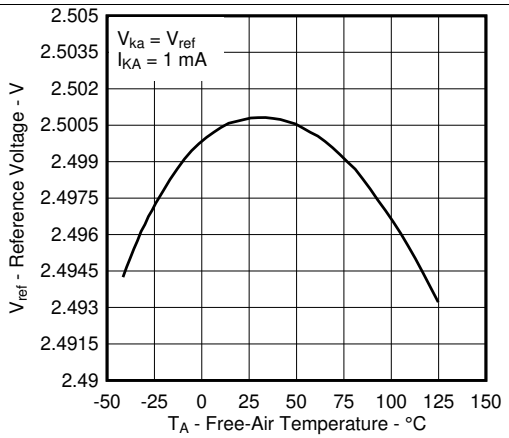


Figure 1. Reference Voltage vs Free-Air Temperature

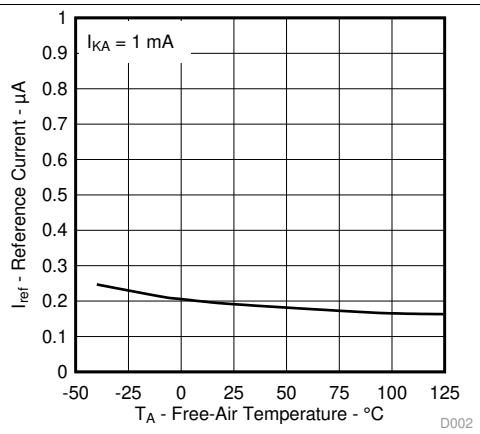


Figure 2. Reference Current vs Free-Air Temperature

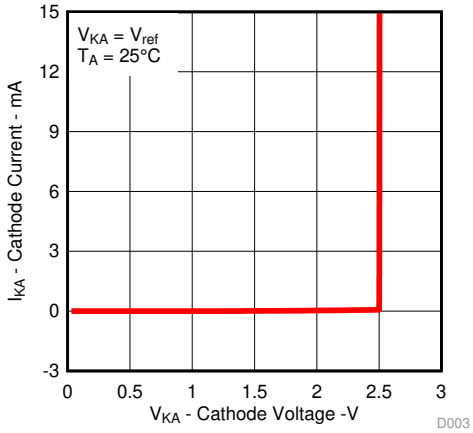


Figure 3. Cathode Current vs Cathode Voltage

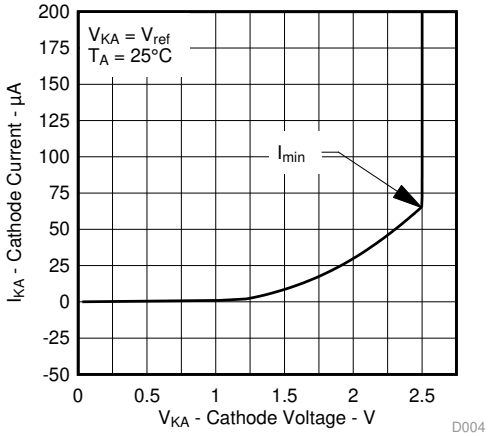


Figure 4. Cathode Current vs Cathode Voltage

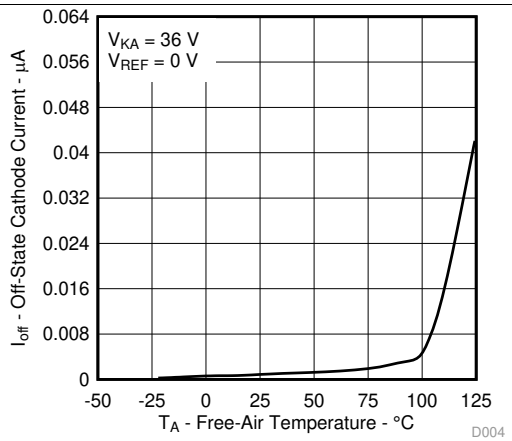


Figure 5. Off-State Cathode Current vs Free-Air Temperature

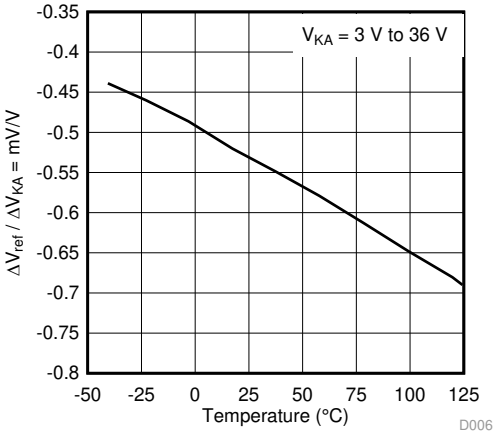


Figure 6. Ratio of Delta Reference Voltage to Delta Cathode Voltage vs Free-Air Temperature

Typical Characteristics (continued)

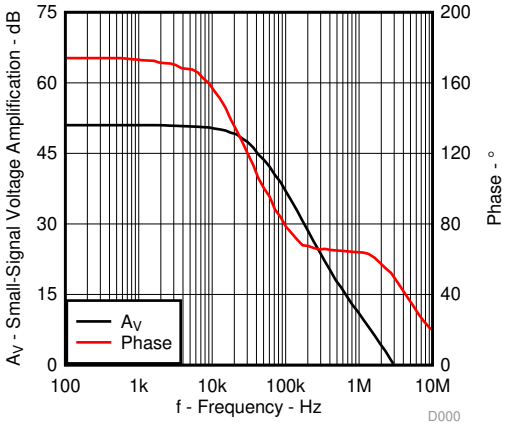


Figure 7. Small-Signal Voltage Amplification vs Frequency

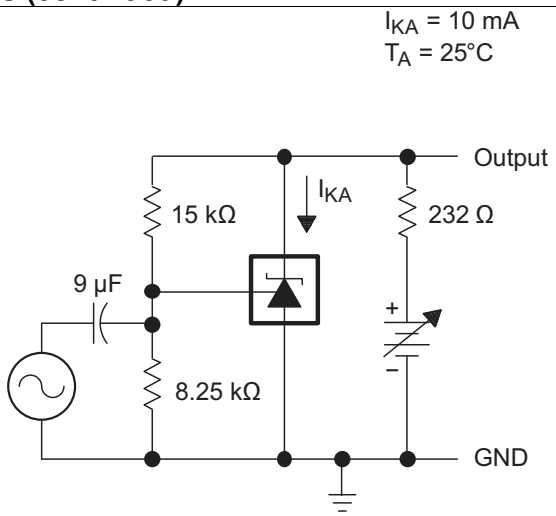


Figure 8. Test Circuit for Voltage Amplification

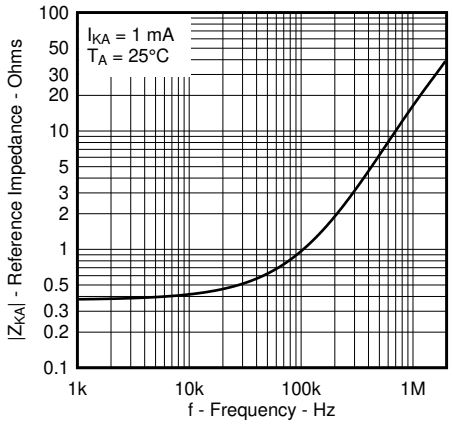


Figure 9. Reference Impedance vs Frequency

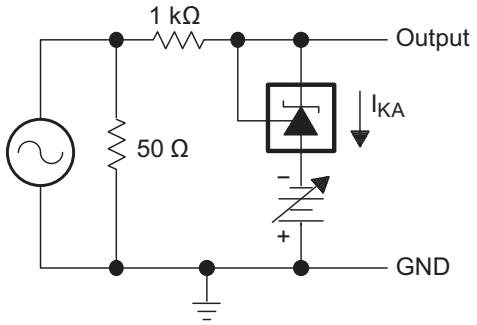


Figure 10. Test Circuit for Reference Impedance

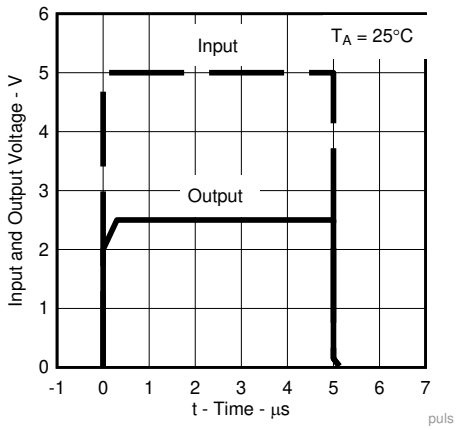


Figure 11. Pulse Response

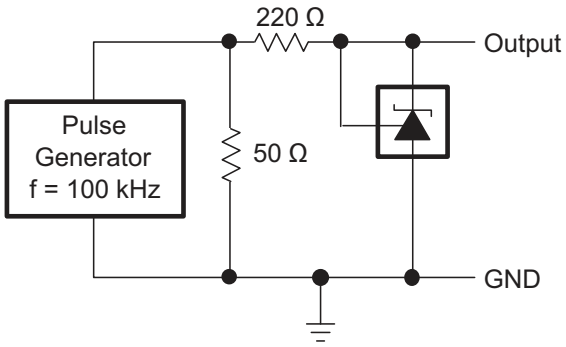
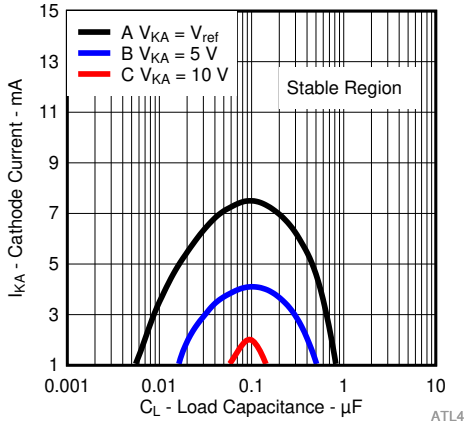


Figure 12. Test Circuit for Pulse Response

Typical Characteristics (continued)



The areas under the curves represent conditions that may cause the device to oscillate. For curves B and C, R2 and V+ are adjusted to establish the initial V_{KA} and I_{KA} conditions, with C_L = 0. V_{BATT} and C_L then are adjusted to determine the ranges of stability.

Figure 13. Stability Boundary Conditions for All ATL431LI, ATL432LI Devices Above 1 mA

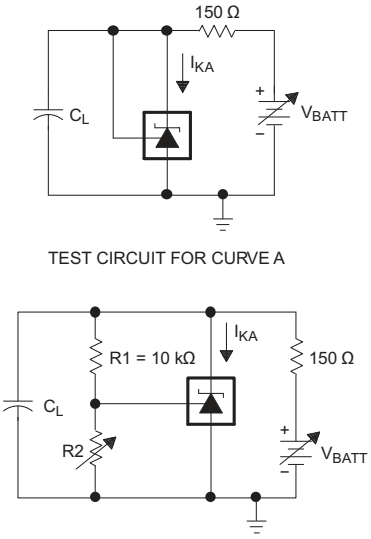
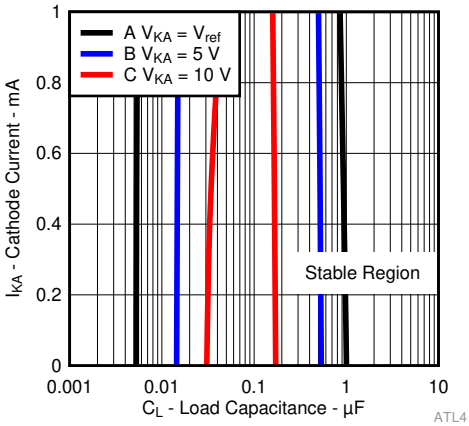


Figure 14. Test Circuit for Stability Boundary Conditions



The areas in-between the curves represent conditions that may cause the device to oscillate. For curves B, and C, R2 and V+ are adjusted to establish the initial V_{KA} and I_{KA} conditions, with C_L = 0. V_{BATT} and C_L then are adjusted to determine the ranges of stability.

Figure 15. Stability Boundary Conditions for All ATL431LI, ATL432LI Devices Below 1 mA

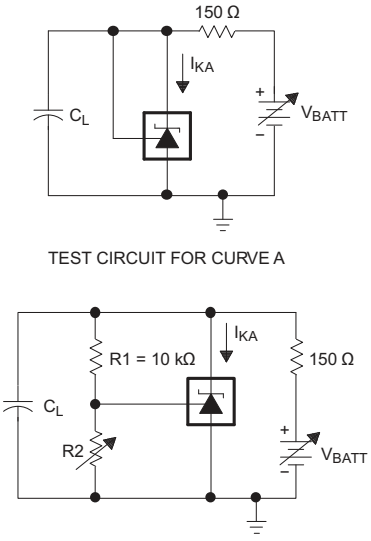


Figure 16. Test Circuit for Stability Boundary Conditions

9 Parameter Measurement Information

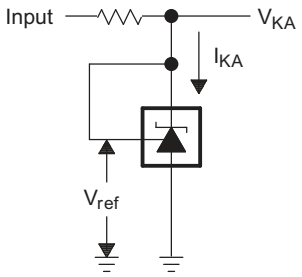


Figure 17. Test Circuit for $V_{KA} = V_{ref}$

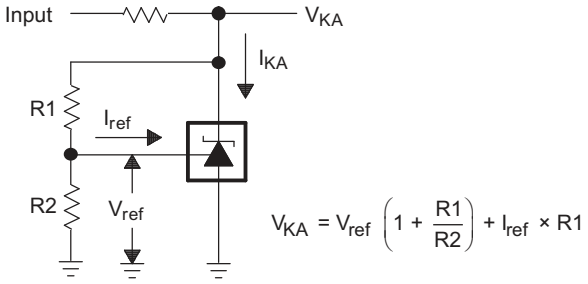


Figure 18. Test Circuit for $V_{KA} > V_{ref}$

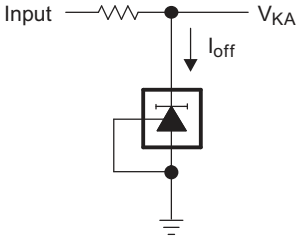


Figure 19. Test Circuit for I_{off}

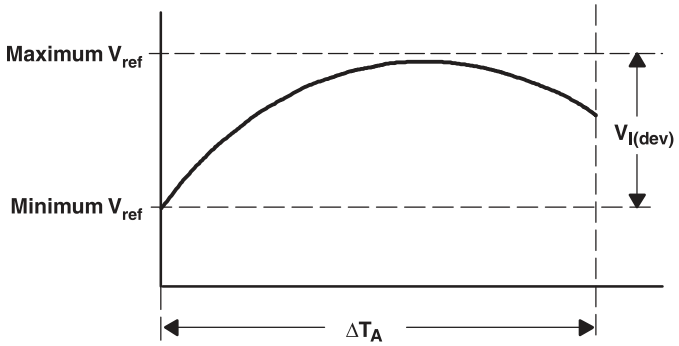
9.1 Temperature Coefficient

The deviation of the reference voltage, V_{ref}, over the full temperature range is known as $V_{I(dev)}$. The parameter of $V_{I(dev)}$ can be used to find the temperature coefficient of the device. The average full-range temperature coefficient of the reference input voltage, α_{Vref}, is defined as:

$$\left|\alpha_{Vref}\right| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{I(dev)}}{V_{ref\ at\ 25°C}}\right) \times 10^6}{\Delta T_A}$$

where:

ΔT_A is the rated operating temperature range of the device.



α_{Vref} is positive or negative, depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature. The full-range temperature coefficient is an average and therefore any subsection of the rated operating temperature range can yield a value that is greater or less than the average. For more details on temperature coefficient, check out *Voltage Reference Selection Basics.*

9.2 Dynamic Impedance

The dynamic impedance is defined as: $|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_{KA}}$. When the device is operating with two external resistors (see Figure 18), the total dynamic impedance of the circuit is given by: $|z'| = \frac{\Delta V}{\Delta I}$ which is approximately equal to $|Z_{KA}|\left(1+\frac{R1}{R2}\right)$.

The V_{KA} of the ATL431LI can be affected by the dynamic impedance. The ATL431LI test current I_{test} for V_{KA} is specified on the *Eletrical Characteristics* . Any deviation from I_{test} can cause deviation on the output V_{KA}. Figure 20 shows the effect of the dynamic impedance on the V_{KA}.

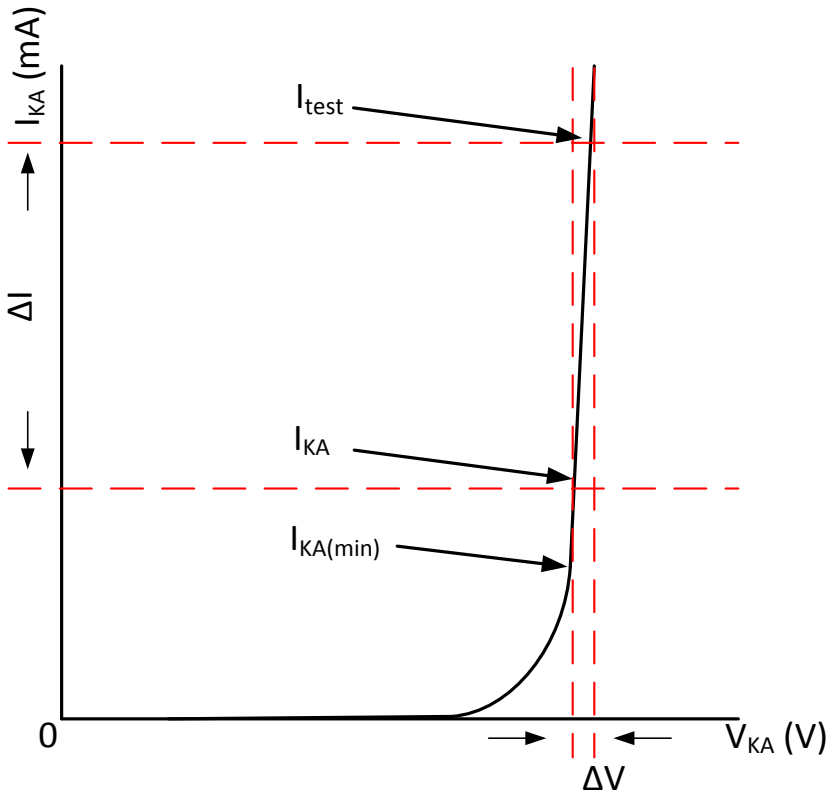


Figure 20. Dynamic Impedance

10 Detailed Description

10.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications, ranging from power to signal path. This is due to its key components containing an accurate voltage reference and opamp, which are very fundamental analog building blocks. ATL431LI is used in conjunction with its key components to behave as a single voltage reference, error amplifier, voltage clamp or comparator with integrated reference.

ATL431LI can be operated and adjusted to cathode voltages from 2.5V to 36V, making this part optimal for a wide range of end equipments in industrial, auto, telecom & computing. In order for this device to behave as a shunt regulator or error amplifier, >80µA (I_{min}(maximum)) must be supplied in to the cathode pin. Under this condition, feedback can be applied from the Cathode and Ref pins to create a replica of the internal reference voltage.

Various reference voltage options can be purchased with initial tolerances (at 25°C) of 0.5%, and 1%. These reference options are denoted by B (0.5%) and A (1.0%) after the ATL431LI or ATL432LI. ATL431LI and ATL432LI are both functionally the same, but have separate pinout options.

The ATL43xLIxQ devices are characterized for operation from –40°C to +125°C.

10.2 Functional Block Diagram

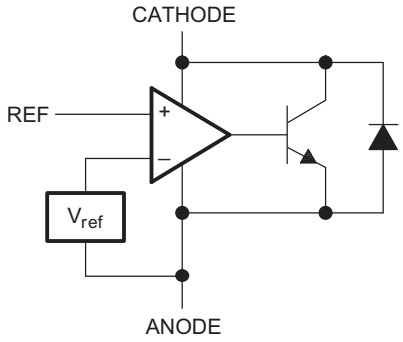


Figure 21. Equivalent Schematic

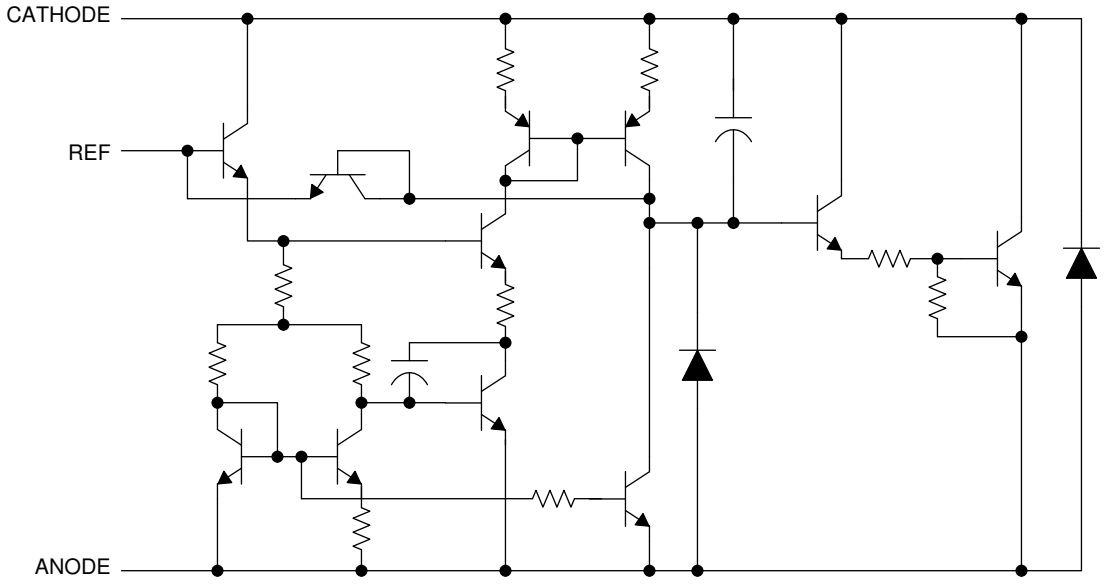


Figure 22. Detailed Schematic

10.3 Feature Description

ATL431LI consists of an internal reference and amplifier that outputs a sink current based on the difference between the reference pin and the virtual internal pin. The sink current is produced by the internal Darlington pair, shown in the above schematic (Figure 21). A Darlington pair is used in order for this device to be able to sink a maximum current of 15 mA.

When operated with enough voltage headroom (≥ 2.5 V) and cathode current (I_{KA}), ATL431LI forces the reference pin to 2.5 V. However, the reference pin can not be left floating, as it needs I_{REF} ≥ 0.4 µA (see *Specifications*). This is because the reference pin is driven into an NPN, which needs base current in order operate properly.

When feedback is applied from the Cathode and Reference pins, ATL431LI behaves as a Zener diode, regulating to a constant voltage dependent on current being supplied into the cathode. This is due to the internal amplifier and reference entering the proper operating regions. The same amount of current needed in the above feedback situation must be applied to this device in open loop, servo or error amplifying implementations in order for it to be in the proper linear region giving ATL431LI enough gain.

Unlike many linear regulators, ATL431LI is internally compensated to be stable without an output capacitor between the cathode and anode. However, if it is desired to use an output capacitor Figure 13 can be used as a guide to assist in choosing the correct capacitor to maintain stability.

10.4 Device Functional Modes

10.4.1 Open Loop (Comparator)

When the cathode/output voltage or current of ATL431LI is not being fed back to the reference/input pin in any form, this device is operating in open loop. With proper cathode current (Ika) applied to this device, ATL431LI will have the characteristics shown in SLVA987. With such high gain in this configuration, ATL431LI is typically used as a voltage comparator. The integrated voltage reference makes the ATL431LI a flexible device for monitoring a signal for undervoltage and overvoltage detection.

10.4.2 Closed Loop

When the cathode/output voltage or current of ATL431LI is being fed back to the reference/input pin in any form, this device is operating in closed loop. The majority of applications involving ATL431LI use it in this manner to regulate a fixed voltage or current. The feedback enables this device to behave as an error amplifier, computing a portion of the output voltage and adjusting it to maintain the desired regulation. This is done by relating the output voltage back to the reference pin in a manner to make it equal to the internal reference voltage, which can be accomplished via resistive or direct feedback.

11 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

As this device has many applications and setups, there are many situations that this datasheet can not characterize in detail. The linked application notes will help the designer make the best choices when using this part.

Application note *Understanding Stability Boundary Conditions Charts in TL431, TL432 Data Sheet*, SLVA482 provides a deeper understanding of this device's stability characteristics and aid the user in making the right choices when choosing a load capacitor. Application note *Setting the Shunt Voltage on an Adjustable Shunt Regulator*, SLVA445 assists with setting the shunt voltage to achieve optimum accuracy for this device.

11.2 Typical Applications

11.2.1 Comparator With Integrated Reference

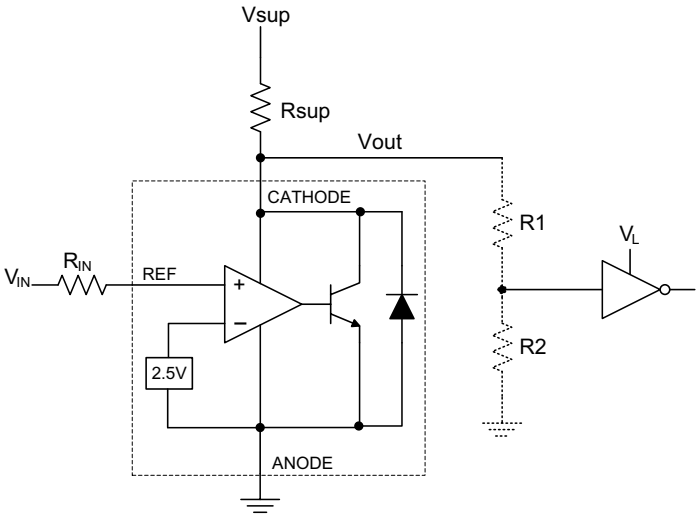


Figure 23. Comparator Application Schematic

Typical Applications (continued)

11.2.1.1 Design Requirements

For this design example, use the parameters listed in *Table 1* as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to 5 V
Input Resistance	10 kΩ
Supply Voltage	24 V
Cathode Current (Ik)	5 mA
Output Voltage Level	~2 V – V_{SUP}
Logic Input Thresholds VIH/VIL	V_L

11.2.1.2 Detailed Design Procedure

When using ATL431LI as a comparator with reference, determine the following:

- Input Voltage Range
- Reference Voltage Accuracy
- Output logic input high and low level thresholds
- Current Source resistance

11.2.1.2.1 Basic Operation

In the configuration shown in Figure 23 ATL431LI will behave as a comparator, comparing the V_{REF} pin voltage to the internal virtual reference voltage. When provided a proper cathode current (I_K), ATL431LI will have enough open loop gain to provide a quick response. This can be seen in Figure 24, where the R_{SUP}=10 kΩ (I_{KA}=500 µA) situation responds much slower than R_{SUP}=1 kΩ (I_{KA}=5 mA). With the ATL431LI max Operating Current (I_{MIN}) being 0.08 mA, operation near that could result in low gain, leading to a slow response.

11.2.1.2.1.1 Overdrive

Slow or inaccurate responses can also occur when the reference pin is not provided enough overdrive voltage. This is the amount of voltage that is higher than the internal virtual reference. The internal virtual reference voltage will be within the range of 2.5 V ±(0.5% or 1.0%) depending on which version is being used. The more overdrive voltage provided, the faster the ATL431LI will respond.

For applications where ATL431LI is being used as a comparator, it is best to set the trip point to greater than the positive expected error (that is +1.0% for the A version). For fast response, setting the trip point to >10% of the internal V_{REF} should suffice.

For minimal voltage drop or difference from Vin to the ref pin, TI recommends to use an input resistor <10kΩ to provide Iref.

11.2.1.2.2 Output Voltage and Logic Input Level

In order for ATL431LI to properly be used as a comparator, the logic output must be readable by the receiving logic device. This is accomplished by knowing the input high and low level threshold voltage levels, typically denoted by V_{IH} and V_{IL}.

As seen in Figure 24, ATL431LI's output low level voltage in open-loop/comparator mode is approximately 2 V, which is typically sufficient for 5V supplied logic. However, would not work for 3.3 V and 1.8 V supplied logic. To accommodate this a resistive divider can be tied to the output to attenuate the output voltage to a voltage legible to the receiving low voltage logic device.

ATL431's output high voltage is equal to V_{SUP} due to ATL431LI being open-collector. If V_{SUP} is much higher than the receiving logic's maximum input voltage tolerance, the output must be attenuated to accommodate the outgoing logic's reliability.

When using a resistive divider on the output, be sure to make the sum of the resistive divider (R1 and R2 in Figure 23) is much greater than R_{SUP} in order to not interfere with ATL431LI's ability to pull close to V_{SUP} when turning off.

11.2.1.2.2.1 Input Resistance

ATL431LI requires an input resistance in this application in order to source the reference current (I_{REF}) needed from this device to be in the proper operating regions while turning on. The actual voltage seen at the ref pin will be $V_{REF}=V_{IN}-I_{REF}*R_{IN}$. Because I_{REF} can be as high as 4 µA. TI recommends to use a resistance small enough that will mitigate the error that I_{REF} creates from V_{IN}.

11.2.1.3 Application Curve

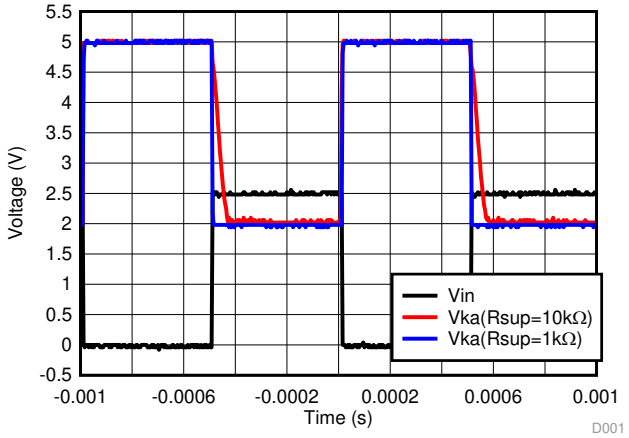


Figure 24. Output Response With Various Cathode Currents

11.2.2 Precision Constant Current Sink

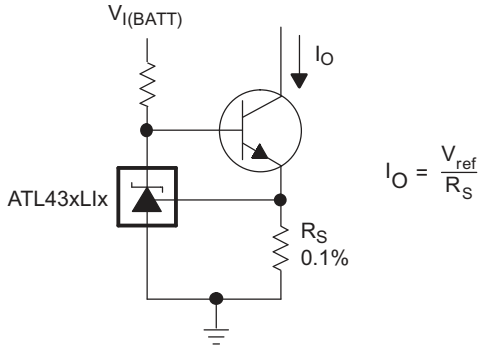


Figure 25. Precision Constant Current Sink Application Schematic

11.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Supply Voltage ($V_{I(BATT)}$)	5 V
Sink Current (I_O)	100mA
Cathode Current (Ik)	5 mA

11.2.2.2 Detailed Design Procedure

When using ATL43xLI as a constant current sink, determine the following:

- Output Current Range
- Output Current Accuracy
- Power Consumption for ATL43xLI

11.2.2.2.1 Basic Operation

In the configuration shown, ATL43xLI acts as a control component within a feedback loop of the constant current sink. Working with an external passing component such as an BJT, ATL43xLI provides precision current sink with accuracy set by itself and the sense resistor R_S. This circuit can also be used as LED driving circuit.

11.2.2.2.1.1 Output Current Range and Accuracy

The output current range of the circuit is determined by the equation shown in the configuration. Keep in mind that the V_{REF} equals to 2.5V. When choosing the sense resistor R_S, it needs to generate 2.5V for the ATL43xLI when I_O reaches the target current. If the overhead voltage of 2.5V is not acceptable, please consider lower voltage reference devices such as TLV43x or TLVH43x.

The output current accuracy is determined by both the accuracy of ATL43xLI chosen, as well as the accuracy of the sense resistor R_S. The internal virtual reference voltage of ATL43xLI will be within the range of 2.5 V ±(0.5% or 1.0%) depending on which version is being used. Another consideration for the output current accuracy is the temperature coefficient of the ATL43xLI and R_S. Please refer to the electrical characterization table for the specification of these parameters.

11.2.2.2.2 Power Consumption

In order for ATL43xLI to properly be used as a control component in this circuit, the minimum operating current needs to be reached. This is accomplished by setting the external biasing resistor in series with the ATL43xLI.

For ATL43xLI, the minimum operating current is 80µA and with margin consideration, most of the designs set this current to be higher than 100µA. To achieve lower power consumption, please consider devices such as ATL43x.

11.2.3 Shunt Regulator/Reference

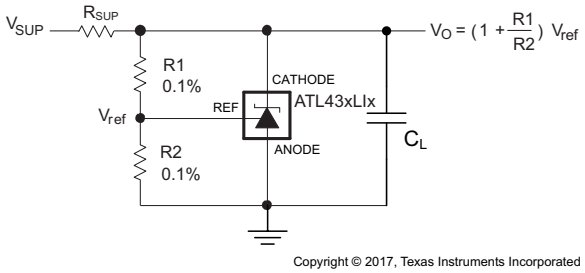


Figure 26. Shunt Regulator Schematic

11.2.3.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Reference Initial Accuracy	1.0%
Supply Voltage	24 V
Cathode Current (Ik)	5 mA
Output Voltage Level	2.5 V - 36 V
Load Capacitance	2 µF
Feedback Resistor Values and Accuracy (R1 and R2)	10 kΩ

11.2.3.2 Detailed Design Procedure

When using ATL431LI as a Shunt Regulator, determine the following:

- Input Voltage Range
- Temperature Range
- Total Accuracy
- Cathode Current
- Reference Initial Accuracy
- Output Capacitance

11.2.3.2.1 Programming Output/Cathode Voltage

In order to program the cathode voltage to a regulated voltage a resistive bridge must be shunted between the cathode and anode pins with the mid point tied to the reference pin. This can be seen in Figure 26, with R1 and R2 being the resistive bridge. The cathode/output voltage in the shunt regulator configuration can be approximated by the equation shown in Figure 26. The cathode voltage can be more accuratel determined by taking in to account the cathode current:

$$Vo = (1+R1/R2) \times V_{REF} - I_{REF} \times R1 \quad (1)$$

In order for this equation to be valid, ATL431LI must be fully biased so that it has enough open loop gain to mitigate any gain error. This can be done by meeting the Imin spec denoted in *Specifications*.

11.2.3.2.2 Total Accuracy

When programming the output above unity gain (V_{KA}=V_{REF}), ATL431LI is susceptible to other errors that may effect the overall accuracy beyond V_{REF}. These errors include:

- R1 and R2 accuracies
- $V_{I(dev)}$ - Change in reference voltage over temperature
- ΔV_{REF} / ΔV_{KA} - Change in reference voltage to the change in cathode voltage
- $|z_{KA}|$ - Dynamic impedance, causing a change in cathode voltage with cathode current

Worst case cathode voltage can be determined taking all of the variables in to account. Application note *Setting the Shunt Voltage on an Adjustable Shunt Regulator*, SLVA445 assists designers in setting the shunt voltage to achieve optimum accuracy for this device.

11.2.3.2.3 Stability

Though ATL431LI is stable with no capacitive load, the device that receives the shunt regulator's output voltage could present a capacitive load that is within the ATL431LI region of stability, shown in Figure 13. Also, designers may use capacitive loads to improve the transient response or for power supply decoupling. When using additional capacitance between Cathode and Anode, see Figure 13. Also, application note *Understanding Stability Boundary Conditions Charts in TL431, TL432 Data Sheet*, SLVA482 will provide a deeper understanding of this devices stability characteristics and aid the user in making the right choices when choosing a load capacitor.

11.2.3.2.4 Start-Up Time

As shown in Figure 27, ATL431LI has a fast response up to approximately 2 V and then slowly charges to its programmed value. This is due to the compensation capacitance (shown in Figure 13) the ATL43xLIx has to meet its stability criteria. Despite the secondary delay, ATL43xLIx still has a fast response suitable for many clamp applications.

11.2.3.3 Application Curve

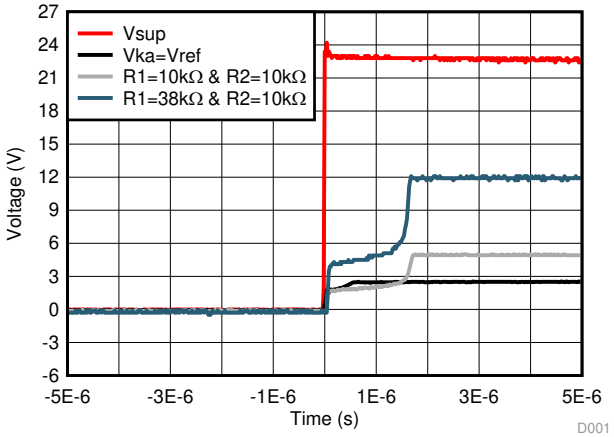


Figure 27. ATL43xLIx Start-Up Response

11.2.4 Isolated Flyback with Optocoupler

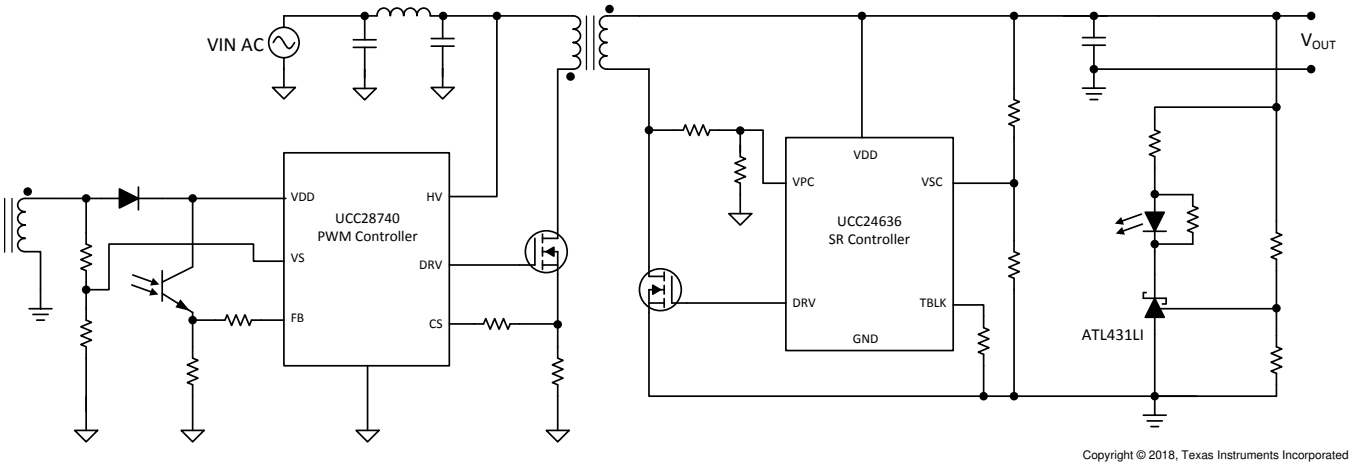


Figure 28. Isolated Flyback with Optocoupler

11.2.4.1 Design Requirements

The ATL431LI is used in the feedback network on the secondary side for a isolated flyback with optocoupler design. Figure 28 shows the simplified flyback converter that used the ATL431LI. For this design example, use the parameters in Table 4 as the input parameters.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Voltage Output	20 V
Feedback Network Quiescent Current (I_q)	<40 mW

11.2.4.1.1 Detailed Design Procedure

In this example a simplified design procedure will be discussed. The compensation network for the feedback network is beyond the scope of this section. Details on compensation network can be found on SLUA671.

The goal of this design is to design a low standby current feedback network to meet the Europe CoC Tier 2 and United States DoE Level VI requirements. To meet the design requirements, the system standby power needs to be below 75mW. In order to meet this, the feedback network needs to consume less than 40mW to allow margin for the power losses on the primary side controller and passive components and this can pose a challenge in systems greater than 10V.

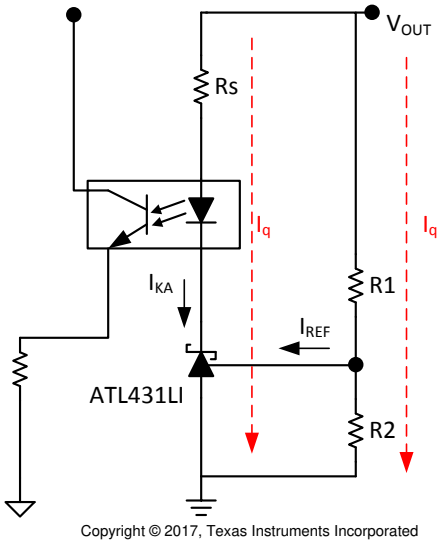


Figure 29. Feedback Quiescent Current

11.2.4.1.1.1 ATL431LI Biasing

Figure 29 shows the simplified version of the feedback network. The standby I_q of the system is dependent on two paths, ATL431LI biasing path and the resistor feedback path. With the given design requirements the total current through the feedback network cannot exceed 2mA.

The design goal is to take full advantage of the I_{min} to set the I_{KA} of the ATL431LI. The benefit of the ATL431LI is its low I_{min} of 80 µA which allows the I_{KA} to be lower at a full load condition compared to typical TL431LI devices. This helps lower the I_{KA} at the no-load condition which is higher than the full load condition due to the dynamic changes in the I_{KA} as the system load varies. The I_{KA} at no-load, I_{OPTNL}, is dependent the value of Rs which is the biasing resistor. Rs is very application specific and is dependent on variables such as optocoupler's CTR, voltage, and current at no-load and this can be seen on Equation 2. By using an optocoupler with a high CTR it is possible to lower I_{OPTNL} to a value of 1.5 mA for a power loss of 30 mW.

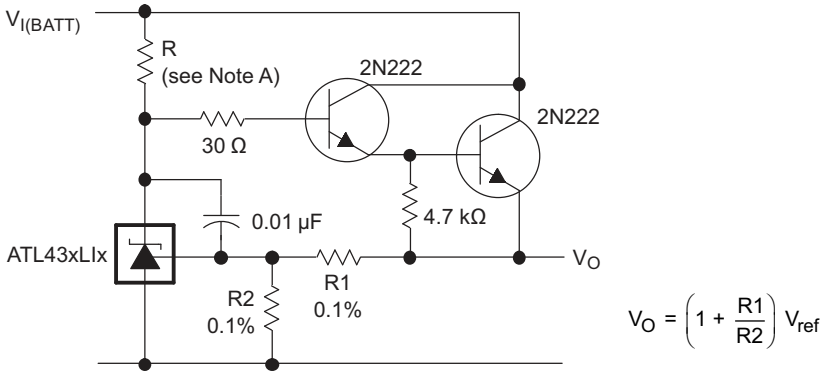
$$Rs \approx (V_{OUT} - V_{OPTNL} - 2\,V) / I_{OPTNL}$$
$$V_{OPTNL} = \text{Optocoupler Voltage at No} - \text{Load Conditions}$$
$$I_{OPTNL} = \text{Optocoupler Current at No} - \text{Load Conditions} \quad (2)$$

11.2.4.1.1.2 Resistor Feedback Network

The feedback resistors set the output voltage of the secondary side and will consume the same I_q at a fixed voltage. The design goal for the feedback resistor path is to minimize the resistor error while maintaining a low I_q. For this system example the feedback network path in this design will consume 0.5 mA to allow enough current for ATL431LI biasing. The resistors, R1 and R2, are sized based on a 0.5 mA budget for I_q and I_{ref}. By using the resistor values from Equation 3 and Equation 4 the total power consumption will be 10mW and this can be further decreased by using larger resistors.

$$R_1 = (V_{OUT} - V_{REF}) / I_{FB}$$
$$R_1 = (20\,V - 2.5\,V) / 0.5\,mA$$
$$R_1 = 35\,k\Omega \quad (3)$$
$$R_2 = V_{REF} / (I_{FB} - I_{REF})$$
$$R_2 = 2.5\,V / (0.5\,mA - 0.4\,\mu A)$$
$$R_2 = 5.004\,k\Omega \quad (4)$$

11.3 System Examples



A. R should provide cathode current ≥ 0.08 mA to the ATL431LI at minimum $V_{(BATT)}$.

Figure 30. Precision High-Current Series Regulator

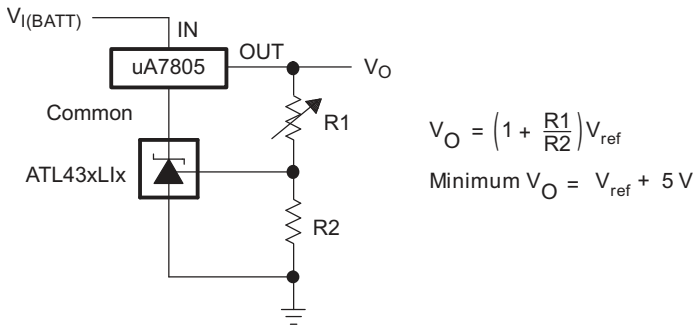


Figure 31. Output Control of a Three-Terminal Fixed Regulator

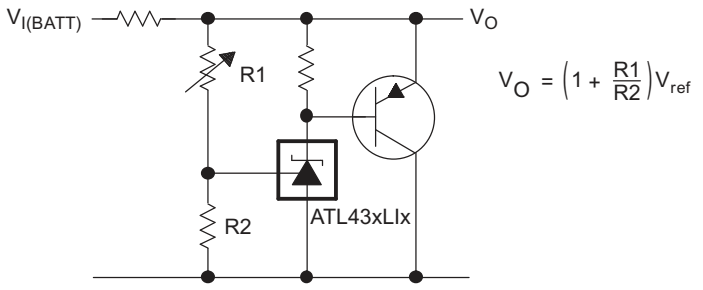
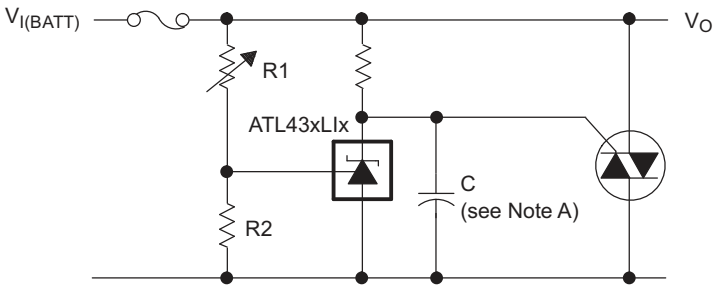


Figure 32. High-Current Shunt Regulator

System Examples (continued)



A. Refer to the stability boundary conditions in and Figure 13 to determine allowable values for C.

Figure 33. Crowbar Circuit

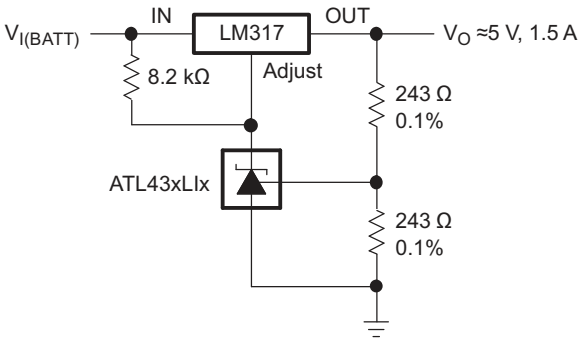
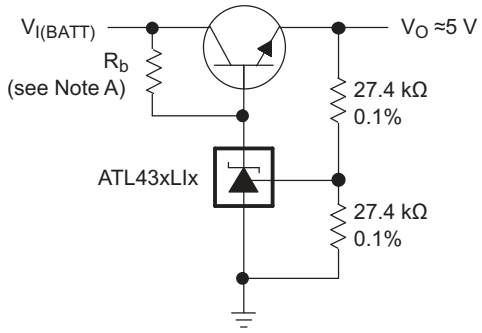


Figure 34. Precision 5-V, 1.5-A Regulator



A. R_b should provide cathode current ≥0.08 mA to the ATL431LI.

Figure 35. Efficient 5-V Precision Regulator

System Examples (continued)

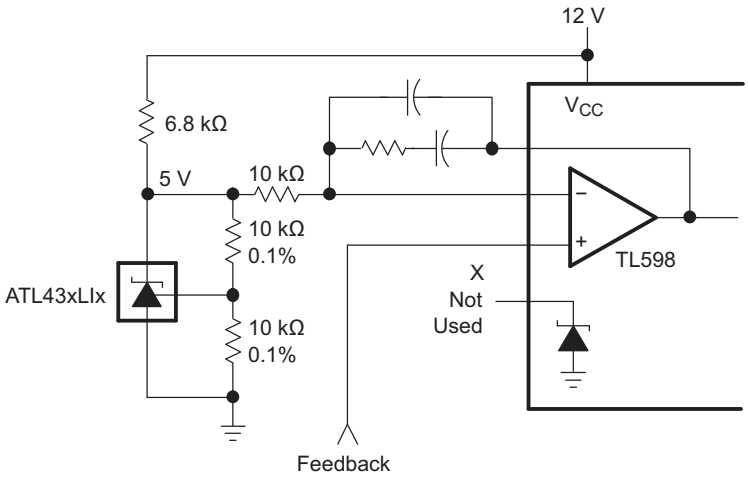
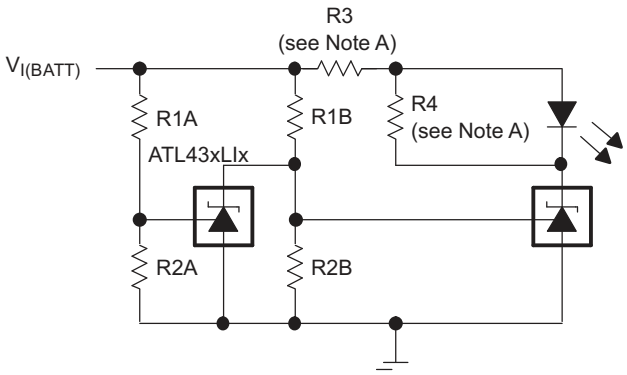


Figure 36. PWM Converter With Reference



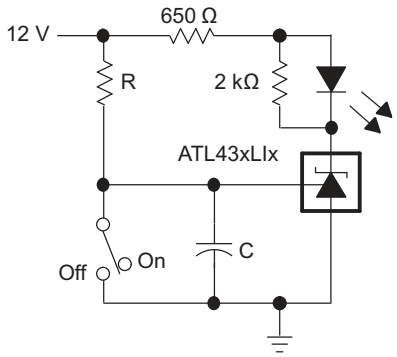
$$\text{Low Limit} = \left(1 + \frac{R1B}{R2B}\right)V_{ref}$$

$$\text{High Limit} = \left(1 + \frac{R1A}{R2A}\right)V_{ref}$$

LED on When Low Limit < $V_{I(BATT)}$ < High Limit

A. Select R3 and R4 to provide the desired LED intensity and cathode current ≥ 0.08 mA to the ATL431LI at the available $V_{I(BATT)}$.

Figure 37. Voltage Monitor



$$\text{Delay} = R \times C \times \ln\left(\frac{12\ V}{12\ V - V_{ref}}\right)$$

Figure 38. Delay Timer

System Examples (continued)

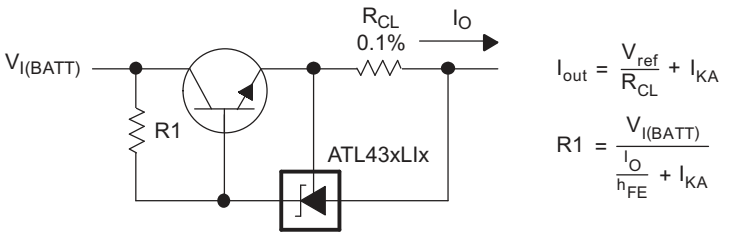


Figure 39. Precision Current Limiter

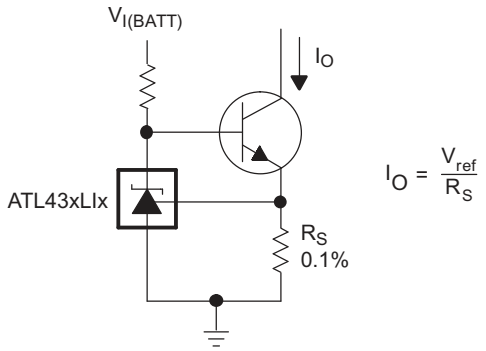


Figure 40. Precision Constant-Current Sink

12 Power Supply Recommendations

When using ATL43xLIx as a Linear Regulator to supply a load, designers will typically use a bypass capacitor on the output/cathode pin. When doing this, be sure that the capacitance is within the stability criteria shown in Figure 13.

To not exceed the maximum cathode current, be sure that the supply voltage is current limited. Also, be sure to limit the current being driven into the Ref pin, as not to exceed its absolute maximum rating.

For applications shunting high currents, pay attention to the cathode and anode trace lengths, adjusting the width of the traces to have the proper current density.

13 Layout

13.1 Layout Guidelines

Bypass capacitors should be placed as close to the part as possible. Current-carrying traces need to have widths appropriate for the amount of current they are carrying; in the case of the ATL43xLIx, these currents will be low.

13.2 SOT23-3 Layout Example

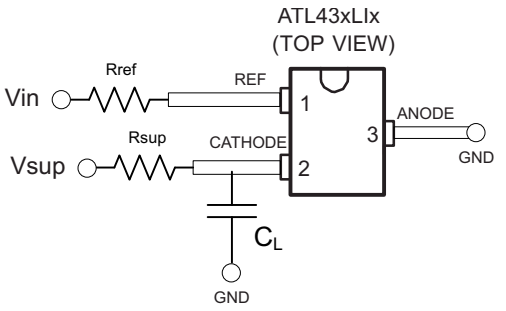


Figure 41. DBZ Layout Example

13.3 X2SON (DQN) Layout Example

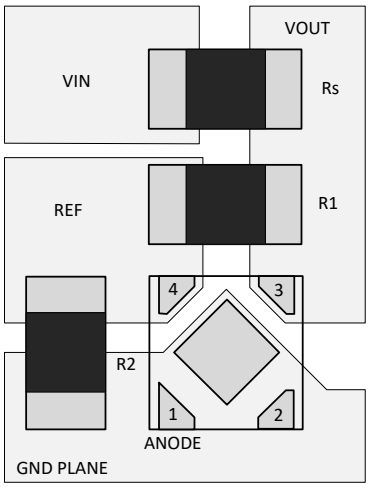


Figure 42. DQN Layout Example

13.4 Thermal Considerations

The thermal performance of the ATL431LI will depend on the power dissipation, thermal resistance, and ambient temperature. The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC thermal metrics are given in the *Specifications* table.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element. For a ATL431LI, the pass element voltage drop will be across the cathode and anode as shown in Equation 5. In certain packages, like the DQN package, the thermal metrics will vary with how the thermal pad is connected. The DQN package is designed to be soldered to a thermal pad on the board. It is reccomended that the DQN thermal pad is conencted to a thermal dissipative section of the PCB if the ATL431LI in DQN package is expected to dissipate a significant amount of power. It is reccomended to use large biasing resistors to keep the cathode current low on the ATL431LI for better thermal performance. For more information on designing and manufacturing with DQN, see Texas Instruments literature number SLUA271 and SCEA055. For reliable operation, limit junction temperature to 125°C (maximum) or its respective temperature maximum from the Reccomended Operating Conditions.

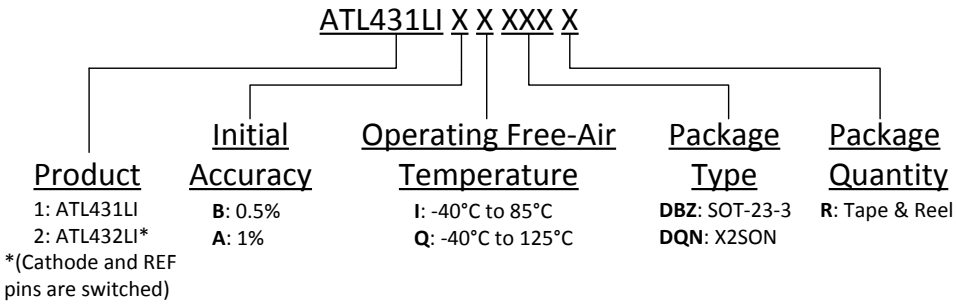
$$P_D = (V_{KA} - V_{ANODE}) / I_{KA} \quad (5)$$

14 Device and Documentation Support

14.1 Documentation Support

14.1.1 Device Nomenclature

TI assigns suffixes and prefixes to differentiate all the combinations of the ATL43xLI family. More details and possible orderable combinations are located in the Package Option Addendum.



14.1.2 Related Documentation

For related documentation see the following:

- *Understanding Stability Boundary Conditions Charts in TL431, TL432 Data Sheet*, SLVA482
- *Setting the Shunt Voltage on an Adjustable Shunt Regulator*, SLVA445

14.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 5. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ATL431LI	Click here	Click here	Click here	Click here	Click here
ATL432LI	Click here	Click here	Click here	Click here	Click here

14.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

14.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

14.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ATL431LIAIDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	1TUP	Samples
ATL431LIAIDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	IA	Samples
ATL431LIAQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1BHP	Samples
ATL431LIAQDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QA	Samples
ATL431LIBIDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	1TVP	Samples
ATL431LIBIDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	IB	Samples
ATL431LIBQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1BIP	Samples
ATL431LIBQDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QB	Samples
ATL432LIAIDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	1TWP	Samples
ATL432LIAQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1BJP	Samples
ATL432LIBIDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	1TXP	Samples
ATL432LIBQDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1BKP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

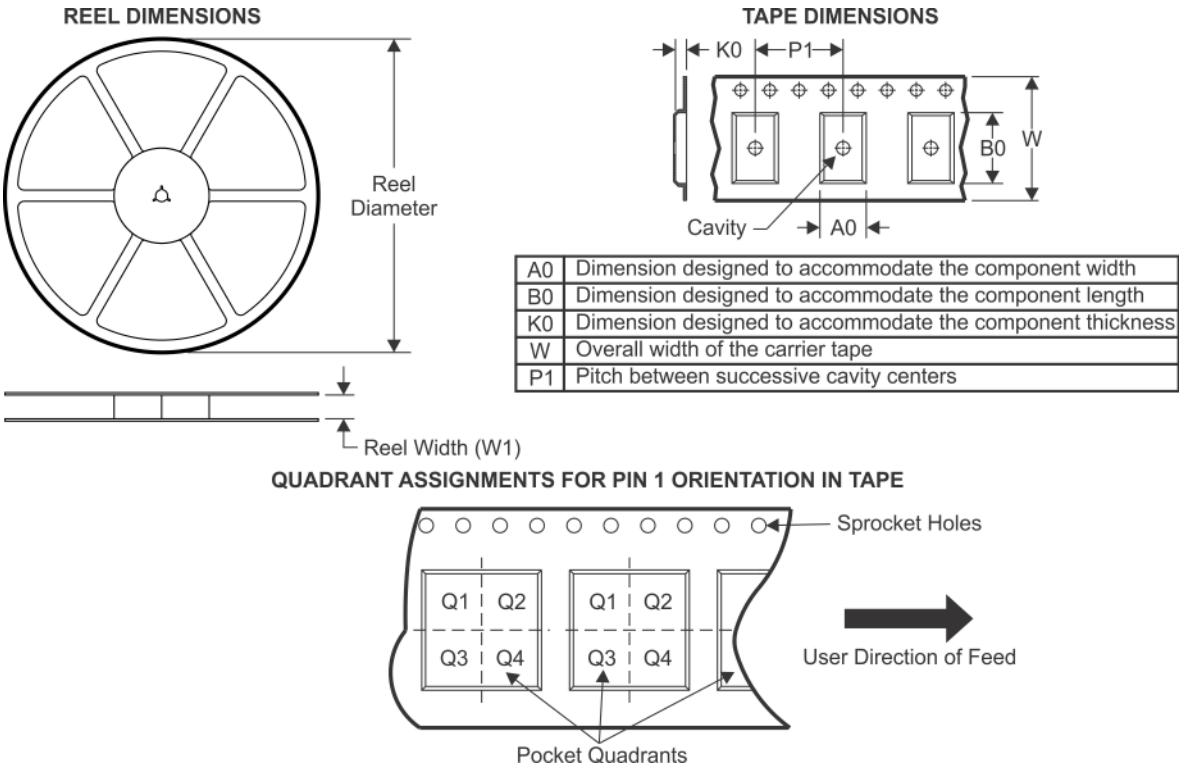
OTHER QUALIFIED VERSIONS OF ATL431LI, ATL432LI :

- Automotive: ATL431LI-Q1, ATL432LI-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



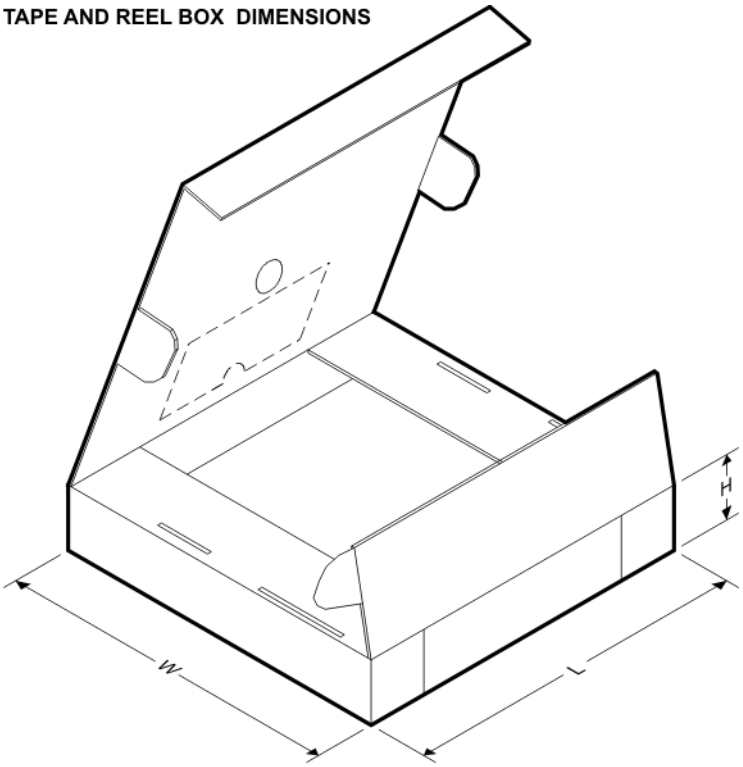
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ATL431LIAIDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
ATL431LIAIDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
ATL431LIAIDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
ATL431LIAQDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
ATL431LIAQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
ATL431LIAQDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
ATL431LIBIDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
ATL431LIBIDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
ATL431LIBIDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
ATL431LIBQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
ATL431LIBQDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
ATL431LIBQDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
ATL432LIAIDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
ATL432LIAIDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
ATL432LIAQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3
ATL432LIAQDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
ATL432LIBIDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
ATL432LIBIDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ATL432LIBQDBZR	SOT-23	DBZ	3	3000	178.0	9.2	3.15	2.77	1.22	4.0	8.0	Q3
ATL432LIBQDBZR	SOT-23	DBZ	3	3000	178.0	9.0	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ATL431LIAIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL431LIAIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL431LIAIDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
ATL431LIAQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL431LIAQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL431LIAQDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
ATL431LIBIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL431LIBIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL431LIBIDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
ATL431LIBQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL431LIBQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL431LIBQDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
ATL432LIAIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL432LIAIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL432LIAQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0

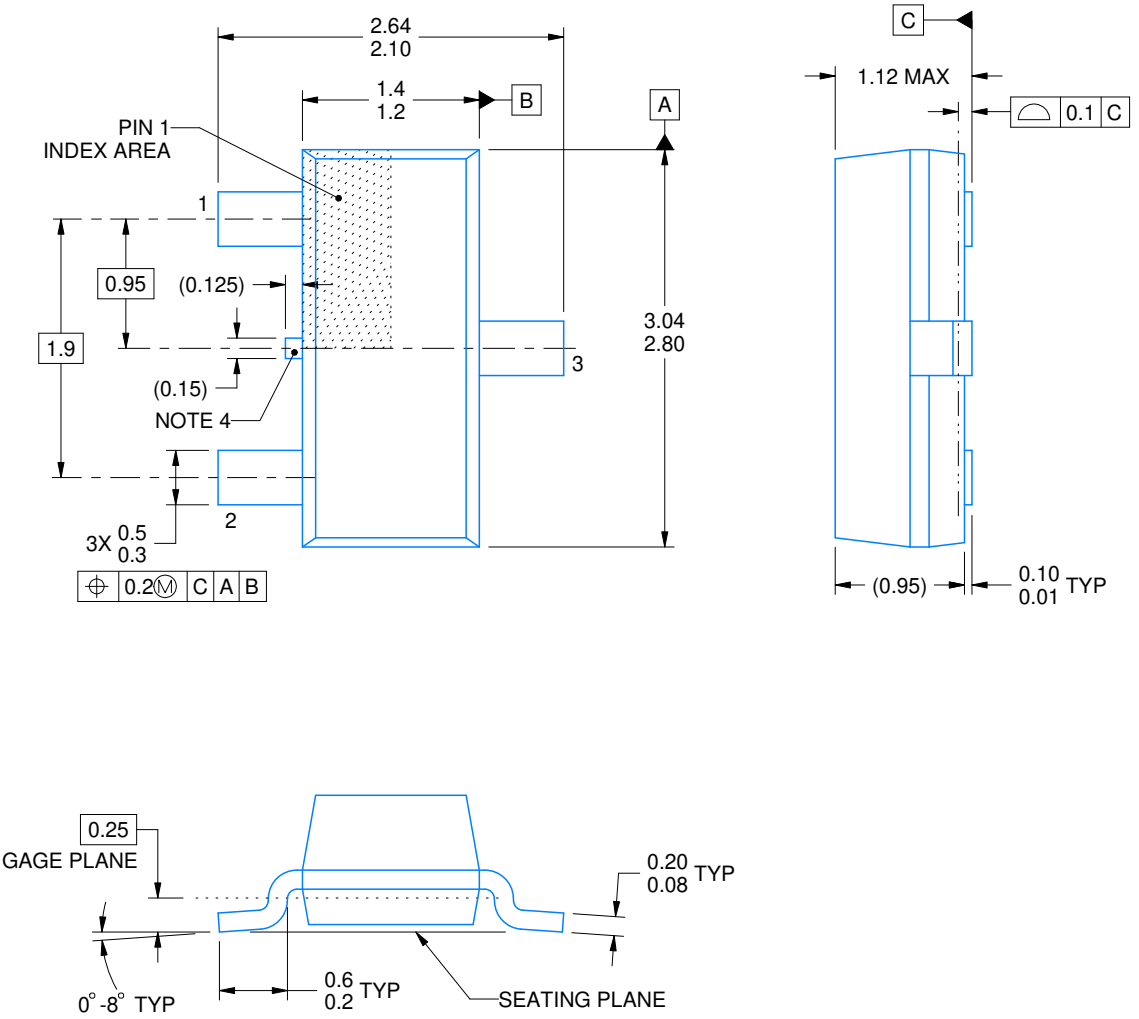
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ATL432LIAQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL432LIBIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL432LIBIDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL432LIBQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0
ATL432LIBQDBZR	SOT-23	DBZ	3	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

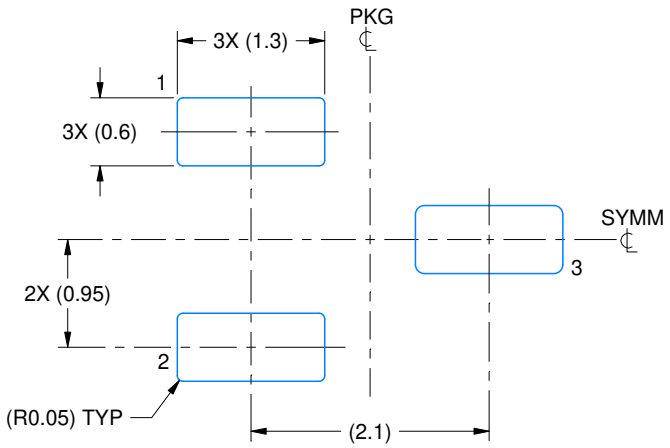
SMALL OUTLINE TRANSISTOR



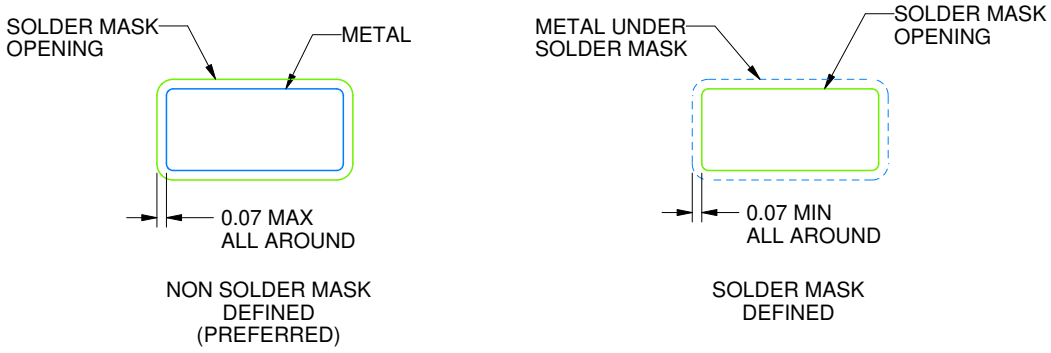
4214838/D 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:15X

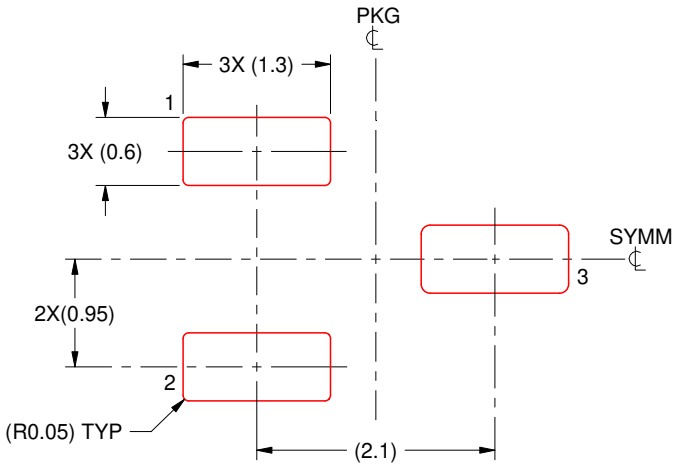


SOLDER MASK DETAILS

4214838/D 03/2023

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/D 03/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DQN 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

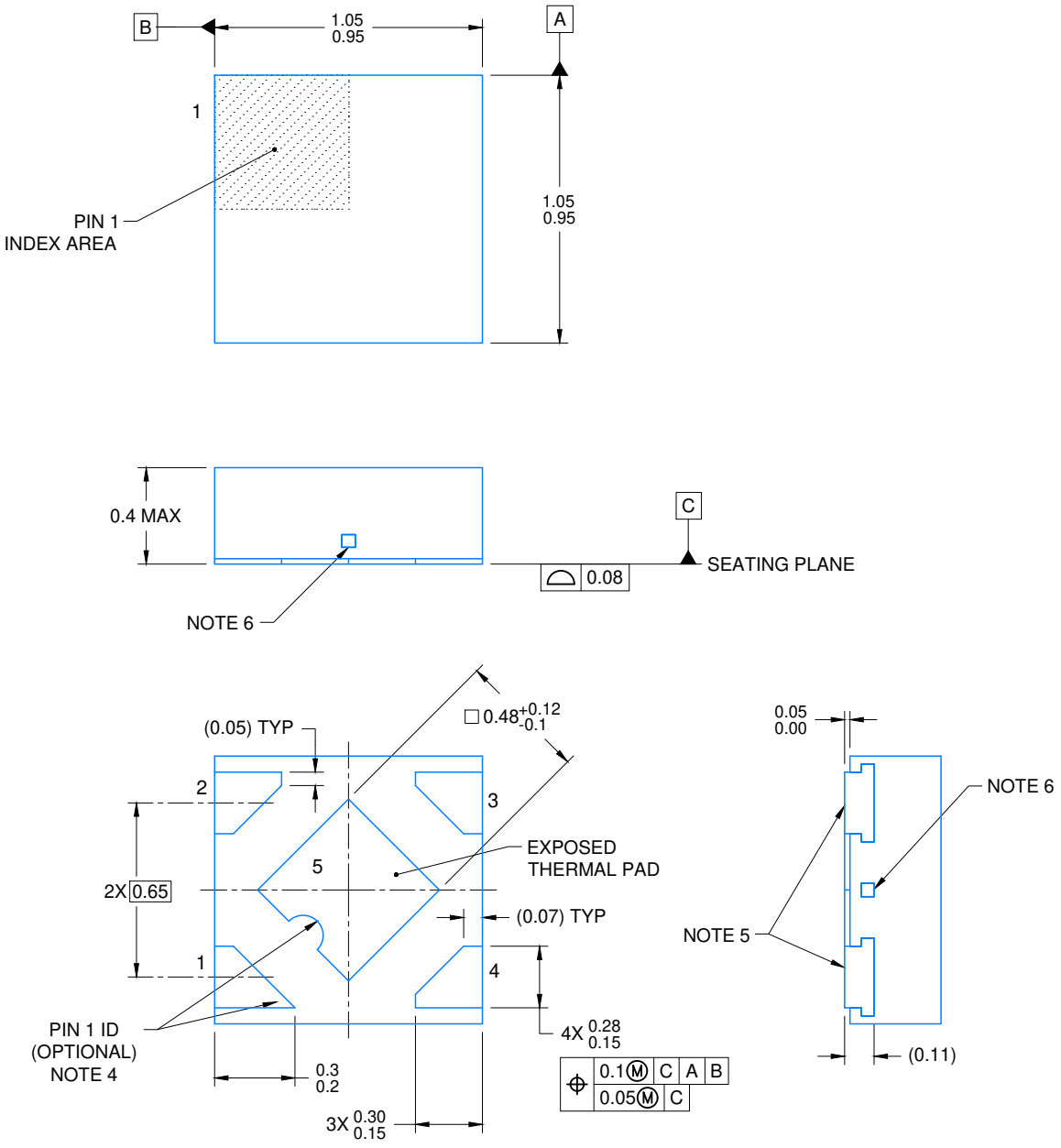
4210367/F

PACKAGE OUTLINE

DQN0004A

X2SON - 0.4 mm max height

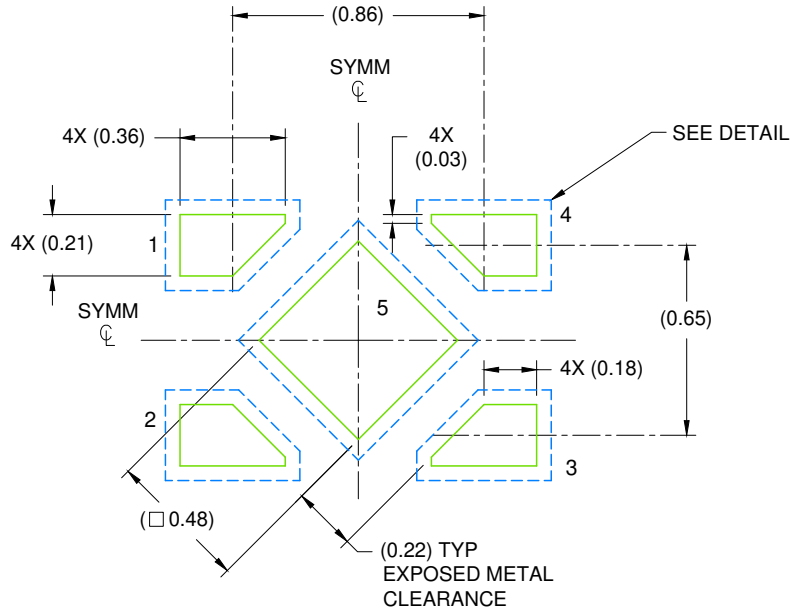
PLASTIC SMALL OUTLINE - NO LEAD



4215302/E 12/2016

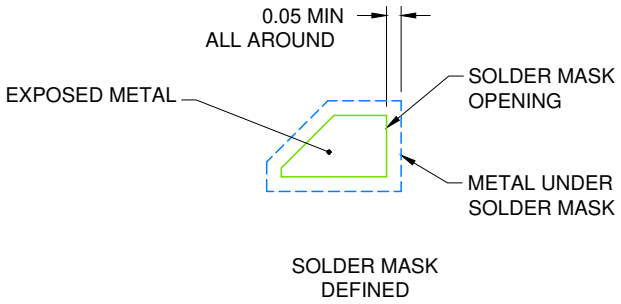
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE

SCALE: 40X

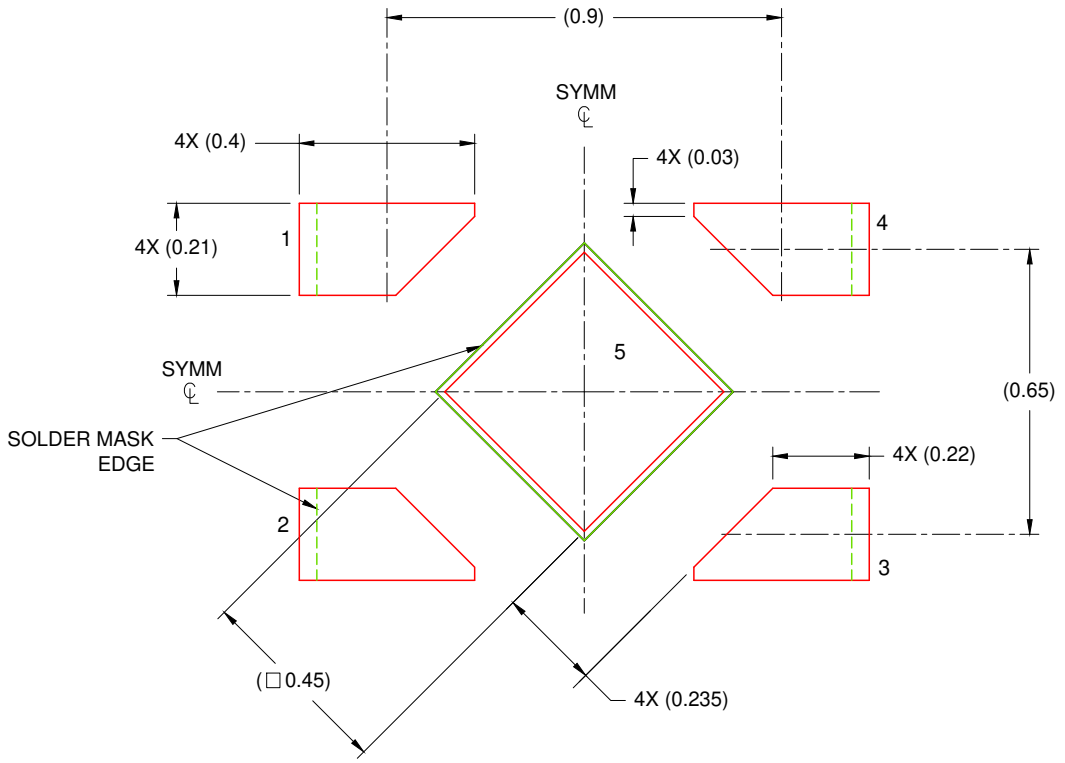


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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