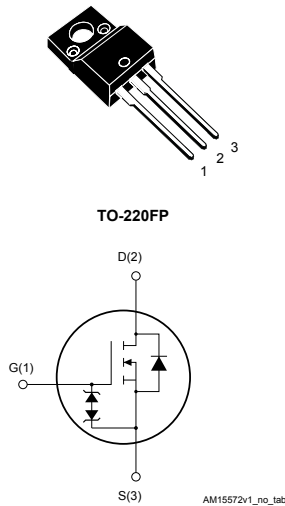


N-channel 600 V, 0.95 Ω typ., 5 A MDmesh™ DM2 Power MOSFET in a TO-220FP package



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STF6N60DM2	600 V	1.10 Ω	5 A	20 W

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM2 fast-recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Product status link

STF6N60DM2

Product summary

Order code	STF6N60DM2
Marking	6N60DM2
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	5	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	3.2	
$I_{DM}^{(1)}$	Drain current (pulsed)	20	A
P_{TOT}	Total power dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	20	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^\circ\text{C}$)	2.5	kV
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 5\text{ A}$, $di/dt = 900\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 480\text{ V}$.
3. $V_{DS} \leq 480\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	6.25	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	1.7	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	132	mJ

1. Pulse width limited by T_{jmax} .
2. starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

($T_{case} = 25\text{ °C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_{case} = 125\text{ °C}$ ⁽¹⁾			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 5	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 2.5\text{ A}$		0.95	1.10	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	274	-	pF
C_{oss}	Output capacitance		-	15	-	
C_{riss}	Reverse transfer capacitance		-	2	-	
$C_{oss\ eq.}$ ⁽¹⁾	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$	-	25	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	6.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	6.2	-	nC
Q_{gs}	Gate-source charge		-	1.8	-	
Q_{gd}	Gate-drain charge		-	2.7	-	

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 2.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	9.2	-	ns
t_r	Rise time		-	5.6	-	
$t_{d(off)}$	Turn-off delay time		-	12	-	
t_f	Fall time		-	19.6	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		20	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 5\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	60		ns
Q_{rr}	Reverse recovery charge		-	135		nC
I_{RRM}	Reverse recovery current		-	4.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	132		ns
Q_{rr}	Reverse recovery charge		-	429		nC
I_{RRM}	Reverse recovery current		-	6.5		A

1. Pulse width is limited by safe operating area.

2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

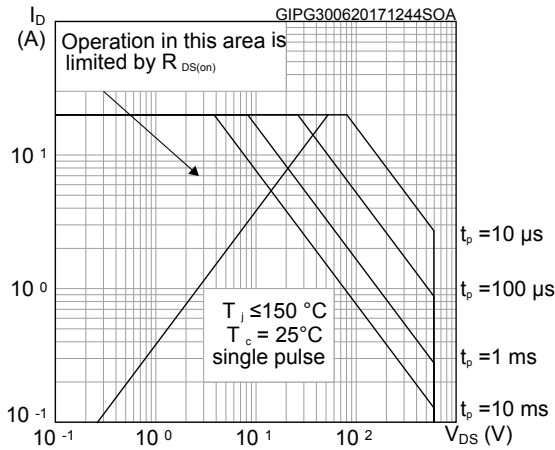


Figure 2. Thermal impedance

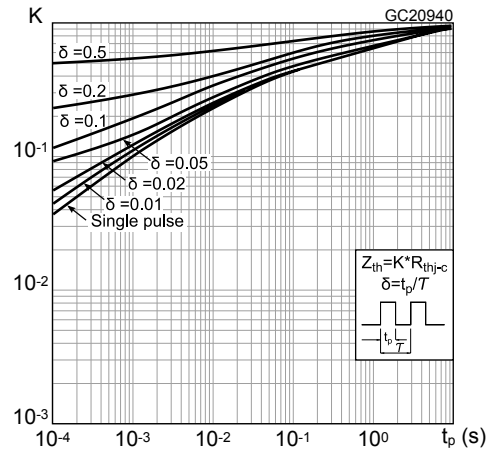


Figure 3. Output characteristics

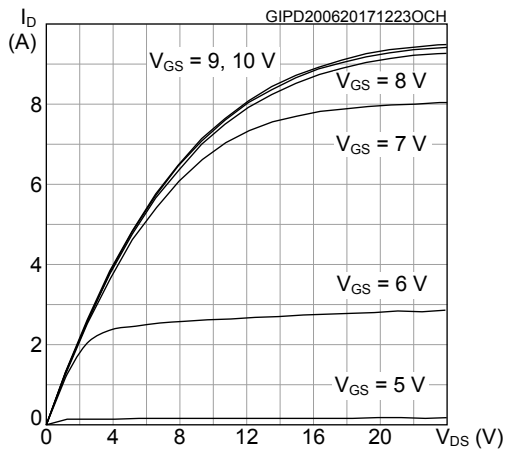


Figure 4. Transfer characteristics

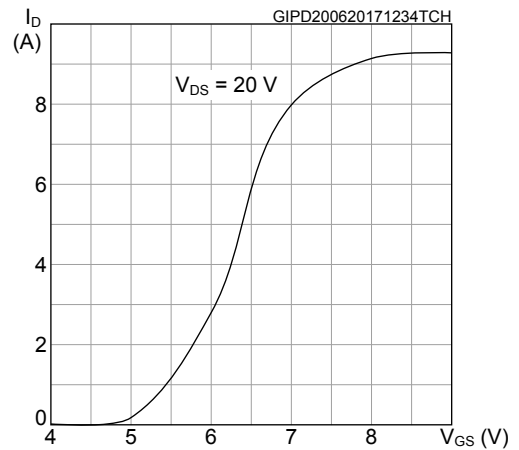


Figure 5. Gate charge vs gate-source voltage

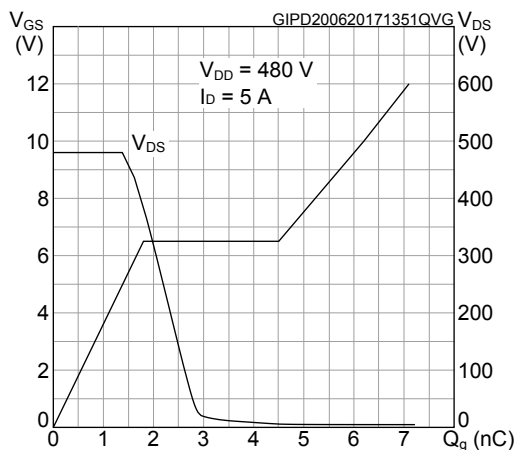


Figure 6. Static drain-source on-resistance

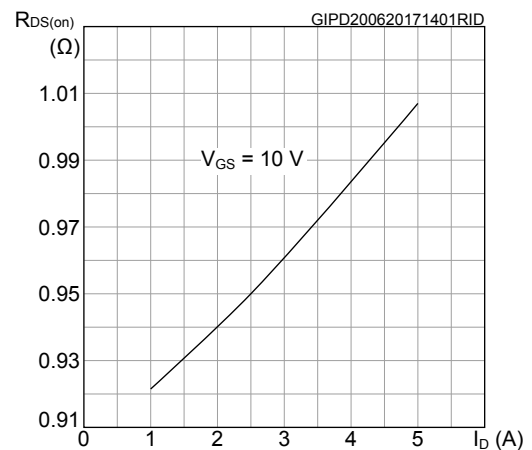


Figure 7. Capacitance variations

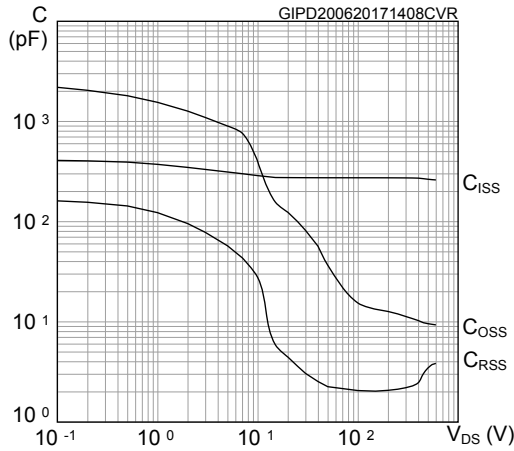


Figure 8. Output capacitance stored energy

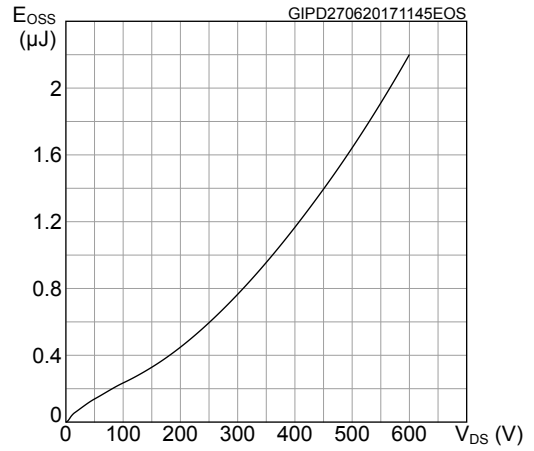


Figure 9. Normalized gate threshold voltage vs temperature

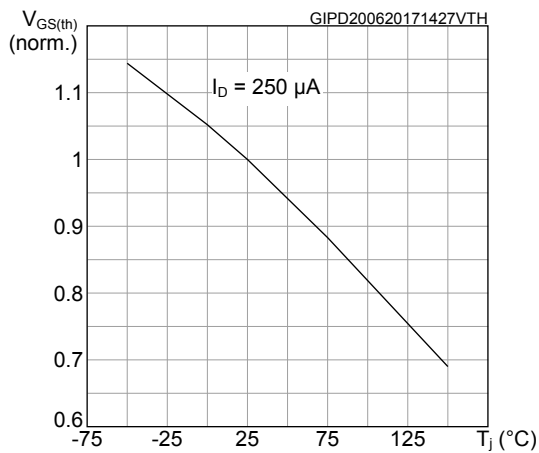


Figure 10. Normalized on-resistance vs temperature

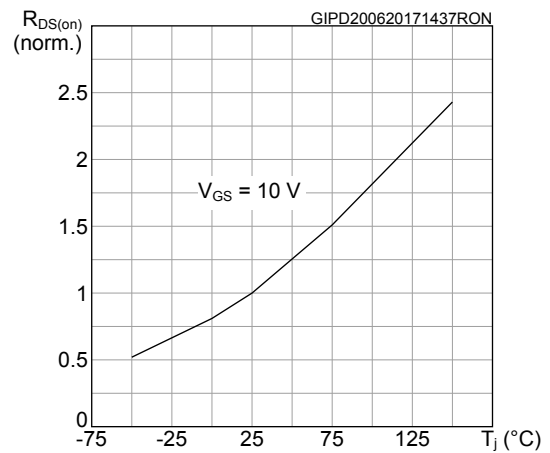


Figure 11. Source-drain diode forward characteristics

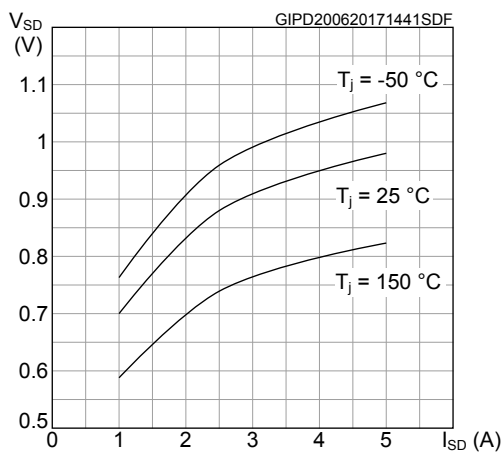
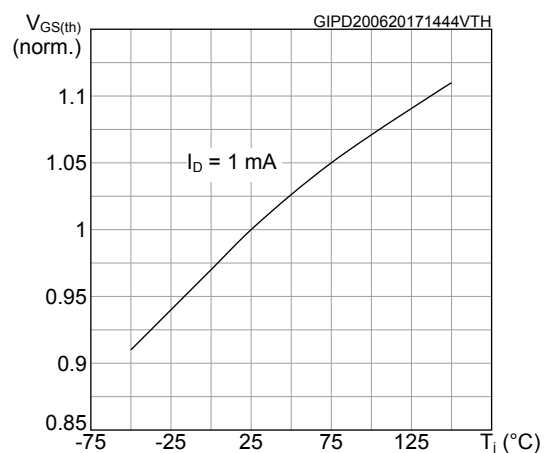
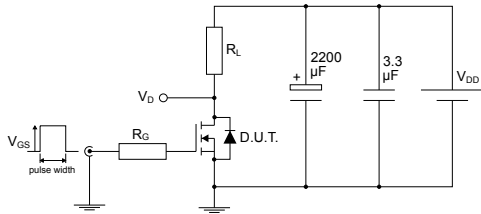


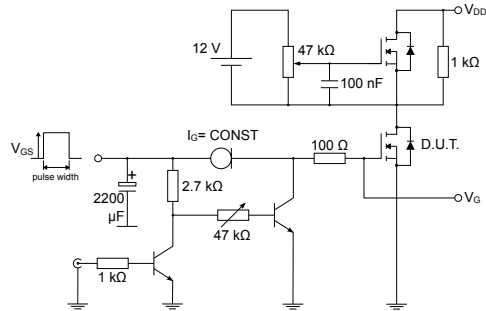
Figure 12. Normalized $V_{(BR)DSS}$ vs temperature



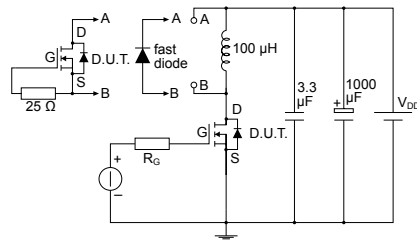
3 Test circuits

Figure 13. Test circuit for resistive load switching times


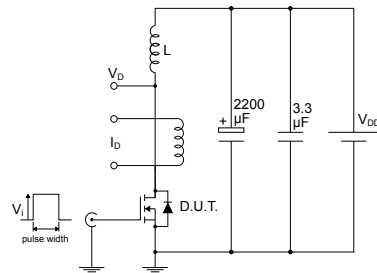
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Figure 14. Test circuit for gate charge behavior


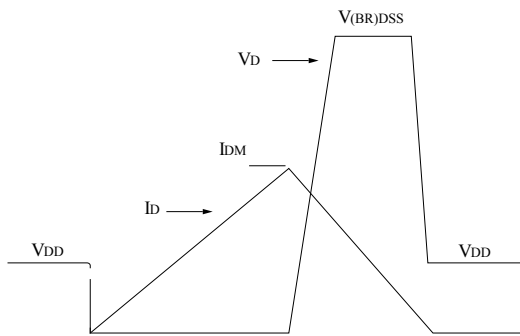
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Figure 15. Test circuit for inductive load switching and diode recovery times


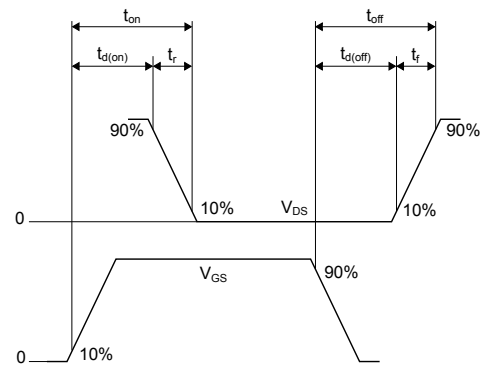
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


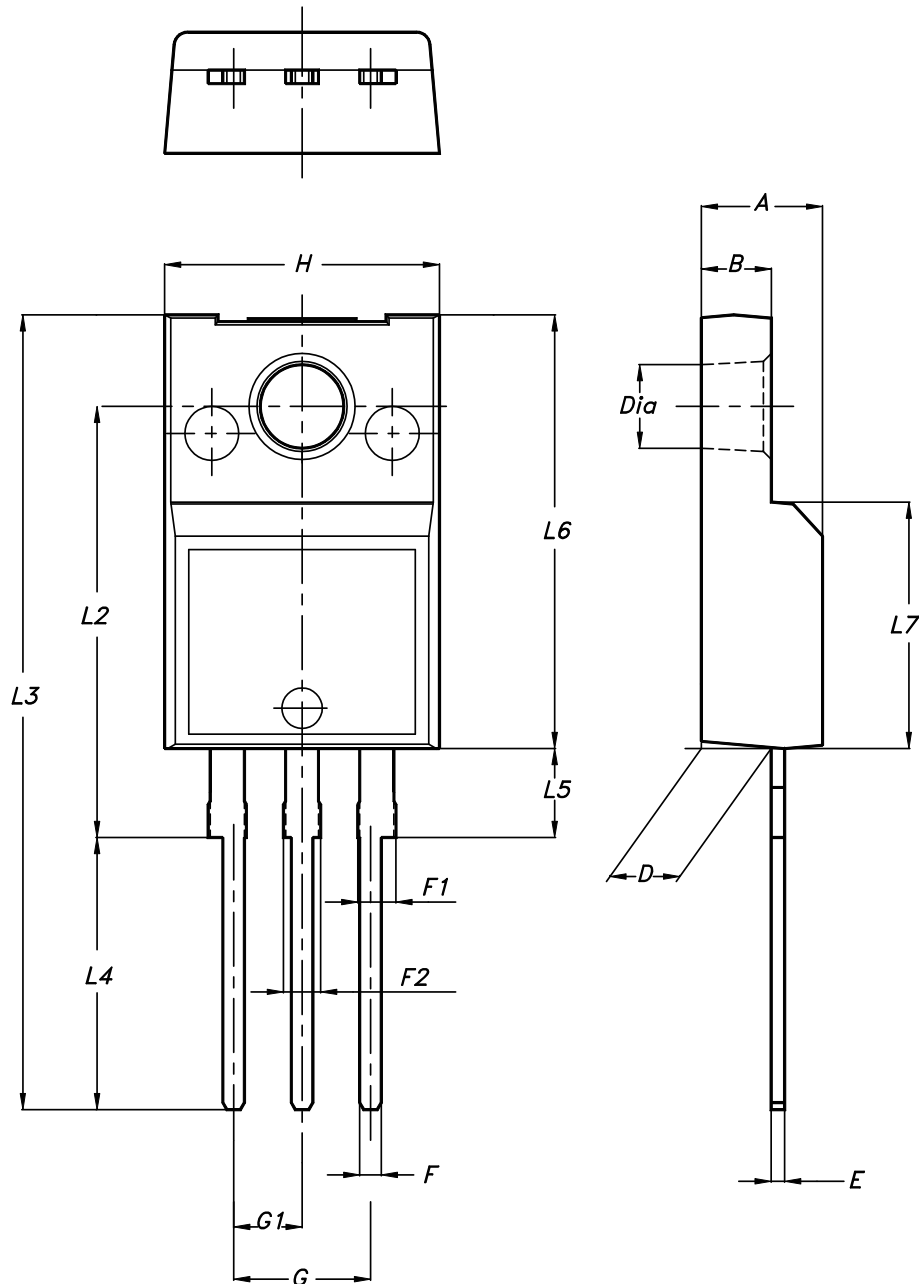
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP package information

Figure 19. TO-220FP package outline



7012510_Rev_13_B

Table 8. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

Revision history

Table 9. Document revision history

Date	Version	Changes
03-Jul-2017	1	First release
12-Jun-2018	2	Updated Table 1. Absolute maximum ratings, Table 2. Thermal data and Table 5. Dynamic.
16-Mar-2020	3	Updated Section Features . Minor text change to improve the readability.

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