

## 74F651 • 74F652 Transceivers/Registers

### General Description

These devices consist of bus transceiver circuits with D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to HIGH logic level. Output Enable pins (OEAB, OEBA) are provided to control the transceiver function.

### Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
  - 'F651 inverting
  - 'F652 non-inverting
- Guaranteed 4000V minimum ESD protection

### Ordering Code:

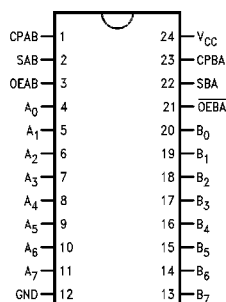
Commercial	Military	Package Number	Package Description
74F651SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F651SDM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
74F651SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54F651FM (Note 2)	W24C	24-Lead Cerpack
	54F651LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C
74F652SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
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	54F652FM (Note 2)	W24C	24-Lead Cerpack
	54F652LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

**Note 1:** Devices also available in 13" reel. Use suffix = SCX

**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB

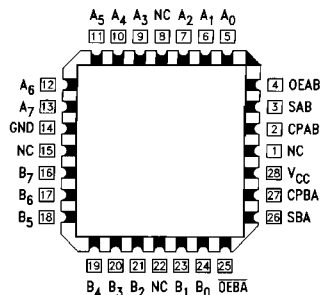
### Connection Diagrams

Pin Assignment  
DIP, SOIC and Flatpak



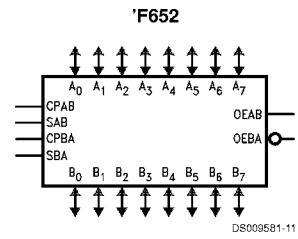
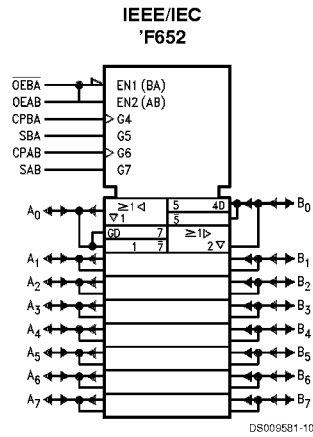
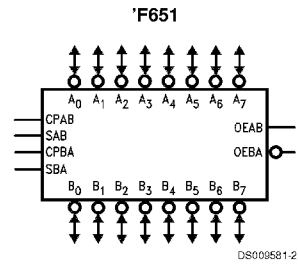
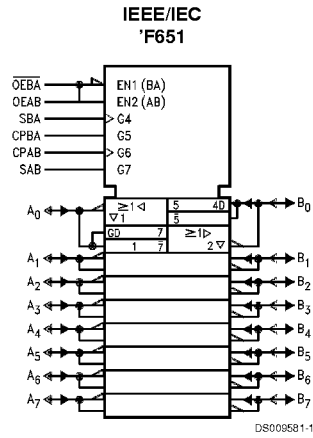
DS009581-3

Pin Assignment  
for LCC



DS009581-4

## Logic Symbols

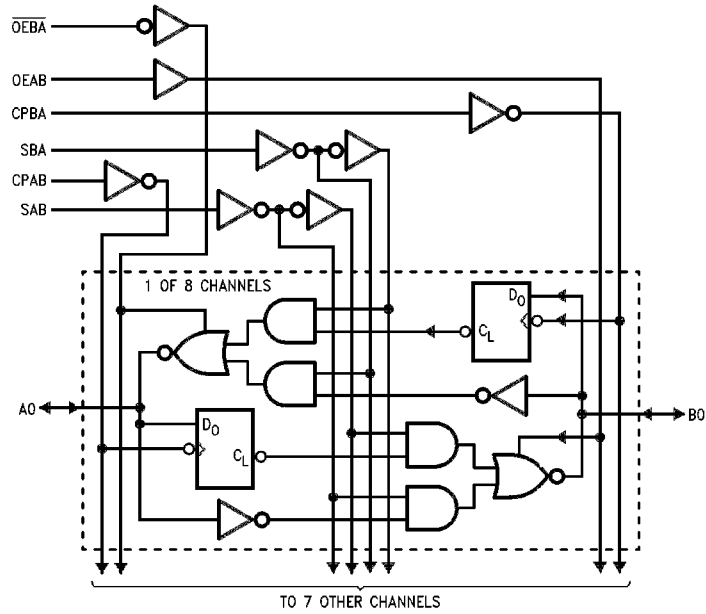


## Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0-A_7, B_0-B_7$	A and B Inputs/ 3-STATE Outputs	1.0/1.0 600/106.6 (80)	20 $\mu A$ /-0.6 mA -12 mA/64 mA (48 mA)
CPAB, CPBA	Clock Inputs	1.0/1.0	20 $\mu A$ /-0.6 mA
SAB, SBA	Select Inputs	1.0/1.0	20 $\mu A$ /-0.6 mA
OEAB, OEBA	Output Enable Inputs	1.0/1.0	20 $\mu A$ /-0.6 mA

## Logic Diagrams

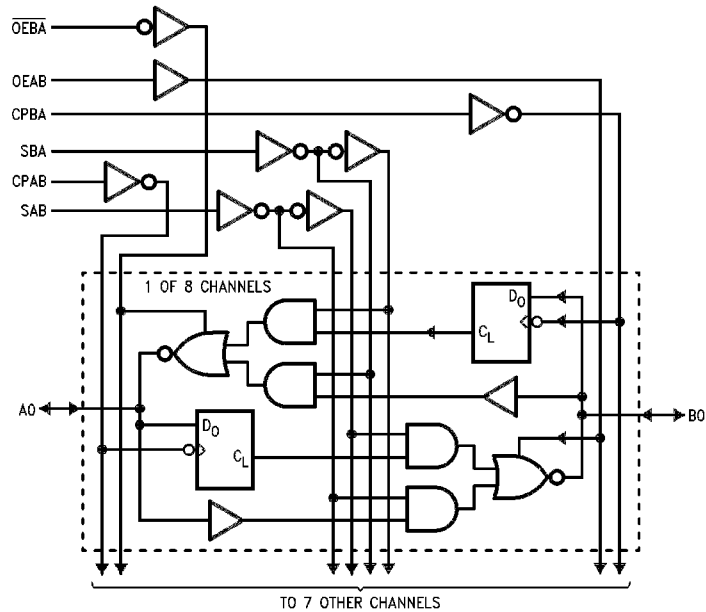
'F652



DS006581-6

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

'F651



DS006581-12

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Functional Description

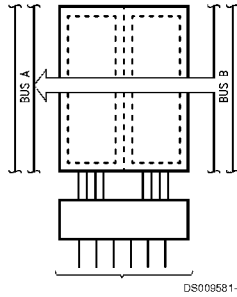
In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB, SBA) controls can multiplex stored and real-time.

The examples in *Figure 1* demonstrate the four fundamental bus-management functions that can be performed with the Octal bus transceivers and receivers.

Data on the A or B data bus, or both can be stored in the internal D flip-flop by LOW to HIGH transitions at the appropri-

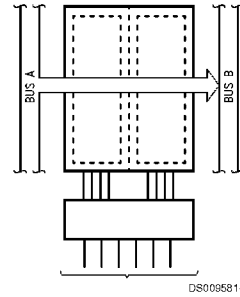
ate Clock Inputs (CPAB, CPBA) regardless of the Select or Output Enable Inputs. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D flip-flops by simultaneously enabling OEAB and OEBA. In this configuration each Output reinforces its Input. Thus when all other data sources to the two sets of bus lines are in a HIGH impedance state, each set of bus lines will remain at its last state.

**Note A: Real-Time Transfer Bus B to Bus A**



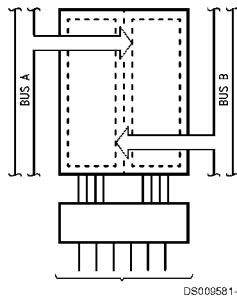
OEAB	OEBA	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

**Note B: Real-Time Transfer Bus A to Bus B**



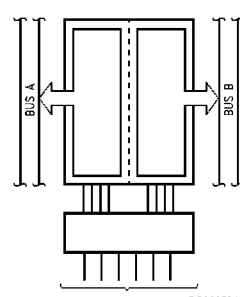
OEAB	OEBA	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

**Note C: Storage**



OEAB	OEBA	CPAB	CPBA	SAB	SBA
X	H	↗	X	X	X
L	X	X	↗	X	X
L	H	↗	↗	X	X

**Note D: Transfer Storage Data to A or B**



OEAB	OEBA	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	X

FIGURE 1.

## Functional Description (Continued)

Inputs						Inputs/Outputs (Note 3)		Operating Mode
OEAB	OEBA	CPAB	CPBA	SAB	SBA	A <sub>0</sub> thru A <sub>7</sub>	B <sub>0</sub> thru B <sub>7</sub>	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↗	↗	X	X			Store A and B Data
X	H	↗	H or L	X	X	Input	Not Specified	Store A, Hold B
H	H	↗	↗	X	X	Input	Output	Store A in Both Registers
L	X	H or L	↗	X	X	Not Specified	Input	Hold A, Store B
L	L	↗	↗	X	X	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Store B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = LOW to HIGH Clock Transition

**Note 3:** The data output functions may be enabled or disabled by various signals at OEAB or OEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW to HIGH transition on the clock inputs.

## Absolute Maximum Ratings (Note 4)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 5)	-0.5V to +7.0V
Input Current (Note 5)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

ESD Last Passing Voltage (Min)

4000V

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

**Note 4:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 5:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

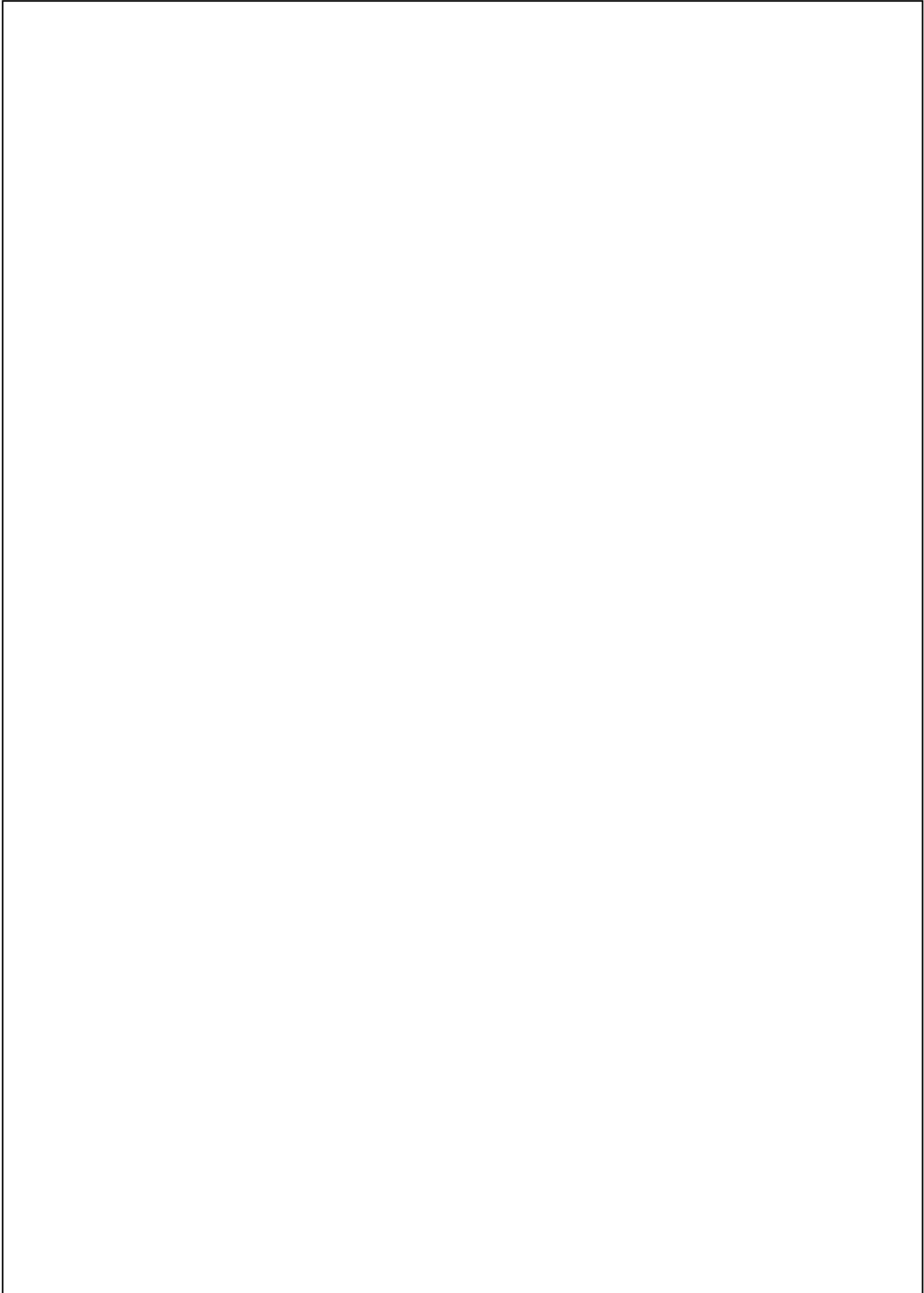
Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				V	Min	I <sub>IN</sub> = -18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.0		V	Min	I <sub>OH</sub> = -12 mA (A <sub>n</sub> , B <sub>n</sub> )
	74F 10% V <sub>CC</sub>	2.0					I <sub>OH</sub> = -15 mA (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>	0.55		V	Min	I <sub>OL</sub> = 48 mA (A <sub>n</sub> , B <sub>n</sub> )
	74F 10% V <sub>CC</sub>	0.55					I <sub>OL</sub> = 64 mA (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current	54F	20.0		μA	Max	V <sub>IN</sub> = 2.7V
	74F	5.0					(Non I/O Pins)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F	100		μA	Max	V <sub>IN</sub> = 7.0V
	74F	7.0					
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)	54F	1.0		mA	Max	V <sub>IN</sub> = 5.5V
	74F	0.5					(A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current	54F	250		μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
	74F	50					
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA
							All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F	3.75		μA	0.0	V <sub>I<sub>OD</sub></sub> = 150 mV
							All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				mA	Max	V <sub>IN</sub> = 0.5V (Non I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current				μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current				μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	-100		-225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test				μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current	105		135	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current	118		150	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current	115		150	mA	Max	V <sub>O</sub> = HIGH Z

## AC Electrical Characteristics

Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Max	Min	Max	Min	Max	
$f_{\text{max}}$	Max. Clock Frequency	90		75		90		MHz
$t_{\text{PLH}}$	Propagation Delay	2.0	7.0	2.0	8.5	2.0	8.0	ns
$t_{\text{PHL}}$	Clock to Bus	2.0	8.0	2.0	9.5	2.0	9.0	
$t_{\text{PLH}}$	Propagation Delay	2.0	8.5	1.0	9.0	2.0	9.0	ns
$t_{\text{PHL}}$	Bus to Bus ('F651)	1.0	7.5	1.0	8.0	1.0	8.0	
$t_{\text{PLH}}$	Propagation Delay	1.0	7.0	1.0	8.0	1.0	7.5	ns
$t_{\text{PHL}}$	Bus to Bus ('F652)	1.0	6.5	1.0	8.0	1.0	7.0	
$t_{\text{PLH}}$	Propagation Delay	2.0	8.5	2.0	11.0	2.0	9.5	ns
$t_{\text{PHL}}$	SBA or SAB to A or B	2.0	8.0	2.0	10.0	2.0	9.0	

## AC Operating Requirements

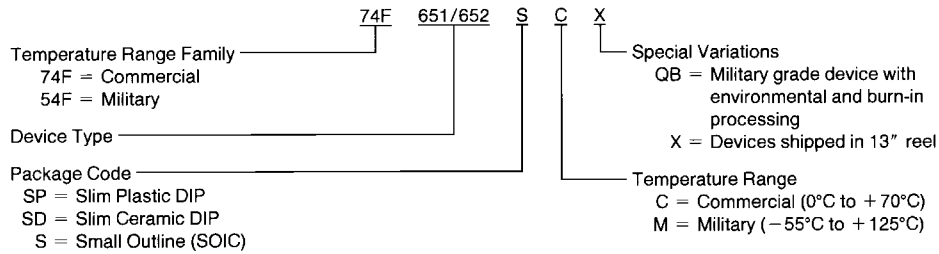
Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_{\text{PZH}}$	Enable Time	2.0	9.5	2.0	10.0	2.0	10.0	ns
$t_{\text{PZL}}$	*OEBA to A	2.0	12.0	2.0	10.0	2.0	12.5	
$t_{\text{PHZ}}$	Disable Time	1.0	7.5	1.0	9.0	1.0	8.0	
$t_{\text{PLZ}}$	*OEBA to A	2.0	8.5	1.0	9.0	2.0	9.0	
$t_{\text{PZH}}$	Enable Time	2.0	9.5	2.0	10.0	2.0	10.0	
$t_{\text{PZL}}$	OEAB to B	3.0	13.0	2.0	12.0	3.0	14.0	
$t_{\text{PHZ}}$	Disable Time	2.0	9.0	1.0	9.0	2.0	10.0	ns
$t_{\text{PLZ}}$	OEAB to B	2.0	10.5	1.0	12.0	2.0	11.0	
$t_s(\text{H})$	Setup Time, HIGH or	5.0		5.0		5.0		ns
$t_s(\text{L})$	LOW, Bus to Clock	5.0		5.0		5.0		
$t_h(\text{H})$	Hold Time, HIGH or	2.0		2.5		2.0		ns
$t_h(\text{L})$	LOW, Bus to Clock	2.0		2.5		2.0		
$t_w(\text{H})$	Clock Pulse Width	5.0		5.0		5.0		ns
$t_w(\text{L})$	HIGH or LOW	5.0		5.0		5.0		





## Ordering Information

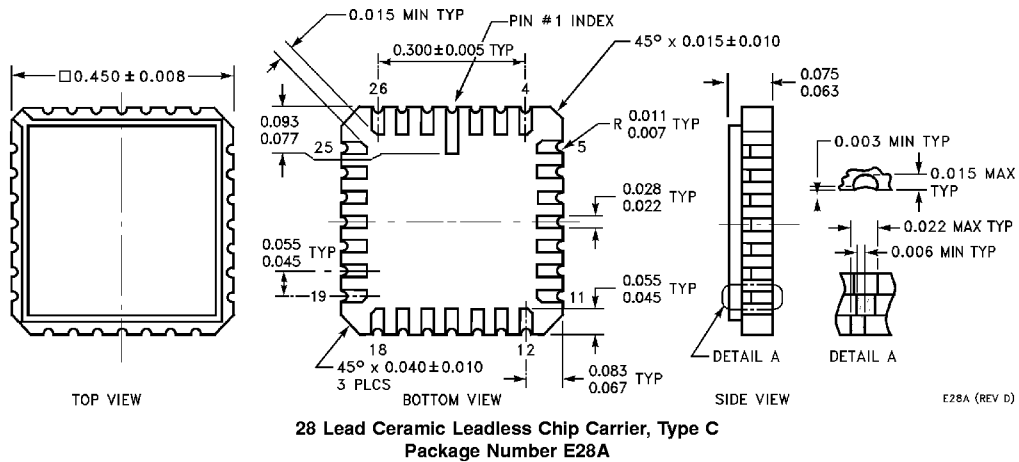
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



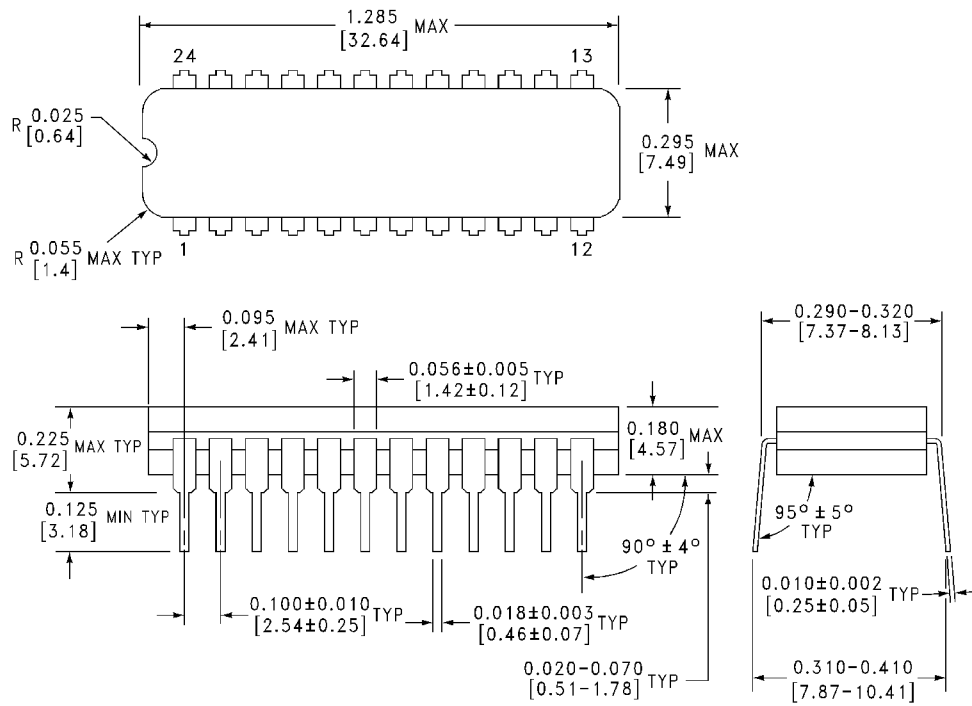
DS009581-14

## Physical Dimensions

inches (millimeters) unless otherwise noted



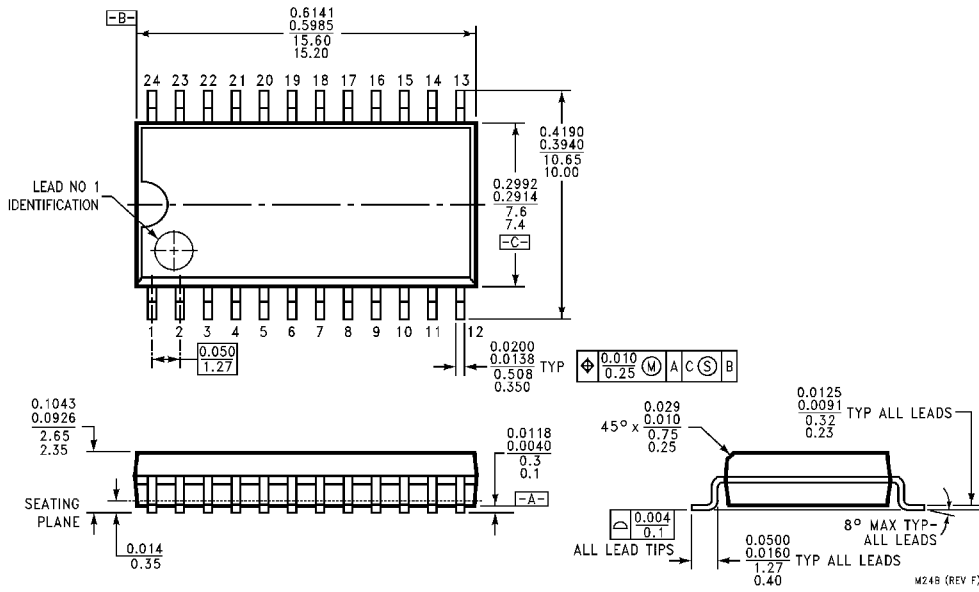
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



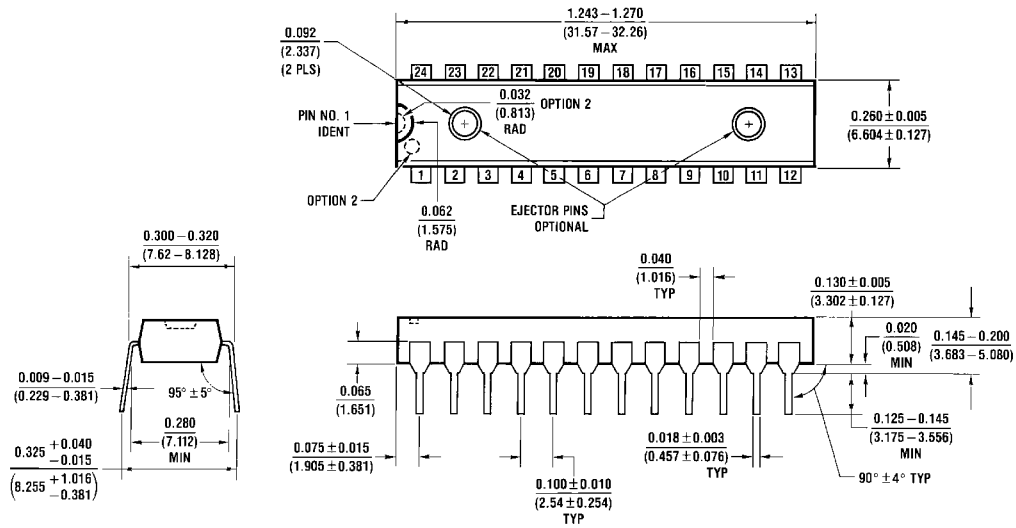
J24F (REV. H)

**24 Lead (0.300" Wide) Ceramic Dual-In-Line Package (SD)  
Package Number J24F**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

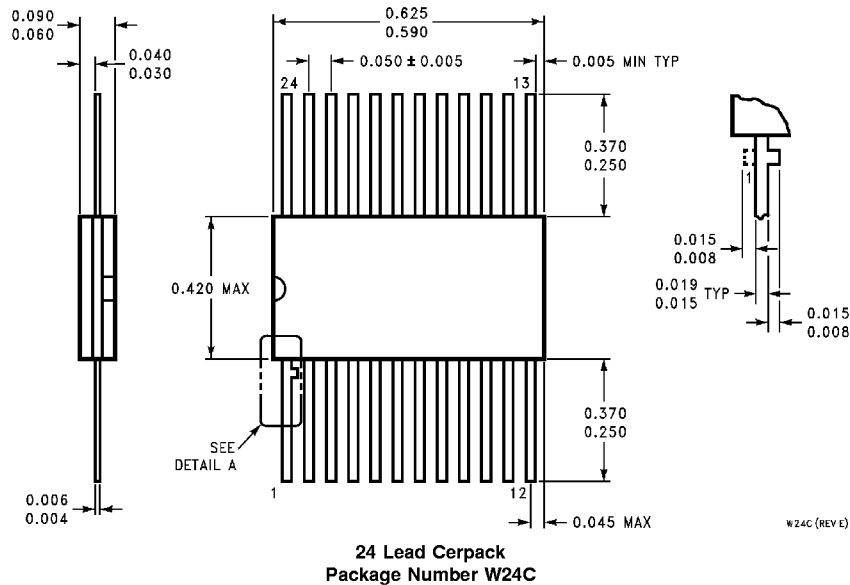


**24 Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)  
Package Number M24B**



**24 Lead (0.300" Wide) Molded Dual-In-Line Package (SP)  
Package Number N24C**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



W24C (REV E)

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Deutsch Tel: +49 (0) 8 141-35-0  
English Tel: +44 (0) 1 793-85-68-56  
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**Fairchild Semiconductor Hong Kong Ltd.**  
13th Floor, Straight Block,  
Ocean Centre, 5 Canton Rd.  
Tsimshatsui, Kowloon  
Hong Kong  
Tel: +852 2737-7200  
Fax: +852 2314-0061

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