CeraLink

Capacitors for fast-switching semiconductors

Series/Type: **Solder pin (SP) series**
Ordering code: **B58033***

Date: 2023-08-20
Version: 6.3

Applications

- Power converters and inverters
- DC link/snubber capacitor for power converters and inverters

Features

- High ripple current capability
- High temperature robustness
- Low equivalent serial inductance (ESL)
- Low equivalent serial resistance (ESR)
- Low power loss
- Low dielectric absorption
- Optimized for high frequencies up to several 100 kHz
- Increasing capacitance with DC bias up to operating voltage
- High capacitance density
- Minimized dielectric loss at high temperatures
- Qualification based on AEC-Q200 rev. D

Construction

- RoHS-compatible PLZT ceramic (lead lanthanum zirconium titanate)
- Copper inner electrodes
- Silver outer electrodes
- Silver coated copper pins
- Silicone based casting compound according to UL 94 V-0
- Plastic housing according to UL 94 V-0

General technical data

Dissipation factor	$\tan\delta$	< 0.02	
Insulation resistance	$R_{ins, typ}$ [1)]	> 1	GΩ
Operating device temperature	T_{device}	-40 … +150	°C
Weight of device		approx. 31	g

1) Typical insulation resistance, measured at operating voltage V_{op} and measurement time > 240 s, +25 °C

Electrical specifications and ordering codes

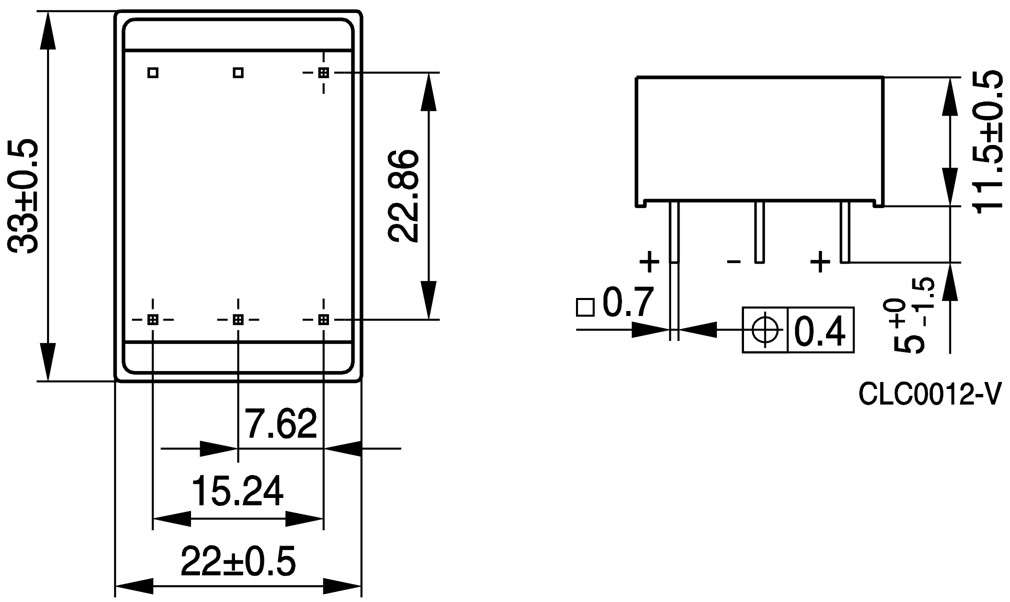
Type	$V_{pk,max}$ V	V_R V	V_{op} V	$C_{nom,typ}$ µF	$C_{eff,typ}$ µF	C_0 µF	Ordering code
SP500	650	500	400	20	12	6.5 ±20%	B58033I5206M001
SP700	1000	700	600	10	5	2.8 ±20%	B58033I7106M001
SP900	1300	900	800	5	3	1.5 ±20%	B58033I9505M001 *)

*) This part is affected by "Dual Use" regulations according to the law of the country the production site is located in. Deliveries of such products are subject to prior approval of the respective local authorities based on customer declarations. The delivery to certain countries may be restricted.

Aging

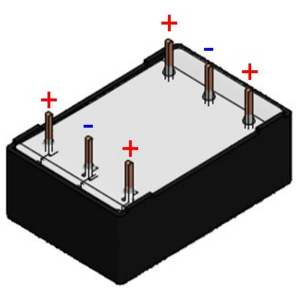
The capacitance has an aging behavior which shows a decrease of capacitance with time.
The typical aging rate is about 2.5% per logarithmic decade in hours.

Dimensional drawings



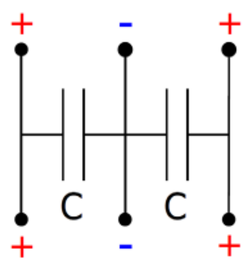
Dimensions in mm (values without tolerances are typical)

Polarity



Note that polarity is only for incoming inspection purposes, and it does not affect operation. If put under reverse rated voltage V_R, CeraLink® is repoled and works identically, see our *CeraLink Technical Guide* for further details.

Equivalent circuit diagram



Marking of components

Manufacturer's logo
CeraLink type
Nominal capacitance
Rated voltage

Typical values as a design reference for CeraLink applications

V_R V	**ESR** 0 V DC, 0.5 V AC (RMS), 25 °C, 1 kHz **mΩ**	**ESR** 0 V DC, 0.5 V AC (RMS), 25 °C, 100 kHz **mΩ**	**ESL** **nH**	I_{op} 1) 100 kHz T_{amb} = 85 °C A_{RMS}	I_{op} 1) 100 kHz T_{amb} = 105 °C A_{RMS}
500	275	4	4	41	32
700	550	11	4	33	27
900	1000	18	4	26	24

1) Normal operating current without forced cooling at T_{device} = +150 °C. Higher values permissible at reduced lifetime.

Application Notes

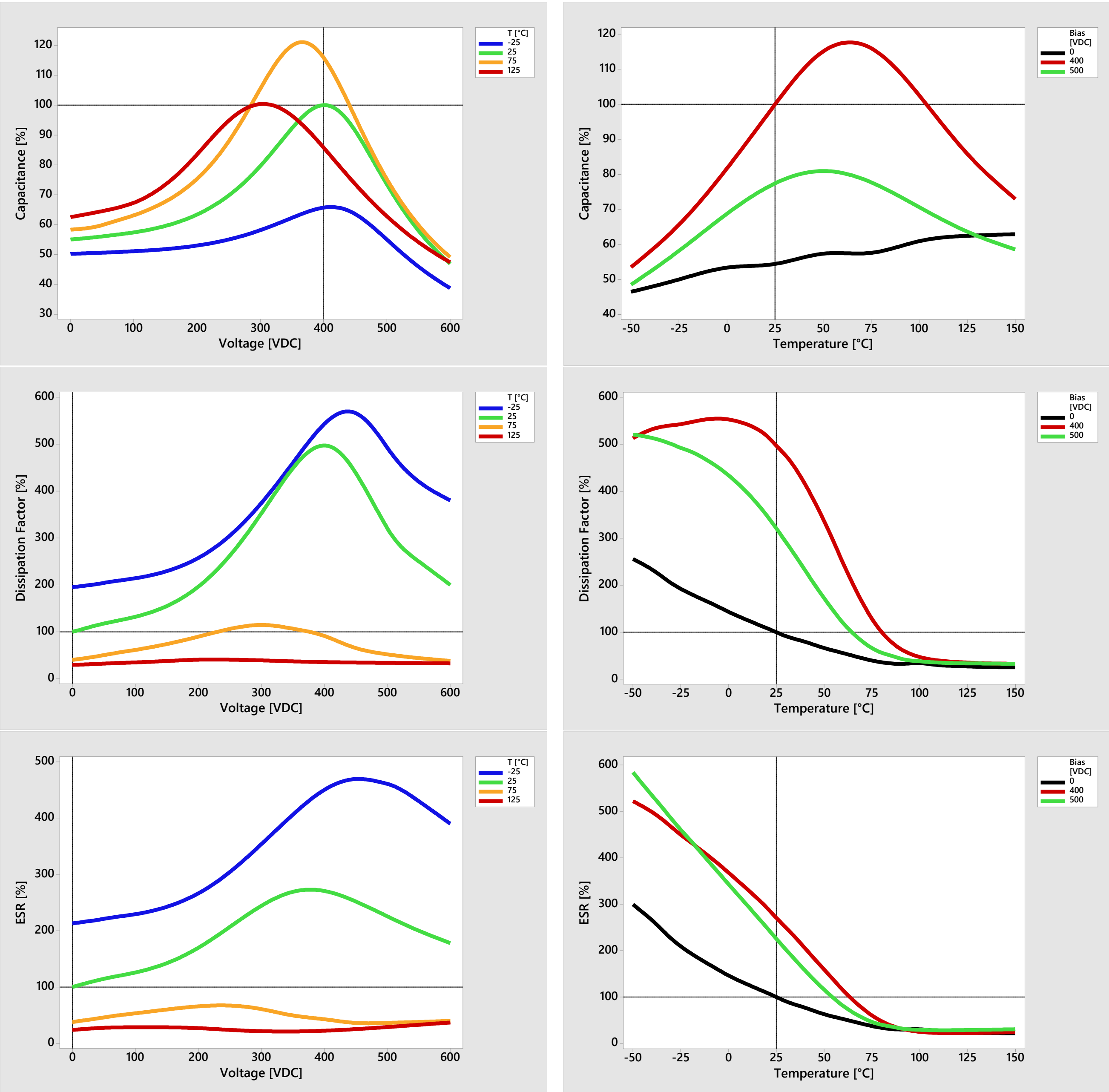
Further typical electrical characteristics as a design reference for CeraLink applications

Typical characteristics as a function of temperature and voltage V_R = 500 V

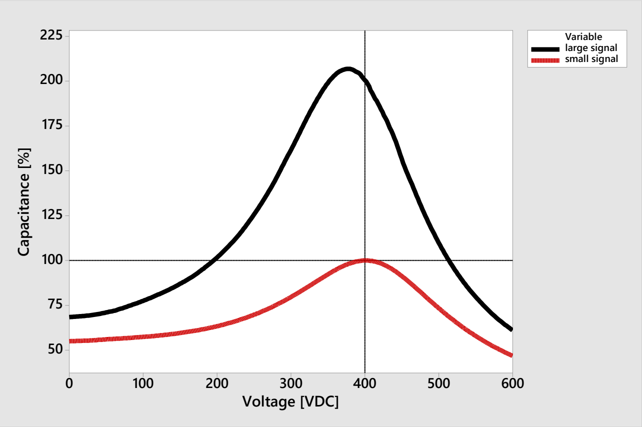
(0.5 V AC (RMS), frequency = 1 kHz)

All given temperatures are device temperatures.

The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100%-values correspond to tan δ, $C_{eff,typ}$ and ESR_{1kHz} which are given on page 2, 3 and 4 of this data sheet.



Typical capacitance values as a function of voltage V_R = 500 V



Large signal capacitance:

Quasistatic (slow variation of the voltage), +25 °C

The nominal capacitance is defined as the large signal capacitance at V_{op}.

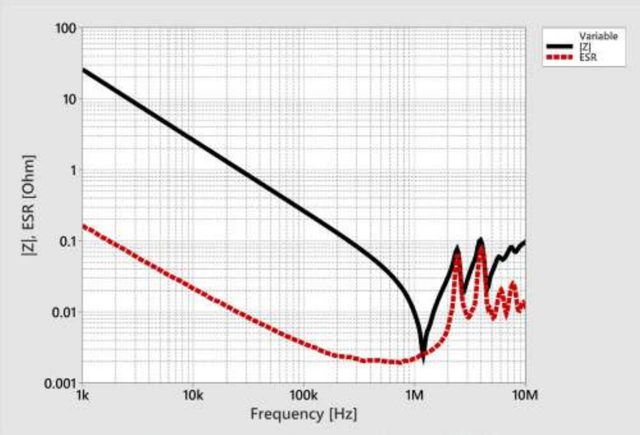
See glossary for further information.

Small signal capacitance:

0.5 V AC (RMS), 1 kHz, +25 °C

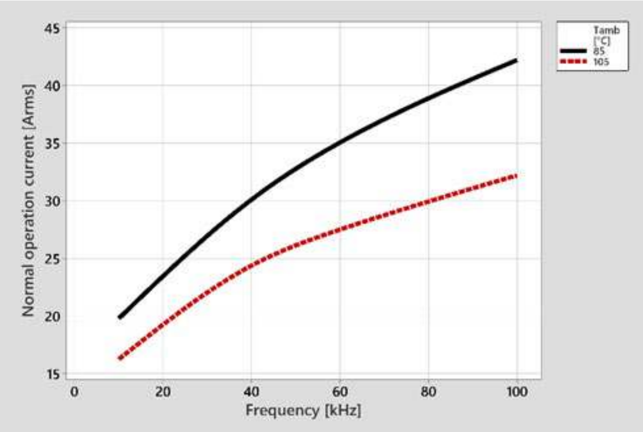
The effective capacitance is defined as the small signal capacitance at V_{op}.

Typical impedance and ESR as a function of frequency V_R = 500 V



0 V DC, 0.5 V AC (RMS), T_{device} = +25 °C

Typical permissible current as a function of frequency V_R = 500 V



Measurement performed at V_{op}.

The values correspond to a device temperature of +150 °C.

No active cooling was used.

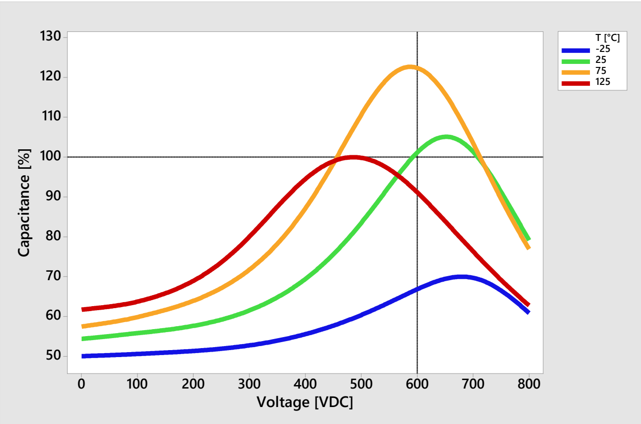
Note that with additional cooling the typical permissible current can be significantly higher.

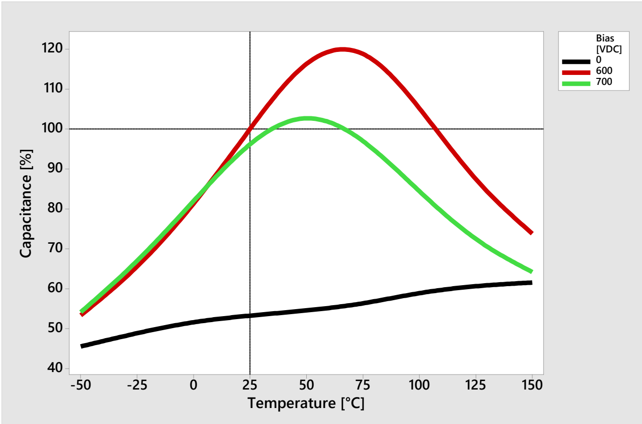
Typical characteristics as a function of temperature and voltage V_R = 700 V

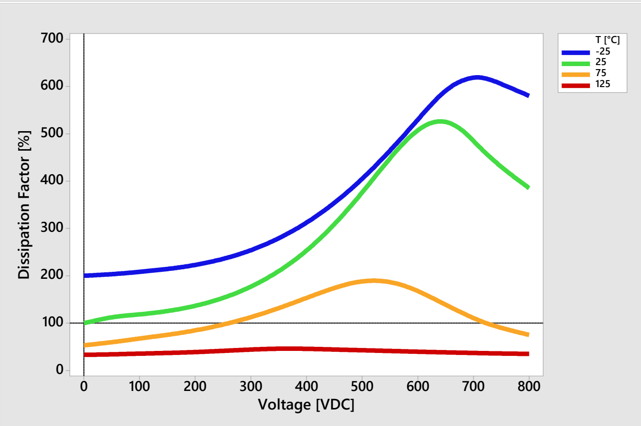
(0.5 V AC (RMS), frequency = 1 kHz)

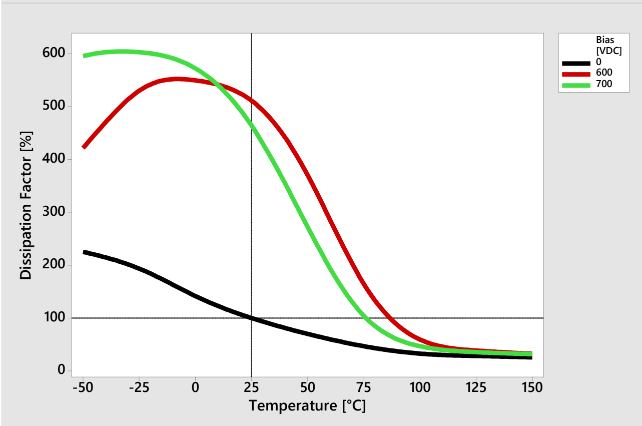
All given temperatures are device temperatures.

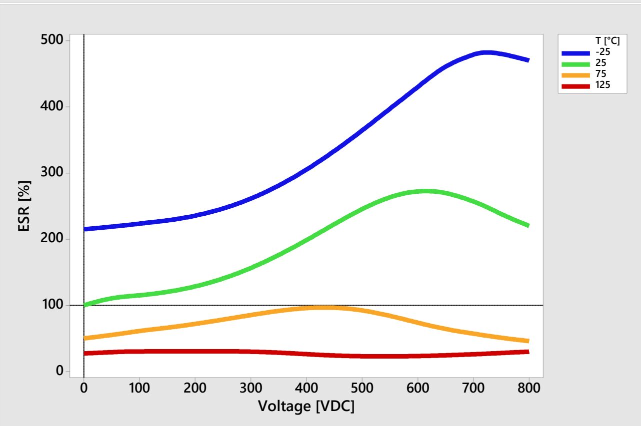
The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100%-values correspond to tan δ, $C_{eff,typ}$ and ESR_{1kHz} which are given on page 2, 3 and 4 of this data sheet.

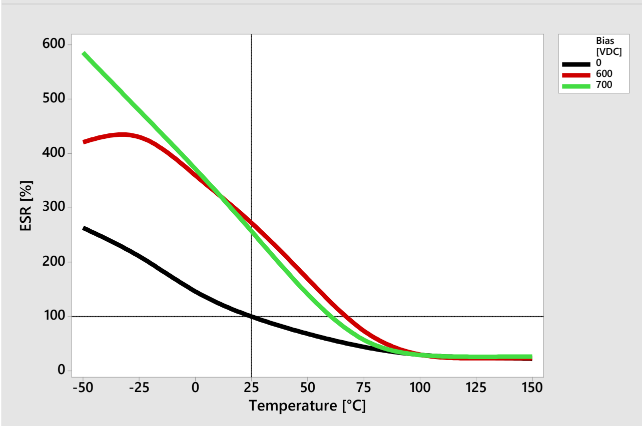




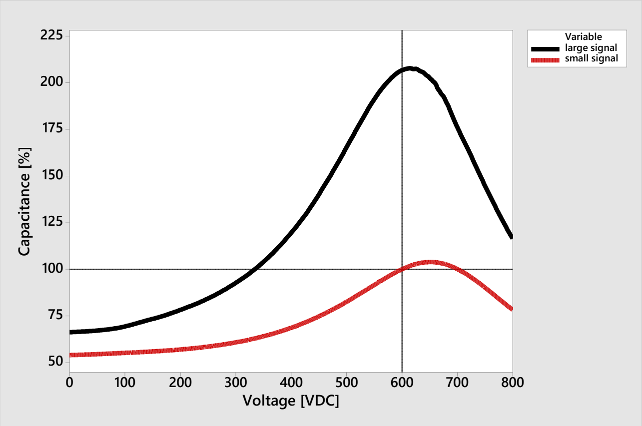








Typical capacitance values as a function of voltage V_R = 700 V



Large signal capacitance:

Quasistatic (slow variation of the voltage), +25 °C

The nominal capacitance is defined as the large signal capacitance at V_{op}.

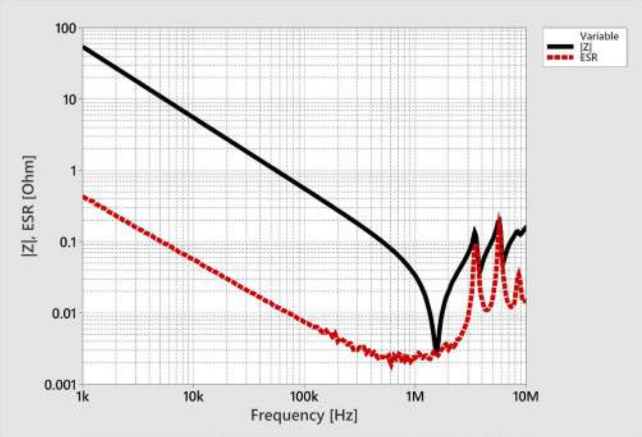
See glossary for further information.

Small signal capacitance:

0.5 V AC (RMS), 1 kHz, +25 °C

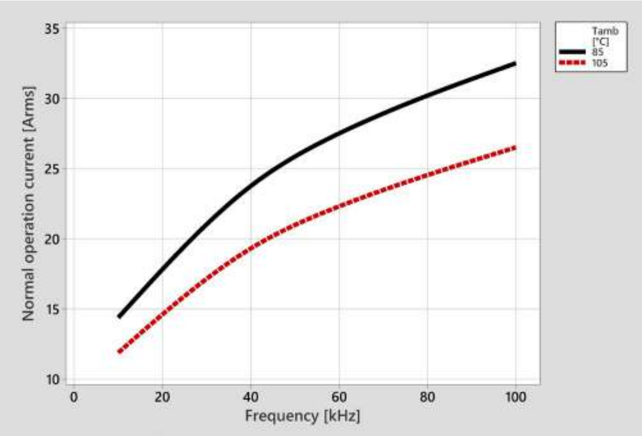
The effective capacitance is defined as the small signal capacitance at V_{op}.

Typical impedance and ESR as a function of frequency V_R = 700 V



0 V DC, 0.5 V AC (RMS), T_{device} = +25 °C

Typical permissible current as a function of frequency VR = 700 V



Measurement performed at V_{op}.

The values correspond to a device temperature of +150 °C.

No active cooling was used.

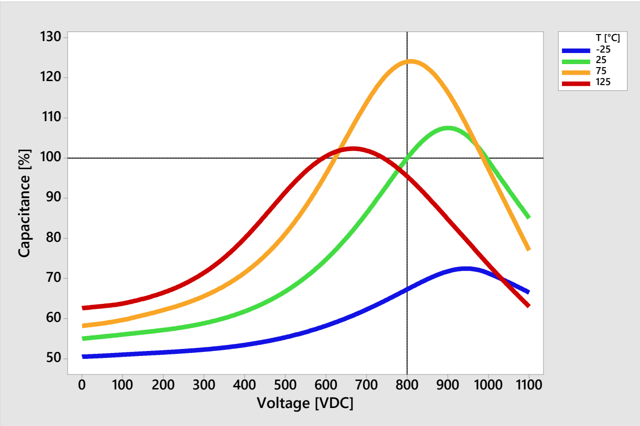
Note that with additional cooling the typical permissible current can be significantly higher.

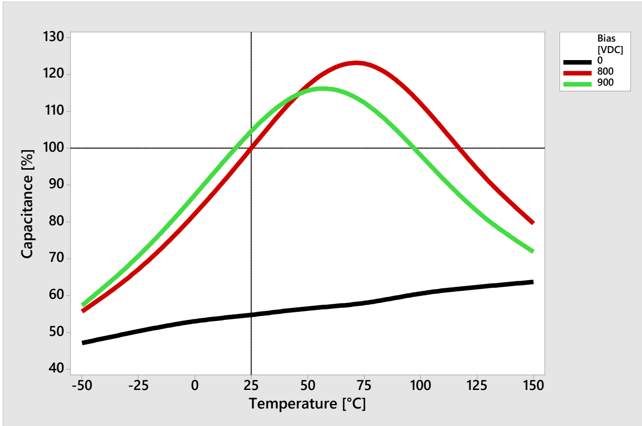
Typical characteristics as a function of temperature and voltage V_R = 900 V

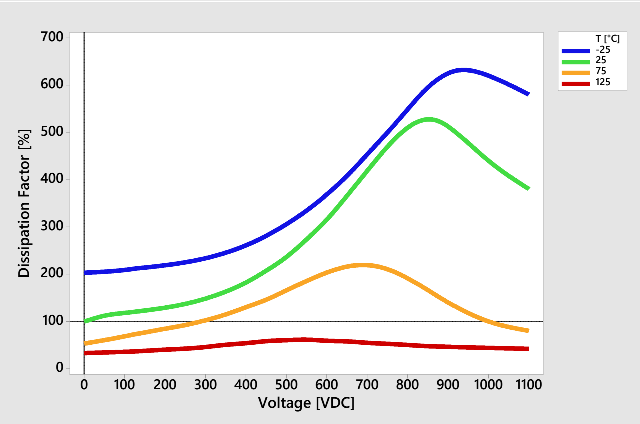
(0.5 V AC (RMS), frequency = 1 kHz)

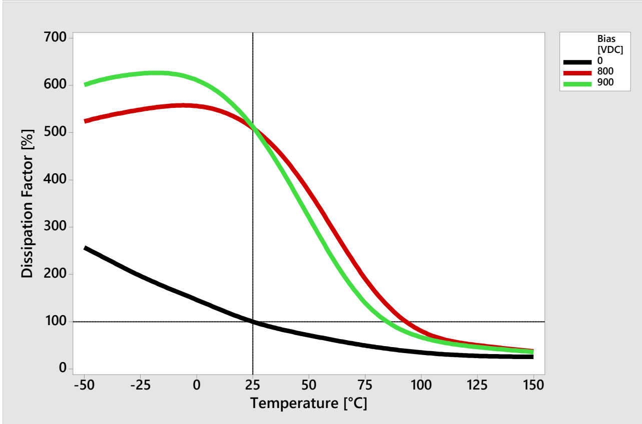
All given temperatures are device temperatures.

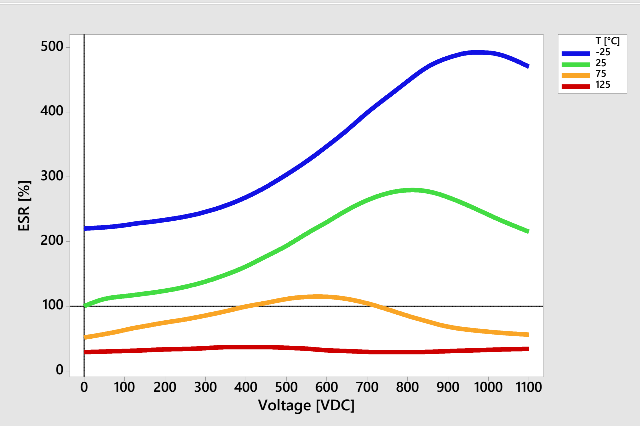
The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100%-values correspond to tan δ, $C_{eff,typ}$ and ESR_{1kHz} which are given on page 2, 3 and 4 of this data sheet.

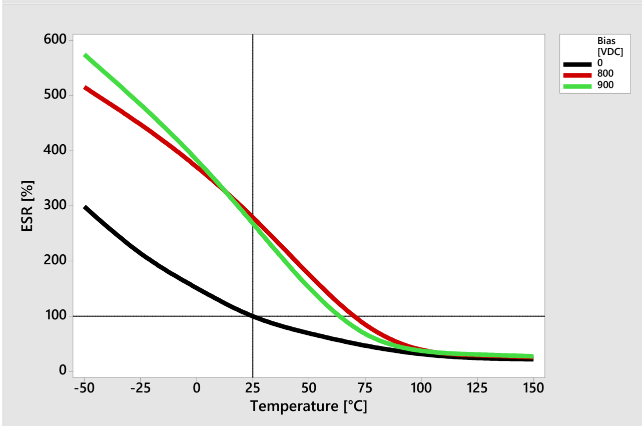




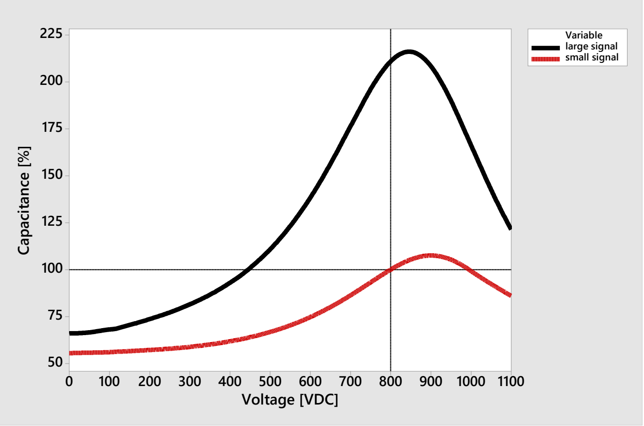








Typical capacitance values as a function of voltage V_R = 900 V



Large signal capacitance:

Quasistatic (slow variation of the voltage), +25 °C

The nominal capacitance is defined as the large signal capacitance at V_{op}.

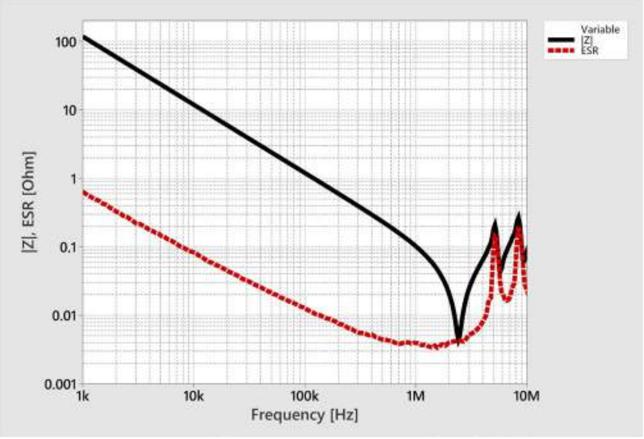
See glossary for further information.

Small signal capacitance:

0.5 V AC (RMS), 1 kHz, +25 °C

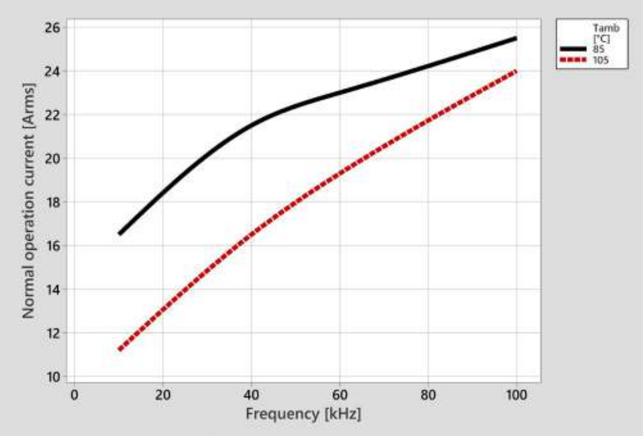
The effective capacitance is defined as the small signal capacitance at V_{op}.

Typical impedance and ESR as a function of frequency V_R = 900 V



0 V DC, 0.5 V AC (RMS), T_{device} = +25 °C

Typical permissible current as a function of frequency



Measurement performed at V_{op}.

The values correspond to a device temperature of +150 °C.

No forced cooling was used.

Note that with additional cooling the typical permissible current can be significantly higher.

Reliability

A. Preconditioning

- Solder the capacitor on a PCB using the recommended soldering profile
- Check of external appearance
- Measurement of isolation resistance R_{ins} *)
  - Apply $V_{pk,max}$ for 60 seconds and measure R_{ins} at room temperature:
    Isolation resistance (@ $V_{pk,max}$, 60 s, 25 °C) **R_{ins} > 100 MΩ**
- Measurement of electrical parameters C_0 and tanδ according to specification
  - Measure C_0 and tanδ within 10 minutes to 1 hour afterwards:
    Initial capacitance (@ 0 V DC, 0.5 V AC (RMS), 1 kHz, 25 °C) **C_0 acc. spec. on page 3**
    Dissipation factor (@ 0 V DC, 0.5 V AC (RMS), 1 kHz, 25 °C) **tanδ < 0.02**

B. Performance of a specific reliability test

C. After performing a specific test:

- Check the external appearance again
- Repeat the measurement of the electrical parameters
  - Apply $V_{pk,max}$ for 60 seconds and measure R_{ins} at room temperature:
    Isolation resistance (@$V_{pk,max}$, 60 s, 25 °C) **R_{ins} > 100 MΩ**
  - Measure C_0 and tan δ:
    Change of initial capacitance (@ 0 V DC, 0.5 V AC (RMS), 1 kHz, 25 °C) **|ΔC_0 / C_0| < 15%**
  - Dissipation factor (@ 0 V DC, 0.5 V AC (RMS), 1 kHz, 25 °C) **tan δ < 0.05**

*) Note that the measurement of the isolation resistance R_{ins} using the described measurement conditions is for pre- and post-measurement within the scope of the AEC-Q200 reliability tests only.

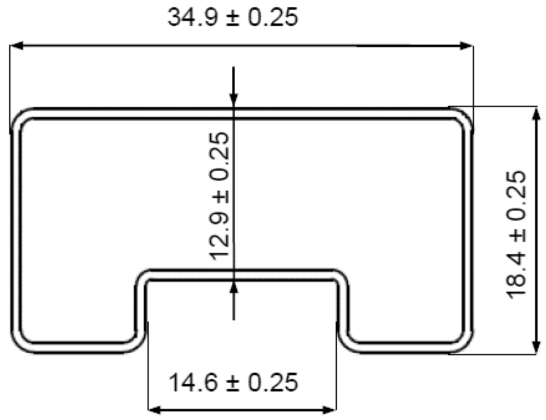
Qualification tests based on AEC-Q200 Rev. D (Table 2)

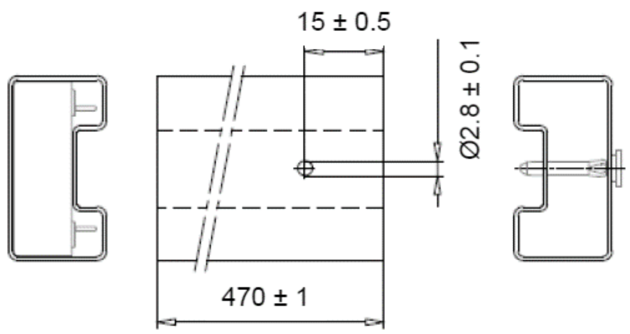
Test	No	Standard	Test conditions	Criteria
Pre- and post-stress electrical	1	-	As described above	|ΔC_0/C_0|, tanδ and R_{ins} within defined limits.
High temperature exposure	3	MIL-STD-202 Method 108	+150 °C, unpowered, 1000 hours	No mechanical damage |ΔC_0/C_0|, tan δ and R_{ins} within defined limits
Temperature cycling	4	JESD22 Method JA-104	-55 °C to +150 °C, 20 seconds transfer time, 15 minutes dwell time, 1000 cycles	No mechanical damage |ΔC_0/C_0|, tan δ and R_{ins} within defined limits
Destructive Physical analysis	5	EIA-469	-	No internal defects that might affect performance or reliability
Moisture resistance	6	MIL-STD-202 Method 106	+25 °C to +65 °C 90% rel. hum. to 100% rel. hum. 10 cycles, unpowered	No mechanical damage |ΔC_0/C_0|, tan δ and R_{ins} within defined limits
Biased humidity	7	MIL-STD-202 Method 103	+85 °C, 85% rel. hum., V_R, 1000 hours	No mechanical damage |ΔC_0/C_0|, tan δ and R_{ins} within defined limits

Test	No	Standard	Test conditions	Criteria
High temperature operating life	8	MIL-STD-202 Method 108	+150 °C, V_R, 1000 hours	No mechanical damage $\lvert\Delta C_0/C_0\rvert$, tan δ and R_{ins} within defined limits
External Visual	9	MIL-STD-883 Method 2009	Visual inspection with magnifying glass	No defects that might affect performance
Physical Dimension	10	JESD22 Method JB-100	Verify physical dimensions to the device specification using a caliper and a gauge	Within specified values in the chapter dimensional drawing
Resistance to solvent	12	MIL-STD-202 Method 215	Dipping and cleaning with isopropanol	Marking must be legible $\lvert\Delta C_0/C_0\rvert$, tan δ and R_{ins} within defined limits
Mechanical shock	13	MIL-STD-202 Method 213	Acceleration 400 m/s² Half sine pulse duration 6 milliseconds 4000 bumps	No mechanical damage $\lvert\Delta C_0/C_0\rvert$, tan δ and R_{ins} within defined limits
Vibration	14	MIL-STD-202 Method 204	5 g / 20 min, 12 cycles, 3 axes 10 Hz to 2000 Hz	No mechanical damage $\lvert\Delta C_0/C_0\rvert$, tan δ and R_{ins} within defined limits
Resistance to soldering heat	15	MIL-STD-202 Method 210 Condition B	Dip test of contact areas in solder bath (+260 °C for 10 seconds)	No damage of pin silver coating, $\lvert\Delta C_0/C_0\rvert$, tan δ and R_{ins} within defined limits
Solderability	18	J-STD-002 Method A	Dip test of contact areas in solder bath (+235 °C for 5 seconds)	Dipped surface is covered with solder coating

Packaging

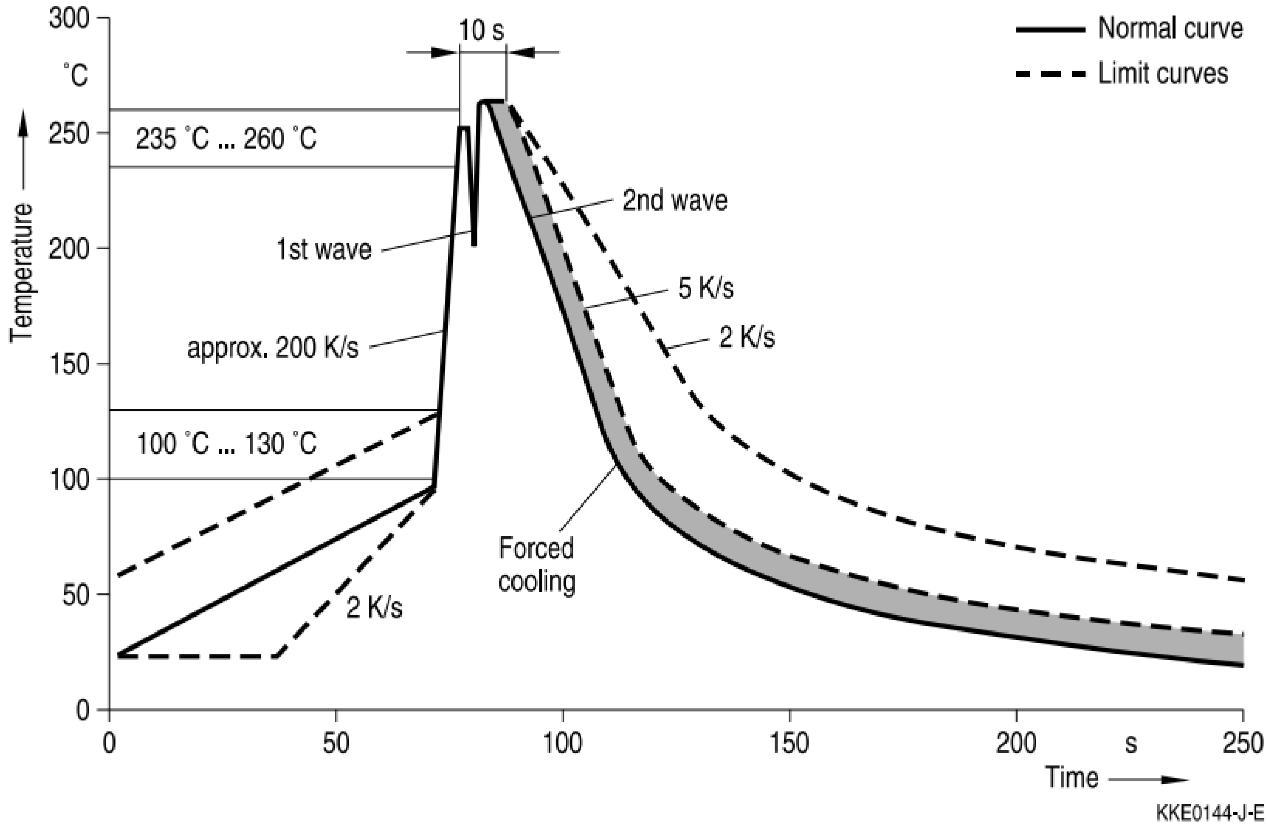
The CeraLink SP type will be delivered in a tube and will be packed in a cardboard box.
The packaging unit is 20 pieces per tube. The tube is terminated with one pin and two plugs.





Recommended wave-soldering profile

Temperature characteristic at component terminal with dual-wave soldering



Notes:

The use of mild, non-activated fluxes for soldering is recommended, as well as proper cleaning of the PCB.

After the soldering process, the capacitance is lowered. Applying V_R to the device will re-establish the capacitance.

General technical information

Storage

- Only store CeraLink capacitors in their original packaging. Do not open the package prior to processing.
- Storage conditions in original packaging: temperature −25 °C to +45 °C, relative humidity ≤ 75% annual average, maximum 95%, dew precipitation is inadmissible.
- Do not store CeraLink capacitors where they are exposed to heat or direct sunlight. Otherwise, the packaging material may be deformed or CeraLink may stick together, causing problems during mounting.
- Avoid contamination of the CeraLink surface during storage, handling, and processing.
- Avoid storing CeraLink devices in harmful environments where they are exposed to corrosive gases (e.g. SOx, Cl).
- Use CeraLink as soon as possible after opening factory seals, such as polyvinyl-sealed packages.
- Solder CeraLink components within 12 months after shipment.

Handling

- Do not drop CeraLink components or allow them to be chipped.
- Do not touch CeraLink with your bare hands - gloves are recommended.
- Avoid contamination of the CeraLink surface during handling.

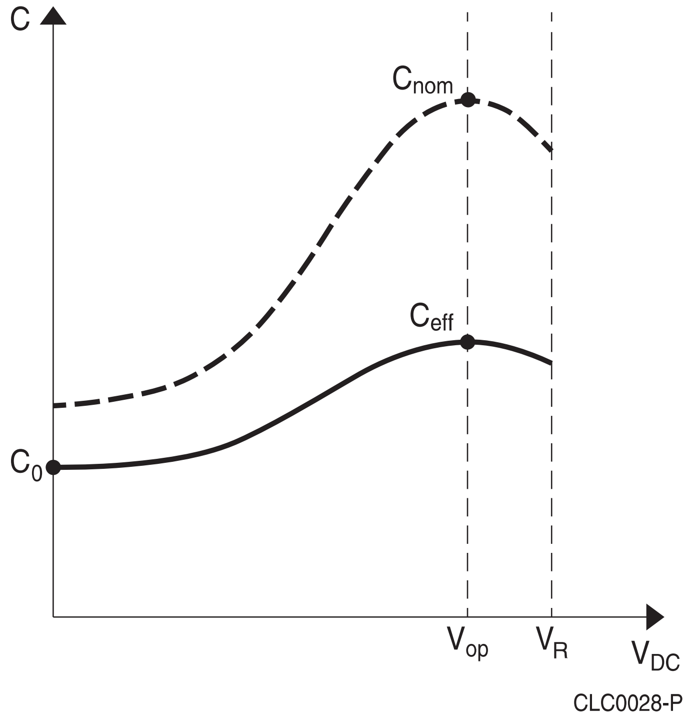
Mounting

- Do not scratch the external electrodes before, during or after the mounting process.
- Make sure contacts and housings used for assembly with CeraLink components are clean before mounting.
- The surface temperature of an operating CeraLink can be higher than the ambient temperature. Ensure that adjacent components are placed at a sufficient distance from a CeraLink to allow proper cooling.
- Avoid contamination of the CeraLink surface during processing.

Soldering guidelines

- The use of mild, non-activated fluxes for soldering is recommended, as well as proper cleaning of the PCB.
- Complete removal of flux is recommended to avoid surface contamination that can result in an instable and/or high leakage current.
- Use resin-type or non-activated flux.
- Bear in mind that insufficient preheating may cause ceramic cracks.
- Rapid cooling by dipping in solvent is not recommended, otherwise a component may crack.
- If an unsuitable cleaning fluid is used, flux residue or foreign particles may stick to the CeraLink surface and deteriorate its insulation resistance. Insufficient or improper cleaning of the CeraLink may cause damage to the component.

Glossary



Initial capacitance C_0:	Is the value at the origin of the hysteresis without any applied direct voltage.
Effective capacitance C_{eff}:	Occurs at V_{op} and is measured with an applied ripple voltage of 0.5 V AC (RMS) and 1 kHz. The CeraLink is designed to have its highest capacitance value at the operating voltage V_{op}.
Nominal capacitance C_{nom}:	Is the value derived by the tangent of the mean hysteresis (as the derivative of the mean hysteresis is dQ/dV ~ C).

See our *CeraLink Technical Guide* for further details.

Symbols and terms

AC	Alternating current
C_0	Initial capacitance @ 0 V DC, 0.5 V AC (RMS), 1 kHz, +25 °C
$C_{eff,typ}$	Typical effective capacitance @ V_{op}, 0.5 V AC (RMS), 1 kHz, +25 °C
$C_{nom,typ}$	Typical nominal capacitance @ V_{op}, quasistatic, +25 °C. See glossary for definition of the nominal capacitance
DC	Direct current
ESL	Equivalent serial inductance
ESR	Equivalent serial resistance
I_{op}	Operating ripple current, root mean square value of sinusoidal AC current
SP	Solder pin
PCB	Printed circuit board
PLZT	Lead lanthanum zirconium titanate
R_{ins}	Insulation resistance @ $V_{pk,max}$, measurement time t = 60 s, +25 °C. For pre- and post-measurements within the scope of the AEC-Q200 reliability tests.
$R_{ins,typ}$	Insulation resistance @ V_{op}, measurement time t ≥ 240 s, +25 °C
T_{amb}	Ambient temperature
tan δ	Dissipation factor @ 0 V DC, 0.5 V AC (RMS),1 kHz, +25°C
T_{device}	Device temperature. $T_{device} = T_{amb} + \Delta T$ (ΔT defines the self-heating of the device due to applied current).
V_{op}	Operating voltage at maximum attenuation capability
V_R	Rated voltage. Reference DC voltage for reliability tests.
$V_{AC,RMS}$	Root mean square value of sinusoidal AC voltage
$V_{pk,max}$	Maximum peak operating voltage (e.g. voltage overshoots or surge pulses which occur < 5% of total component lifecycle). Not recommended for continuous operation.
ΔT	Increase of temperature during operation

Cautions and warnings

General

- Not for use in resonant circuits, where a voltage of alternating polarity occurs.
- Not for AC applications. Consult our local representative for further details.
- If used in snubber circuits, ensure that the sum of all voltages remains at the same polarity.
- Do not use CeraLink components for purposes not identified in our specifications, application notes, and data books.
- Ensure the suitability of a CeraLink in particular by testing it for reliability during design-in. Always evaluate a CeraLink component under worst-case conditions.
- Pay special attention to the reliability of CeraLink devices intended for use in safety-critical applications (e.g. medical equipment, automotive, spacecraft, nuclear power plant).
- Depending on the individual application, CeraLink components are electrically connected to voltages and currents, which are potentially dangerous for life and health of the operator. Installation and operation of CeraLink must be done only by authorized personnel. Ensure proper and safe connections, couplers, and drivers.
- Caution: CeraLink components are highly efficient charge storing devices. Even when disconnected from a supply, the electrical energy content of a loaded component can be high and is held for a long time. Always ensure a complete discharging of the component (e.g. via a 10 kΩ resistor) before handling. Do not discharge by simple short-circuiting, because of the risk of damaging the ceramic.
- Electrical charges can be generated on disconnected components by varying load or temperature. Caution: Discharge a CeraLink before connecting it to a measuring component/electronics, when this component is not sufficiently voltage proved.

  See *Important notes* section for further details.

Design notes

- Consider derating at higher operating temperatures. As a rule, lower temperatures and voltages increase the lifetime of CeraLink devices.
- If steep surge current edges are to be expected, make sure your design is as low-inductive as possible.
- In some cases, the malfunctioning of passive electronic components or failure before the end of their service life cannot be completely ruled out in the current state of the art, even if they are operated as specified. In applications requiring a very high level of operational safety and especially when the malfunction or failure of a passive electronic component could endanger human life or health (e.g. in accident prevention, life-saving systems, or automotive battery line applications such as clamp 30), ensure by suitable design of the application or other measures (e.g. installation of protective circuitry, fuse or redundancy) that no injury or damage is sustained by third parties in the event of such a malfunction or failure.
- Specified values only apply to CeraLink components that have not been subject to prior electrical, mechanical, or thermal damage. The use of CeraLink devices in line-to-ground applications is therefore not advisable, and it is only allowed together with safety countermeasures such as thermal fuses.

Operation

- Use CeraLink only within the specified operating temperature range.
- Use CeraLink only within specified voltage and current ranges.
- The CeraLink has to be operated in a dry atmosphere, which must not contain any additional chemical vapors or substances.
- Environmental conditions must not harm the CeraLink. Use the capacitors under normal atmospheric conditions only. A reduction of the oxygen partial pressure to below 1 mbar is not permissible.
- Prevent a CeraLink from contacting liquids and solvents.
- Avoid dewing and condensation.
- During operation, the CeraLink can produce audible noise due to its piezoelectric characteristic.
- CeraLink components are mainly designed for encased applications. Under all circumstances avoid exposure to:
  - direct sunlight
  - rain or condensation
  - steam, saline spray
  - corrosive gases
  - atmosphere with reduced oxygen content.

This listing does not claim to be complete, but merely reflects the experience of the manufacturer.

Display of ordering codes for TDK Electronics products

The ordering code for one and the same product can be represented differently in data sheets, data books, other publications, on the company website, or in order-related documents such as shipping notes, order confirmations and product labels. **The varying representations of the ordering codes are due to different processes employed and do not affect the specifications of the respective products**. Detailed information can be found on the Internet at http://www.tdk-electronics.tdk.com/orderingcodes.

Important notes

The following applies to all products named in this publication:

1. Some parts of this publication contain **statements about the suitability of our products for certain areas of application**. These statements are based on our knowledge of typical requirements that are often placed on our products in the areas of application concerned. We nevertheless expressly point out **that such statements cannot be regarded as binding statements about the suitability of our products for a particular customer application.** As a rule we are either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always ultimately incumbent on the customer to check and decide whether a product with the properties described in the product specification is suitable for use in a particular customer application.
2. We also point out that **in individual cases, a malfunction of electronic components or failure before the end of their usual service life cannot be completely ruled out in the current state of the art, even if they are operated as specified.** In customer applications requiring a very high level of operational safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health (e.g. in accident prevention or life-saving systems), it must therefore be ensured by means of suitable design of the customer application or other action taken by the customer (e.g. installation of protective circuitry or redundancy) that no injury or damage is sustained by third parties in the event of malfunction or failure of an electronic component.
3. **The warnings, cautions and product-specific notes must be observed.**
4. In order to satisfy certain technical requirements, **some of the products described in this publication may contain substances subject to restrictions in certain jurisdictions (e.g. because they are classed as hazardous)**. Useful information on this will be found in our Material Data Sheets on the Internet (www.tdk-electronics.tdk.com/material). Should you have any more detailed questions, please contact our sales offices.
5. We constantly strive to improve our products. Consequently, **the products described in this publication may change from time to time**. The same is true of the corresponding product specifications. Please check therefore to what extent product descriptions and specifications contained in this publication are still applicable before or when you place an order.

   We also **reserve the right to discontinue production and delivery of products**. Consequently, we cannot guarantee that all products named in this publication will always be available. The aforementioned does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.
6. Unless otherwise agreed in individual contracts, **all orders are subject to our General Terms and Conditions of Supply.**
7. **Our manufacturing sites serving the automotive business apply the IATF 16949 standard.** The IATF certifications confirm our compliance with requirements regarding the quality management system in the automotive industry. Referring to customer requirements and customer specific requirements (“CSR”) TDK always has and will continue to have the policy of respecting individual agreements. Even if IATF 16949 may appear to support the acceptance of unilateral requirements, we hereby like to emphasize that **only requirements mutually agreed upon can and will be implemented in our Quality Management System.** For clarification purposes we like to point out that obligations from IATF 16949 shall only become legally binding if individually agreed upon.

Important notes

8. The trade names EPCOS, CarXield, CeraCharge, CeraDiode, CeraLink, CeraPad, CeraPlas, CSMP, CTVS, DeltaCap, DigiSiMic, FilterCap, FormFit, InsuGate, LeaXield, MediPlas, MiniBlue, MiniCell, MKD, MKK, ModCap, MotorCap, PCC, PhaseCap, PhaseCube, PhaseMod, PhiCap, PiezoBrush, PlasmaBrush, PowerHap, PQSine, PQvar, SIFERRIT, SIFI, SIKOREL, SilverCap, SIMDAD, SiMic, SIMID, SineFormer, SIOV, ThermoFuse, WindCap, XieldCap are **trademarks registered or pending** in Europe and in other countries. Further information will be found on the Internet at www.tdk-electronics.tdk.com/trademarks.

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