

PSMN7R0-100ES

N-channel 100V 6.8 $\mbox{m}\Omega$ standard level MOSFET in I2PAK.

Rev. 03 — 23 February 2010

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in I2PAK package qualified to 175C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive

1.3 Applications

- DC-to-DC converters
- Load switching

- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$		-	-	100	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u>	[1]	-	-	100	Α
P _{tot}	total power dissipation	$T_{mb} = 25 ^{\circ}C; \text{ see } \frac{\text{Figure 2}}{}$		-	-	269	W
T_j	junction temperature			-55	-	175	°C
Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; V_{sup} ≤ 100 V; unclamped; R_{GS} = 50 Ω		-	-	315	mJ
Dynamic	characteristics						
Q_{GD}	gate-drain charge	V_{GS} = 10 V; I_D = 25 A; V_{DS} = 50 V; see <u>Figure 15</u> and <u>14</u>		-	36	-	nC
Q _{G(tot)}	total gate charge	V_{GS} = 10 V; I_D = 25 A; V_{DS} = 50 V; see <u>Figure 14</u> and <u>15</u>		-	125	-	nC



Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static ch	aracteristics					
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A};$ $T_j = 100 \text{ °C}; \text{ see } \frac{\text{Figure } 12}{}$	-	-	12	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure } 13}{}$	-	5.4	6.8	mΩ

^[1] Continuous current is limited by package

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain	mb	D D
3	S	source		
mb	D	mounting base; connected to drain	1 2 3	mbb076 S
			SOT226 (I2PAK)	

3. Ordering information

Table 3. Ordering information

Type number	Package			
	Name	Description	Version	
PSMN7R0-100ES	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226	

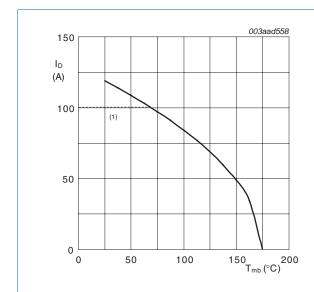
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

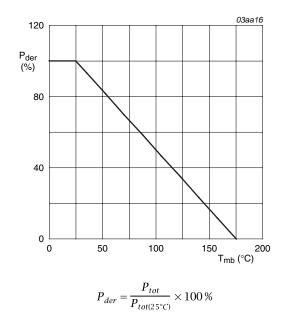
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	100	V
V_{DGR}	drain-gate voltage	$T_j \le 175 \text{ °C}; T_j \ge 25 \text{ °C}; R_{GS} = 20 \text{ k}\Omega$		-	100	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 100 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{\text{Model}}$		-	85	Α
		$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{}$	<u>[1]</u>	-	100	Α
I _{DM}	peak drain current	$t_p \le 10$ μs; pulsed; $T_{mb} = 25$ °C; see Figure 3		-	475	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	269	W
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
	ain diode					
Is	source current	T _{mb} = 25 °C;	<u>[1]</u>	-	100	Α
I _{SM}	peak source current	$t_p \le 10 \ \mu s$; pulsed; $T_{mb} = 25 \ ^{\circ}C$		-	475	Α
Avalanch	e ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; V_{sup} ≤ 100 V; unclamped; R_{GS} = 50 Ω		-	315	mJ

[1] Continuous current is limited by package

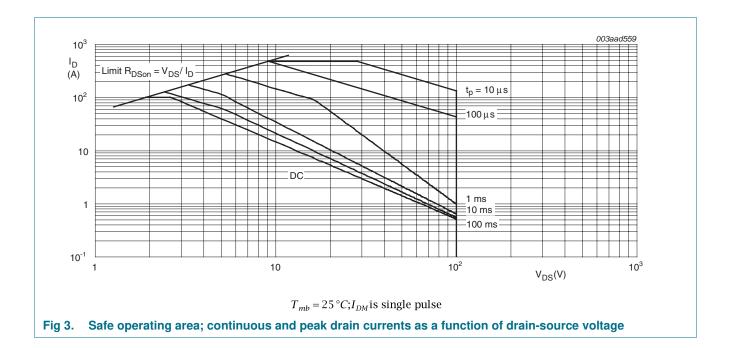


 $V_{GS} \ge 10$ V; (1) capped at 100 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



g 2. Normalized total power dissipation as a function of mounting base temperature



5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.3	0.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air	-	60	-	K/W

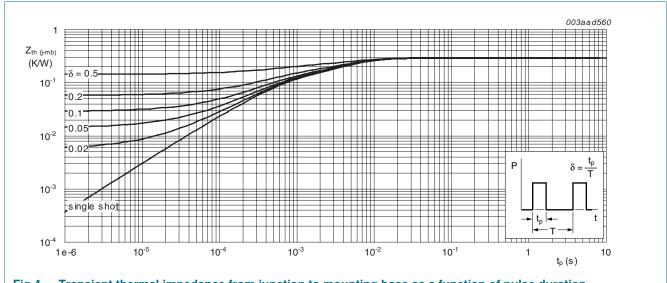


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
V _{(BR)DSS}	drain-source	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ °C}$	90	-	-	V
	breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	100	-	-	V
V _{GS(th)}	gate-source threshold	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 175 \text{ °C}$; see Figure 10	1	-	-	V
\	voltage	I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 25 °C; see <u>Figure 11</u> and <u>10</u>	2	3	4	V
		$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = -55 \text{ °C}$; see Figure 10	-	-	4.8	٧
I _{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ °C}$	-	-	150	μΑ
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.08	4	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	10	100	nΑ
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nA
R _{DSon}	drain-source on-state	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 100 ^{\circ}\text{C}; \text{see } \frac{\text{Figure } 12}{}$	-	-	12	mΩ
resis	resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 175 \text{ °C}; \text{see } \frac{\text{Figure } 12}{}$	-	15	19	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C}; \text{see } \frac{\text{Figure } 13}{\text{ Figure } 13}$	-	5.4	6.8	mΩ
R_G	internal gate resistance (AC)	f = 1 MHz	-	0.74	-	Ω
Dynamic o	characteristics					
$Q_{G(tot)}$ total gate charge	total gate charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; see <u>Figure 14</u> and <u>15</u>	-	125	-	nC
		$I_D = 0 A$; $V_{DS} = 0 V$; $V_{GS} = 10 V$	-	100	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; see <u>Figure 15</u> and <u>14</u>	-	28	-	nC
Q _{GS(th)}	pre-threshold gate-source charge	$I_D = 25 \text{ A}$; $V_{DS} = 50 \text{ V}$; $V_{GS} = 10 \text{ V}$; see <u>Figure 15</u>	-	19.4	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	9	-	nC
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; see <u>Figure 15</u> and <u>14</u>	-	36	-	nC
V _{GS(pl)}	gate-source plateau voltage	$V_{DS} = 50 \text{ V}$; see <u>Figure 15</u> and <u>14</u>	-	4.3	-	V
C _{iss}	input capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_i = 25 °C;$	-	6686	-	pF
C _{oss}	output capacitance	see Figure 16	-	438	-	pF
C _{rss}	reverse transfer capacitance		-	272	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 2 \Omega; V_{GS} = 10 \text{ V};$	-	34.6	-	ns
t _r	rise time	$R_{G(ext)} = 4.7 \Omega; T_j = 25 \degree C$	-	45.6	-	ns
t _{d(off)}	turn-off delay time		_	103.9	-	ns
t _f	fall time		_	49.5	_	ns

Table 6. Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-dr	ain diode					
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ °C}$; see <u>Figure 17</u>	-	8.0	1.2	V
t _{rr}	reverse recovery time	$I_S = 25 \text{ A}$; $dI_S/dt = 100 \text{ A/}\mu\text{s}$; $V_{GS} = 0 \text{ V}$;	-	64	-	ns
Q _r	recovered charge	$V_{DS} = 50 \text{ V}$	-	167	-	nC

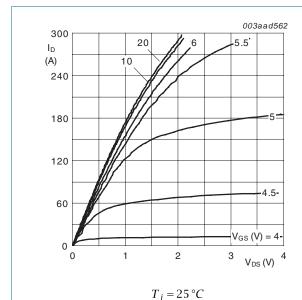


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

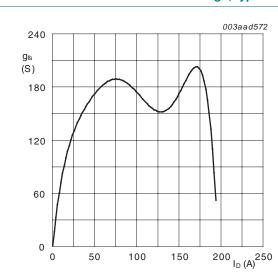


Fig 7. Forward transconductance as a function of drain current; typical values

 $T_j = 25 \,^{\circ}C; V_{DS} = 15 V$

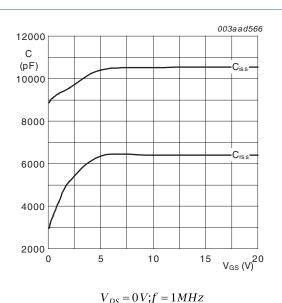


Fig 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

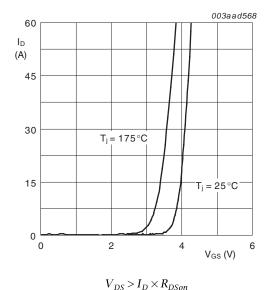


Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

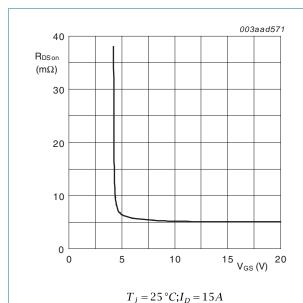


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

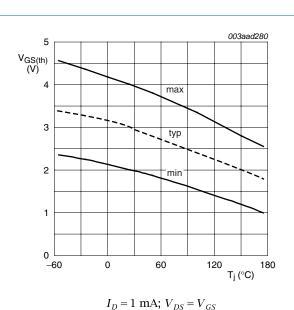
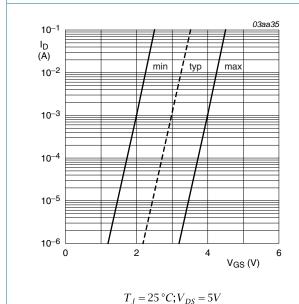


Fig 10. Gate-source threshold voltage as a function of junction temperature



gate-source voltage

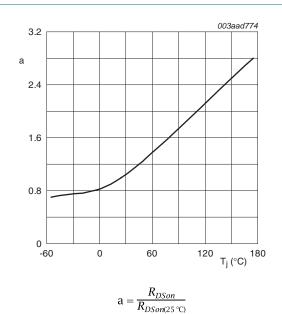


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



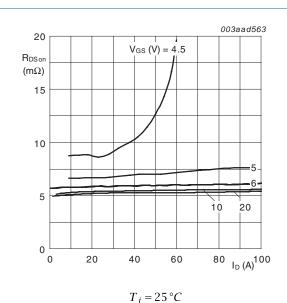


Fig 13. Drain-source on-state resistance as a function of drain current; typical values

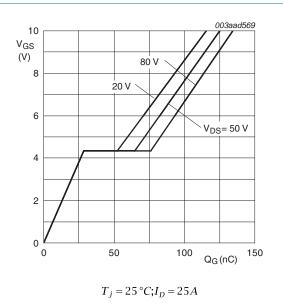


Fig 14. Gate-source voltage as a function of gate charge; typical values

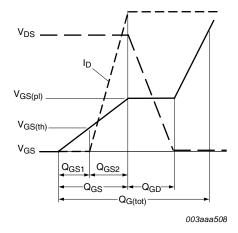
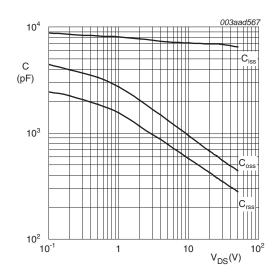
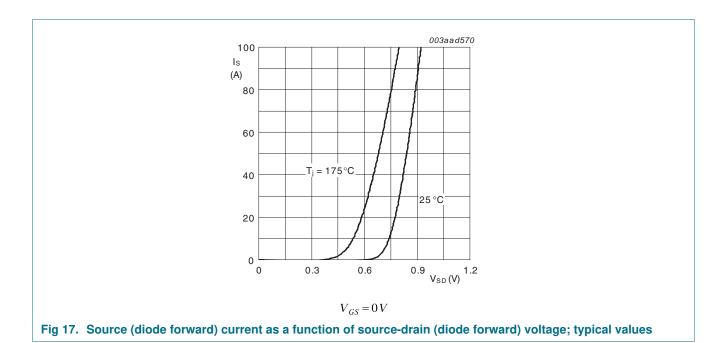


Fig 15. Gate charge waveform definitions



 $V_{GS} = 0V; f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



7. Package outline

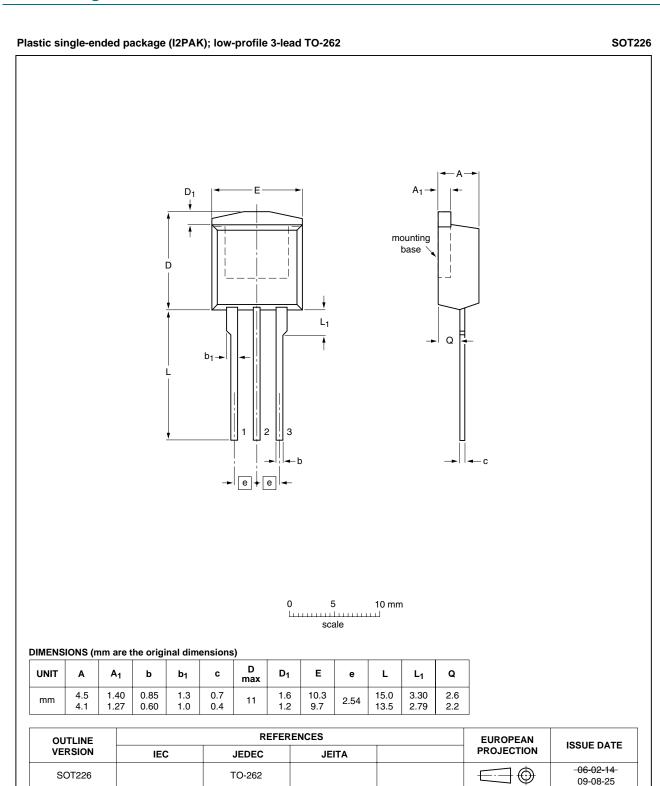


Fig 18. Package outline SOT226 (I2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN7R0-100ES_3	20100223	Product data sheet	-	PSMN7R0-100ES_2
Modifications:	 Various cha 	anges to content.		
PSMN7R0-100ES_2	20100114	Objective data sheet	-	PSMN7R0-100ES_1
PSMN7R0-100ES_1	20090917	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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PSMN7R0-100ES_3

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PSMN7R0-100ES

Nexperia

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