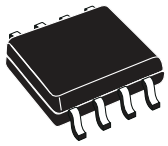
STS3DNE60L

DUAL N-CHANNEL 60V - 0.065Ω - 3A SO-8
STripFET™ POWER MOSFET

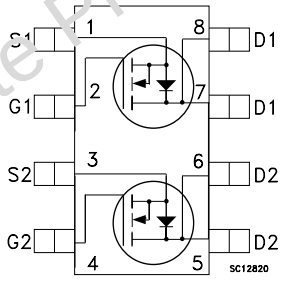
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STS3DNE60L	60 V	< 0.08 Ω	3 A

- TYPICAL $R_{DS}(on)$ = 0.065Ω
- LOW THRESHOLD GATE DRIVE
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY



SO-8

INTERNAL SCHEMATIC DIAGRAM



DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC MOTOR DRIVE
- DC-DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN PORTABLE/ DESKTOP PCS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	60	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	60	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuous) at T_C = 25°C Single Operation Drain Current (continuous) at T_C = 100°C Single Operation	3 1.9	A A
I_{DM} (•)	Drain Current (pulsed)	12	A
P_{TOT}	Total Dissipation at T_C = 25°C Dual Operation Total Dissipation at T_C = 25°C Single Operation	1.6 2.0	W W

(•)Pulse width limited by safe operating area

THERMAL DATA

Rthj-amb	(*)Thermal Resistance Junction-amb Max Single Operation (*)Thermal Resistance Junction-amb Max Dual Operation	62.5 78	°C/W °C/W
T_j	Max. Operating Junction Temperature	150	°C
T_{stg}	Storage Temperature	– 55 to 150	°C

(*) Mounted on FR-4 Board ($t \leq 10$ sec)

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	60			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V, I_D = 1.5 A V_{GS} = 4.5 V, I_D = 1.5 A		0.065 0.08	0.08 0.1	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15V , I_D = 1.5 A		5		S
C_{iss}	Input Capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		815		pF
C_{oss}	Output Capacitance			125		pF
C_{rss}	Reverse Transfer Capacitance			40		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 30 V, I_D = 3 A R_G = 4.7Ω V_{GS} = 5 V (see test circuit, Figure 3)		20 30		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 24 V, I_D = 3 A, V_{GS} = 4.5 V		13.5 6 3.5		nC nC nC

SWITCHING OFF

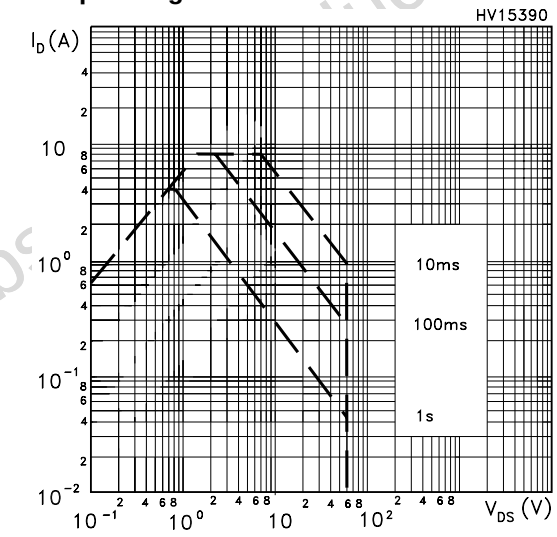
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(off)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 48 V, I_D = 3 A R_G = 4.7Ω, V_{GS} = 5 V (see test circuit, Figure 5)		12 16 32		ns ns ns

SOURCE DRAIN DIODE

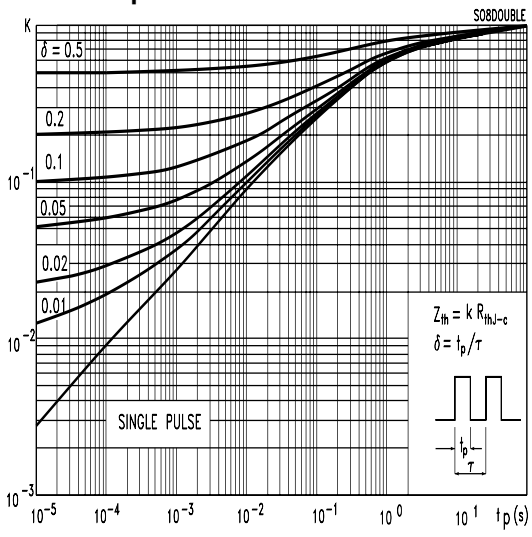
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain Current Source-drain Current (pulsed)				3 12	A A
V_{SD} (2)	Forward On Voltage	I_{SD} = 3 A, V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 3 A, di/dt = 100 A/µs, V_{DD} = 30 V, T_j = 150°C (see test circuit, Figure 5)		60 130 4		ns nC A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

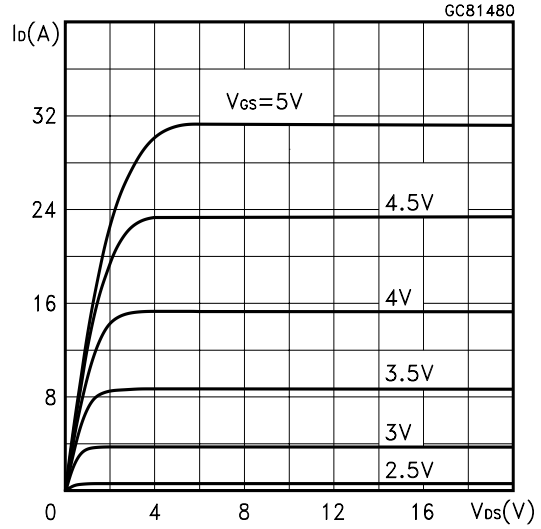
Safe Operating Area



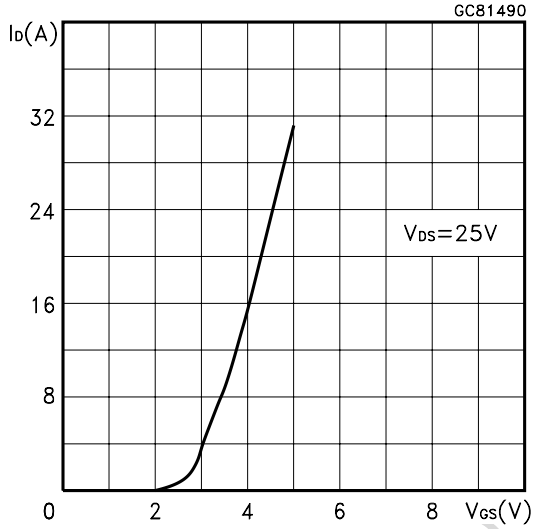
Thermal Impedance



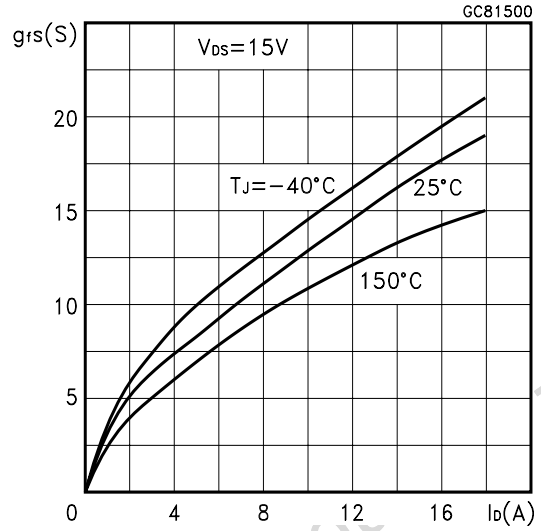
Output Characteristics



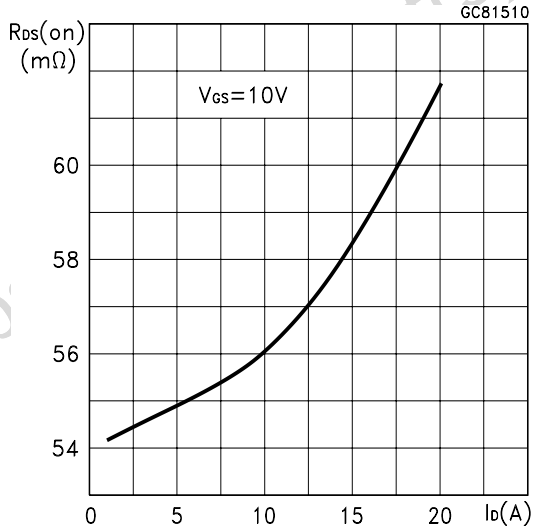
Transfer Characteristics



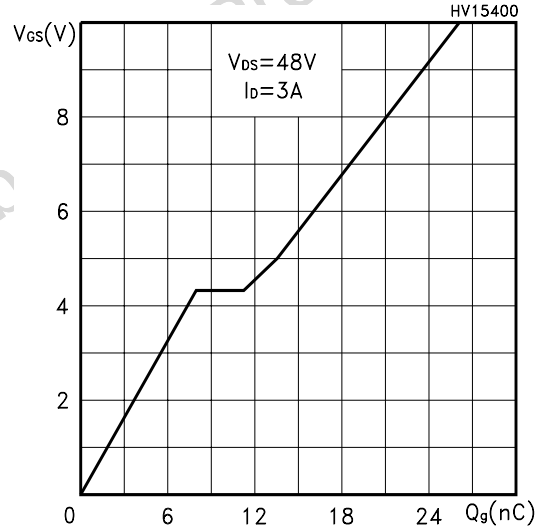
Tranconductance



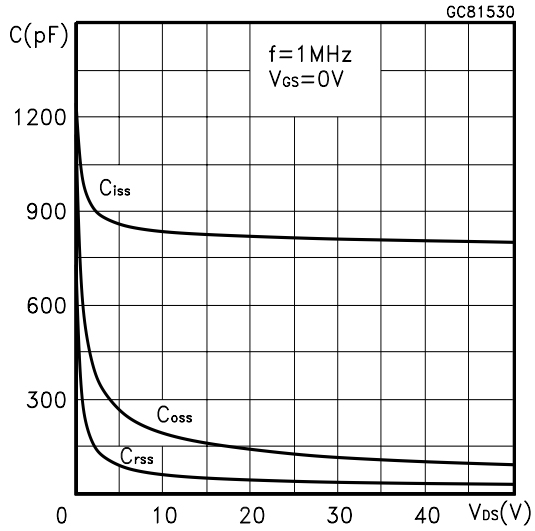
Static Drain-Source On Resistance



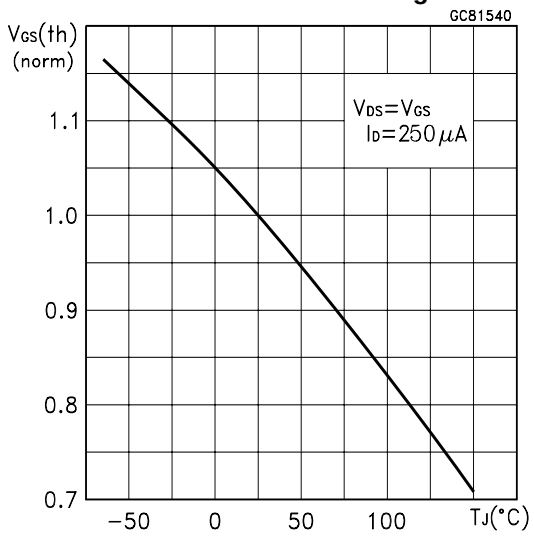
Gate Charge vs Gate-source Voltage



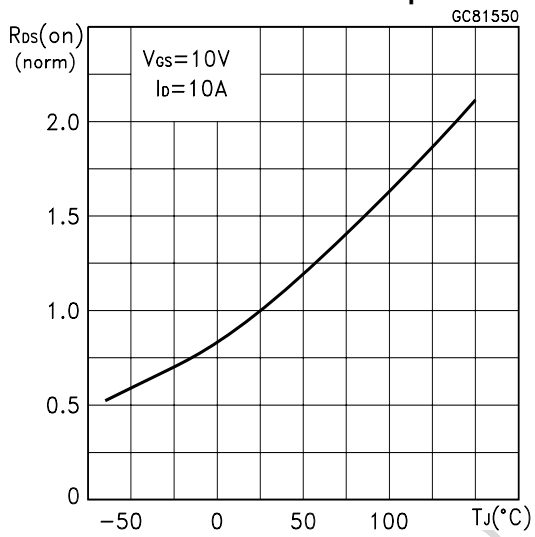
Capacitance Variations



Normalized Gate Thereshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

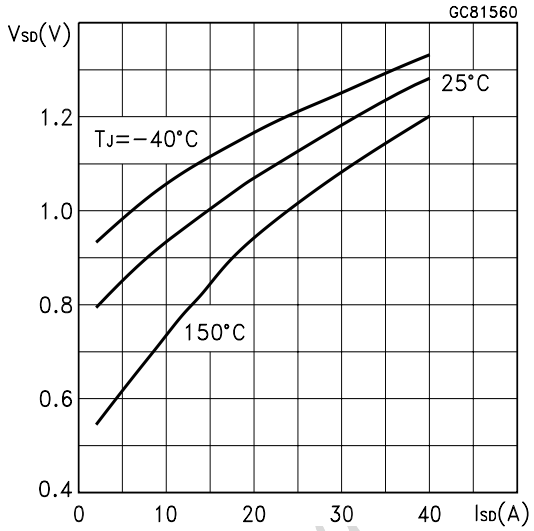


Fig. 1: Unclamped Inductive Load Test Circuit

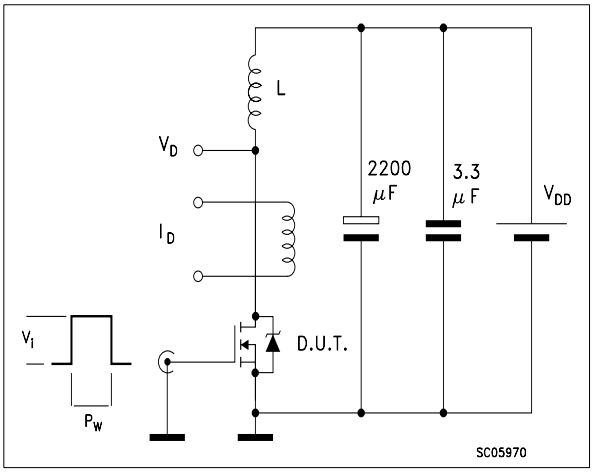


Fig. 2: Unclamped Inductive Waveform

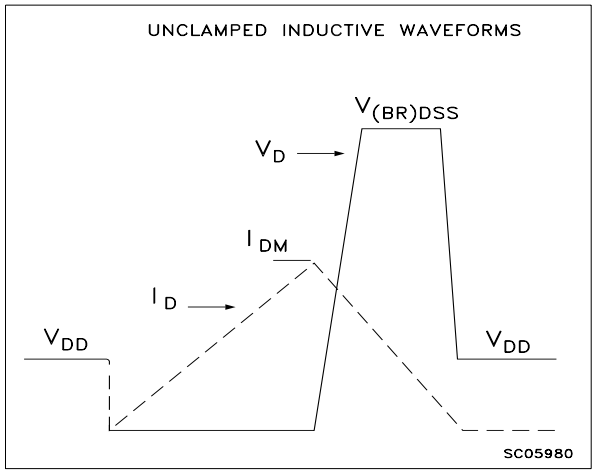


Fig. 3: Switching Times Test Circuit For Resistive Load

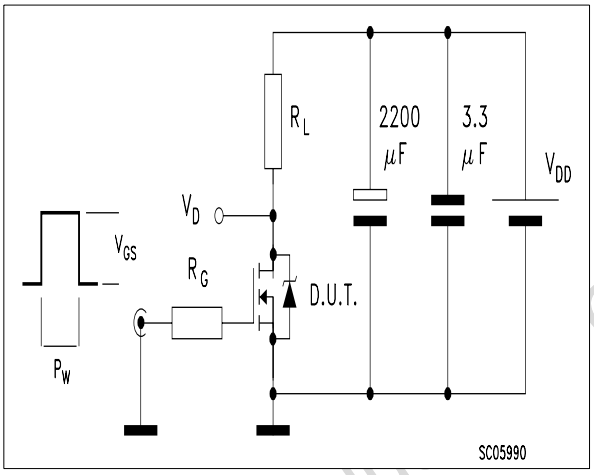


Fig. 4: Gate Charge test Circuit

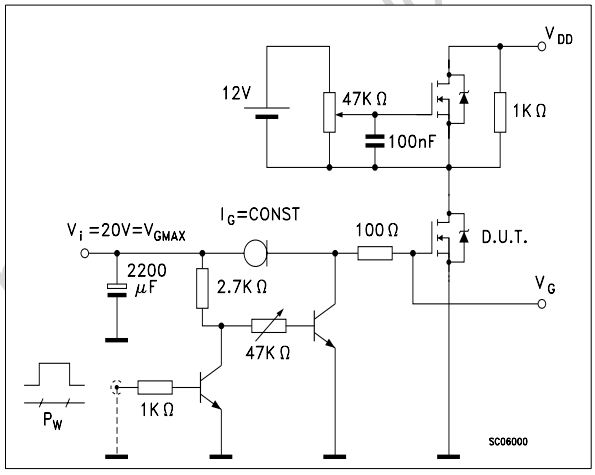
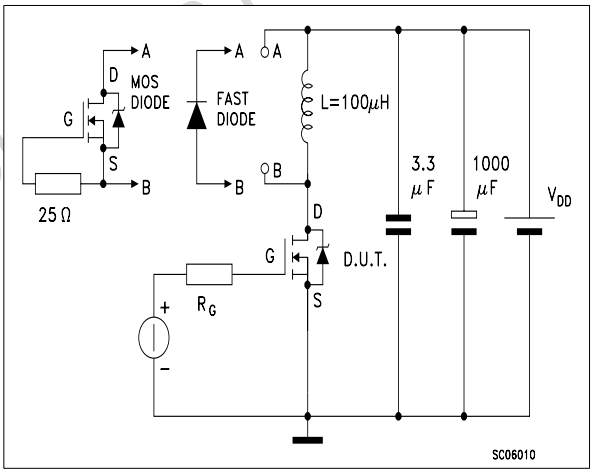
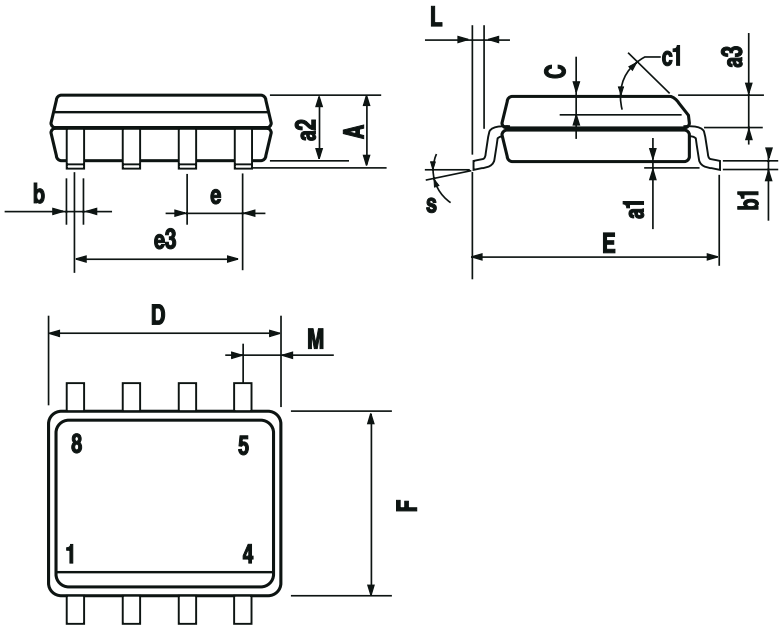


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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