

## 4th Generation USB 2.0 Flash Media Controller with Integrated Card Power FETs

### PRODUCT FEATURES

Datasheet

- Complete System Solution for interfacing SmartMedia™ (SM) or xD Picture Card™ (xD)<sup>1</sup>, Memory Stick™ (MS), High Speed Memory Stick (HSMS), Memory Stick PRO (MSPRO), MS Duo™, Secure Digital (SD), Mini-Secure Digital (Mini-SD), TransFlash (SD), MultiMediaCard™ (MMC), Reduced Size MultiMediaCard (RS-MMC), NAND Flash, Compact Flash™ (CF) and CF Ultra™ I & II, and CF form-factor ATA hard drives to USB 2.0 bus
  - Supports USB Bulk Only Mass Storage Compliant Bootable BIOS
- Support for simultaneous operation of all above devices. (only one at a time of each of the following groups supported: CF or ATA drive, SM or XD or NAND, SD or MMC)
- On-Chip 4-Bit High Speed Memory Stick and MS PRO Hardware Circuitry
- On-Chip firmware reads and writes High Speed Memory Stick and MS PRO
- 1-bit ECC correction performed in hardware for maximum efficiency
- Hardware support for SD Security Command Extensions
- On-chip power FETs for supplying flash media card power with minimum board components
- USB Bus Power Certified
- 3.3 Volt I/O with 5V input tolerance on VBUS/GPIO3
- Complete USB Specification 2.0 Compatibility for Bus Powered Operation
  - Includes USB 2.0 Transceiver
  - A Bi-directional Control and a Bi-directional Bulk Endpoint are provided.
- 8051 8 bit microprocessor
  - Provides low speed control functions
  - 30 Mhz execution speed at 4 cycles per instruction average
  - 12K Bytes of internal SRAM for general purpose scratchpad
  - 768 Bytes of internal SRAM for general purpose scratchpad or program execution while re-flashing external ROM
- Double Buffered Bulk Endpoint
  - Bi-directional 512 Byte Buffer for Bulk Endpoint
  - 64 Byte RX Control Endpoint Buffer
  - 64 Byte TX Control Endpoint Buffer
- Internal or External Program Memory Interface
  - 64K Byte Internal Code Space or Optional 64K Byte External Code Space using Flash, SRAM or EPROM memory.
- On Board 24Mhz Crystal Driver Circuit
- Can be clocked by 48MHz external source
- On-Chip 1.8V Regulator for Low Power Core Operation
- Internal PLL for 480Mhz USB 2.0 Sampling, Configurable MCU clock
- Supports firmware upgrade via USB bus if “boot block” Flash program memory is used
- 15 GPIOs for special function use: LED indicators, button inputs, power control to memory devices, etc.
  - Inputs capable of generating interrupts with either edge sensitivity
  - Attribute bit controlled features:
    - Activity LED polarity/operation/blink rate
    - Full or Partial Card compliance checking
    - Bus or Self Powered
    - LUN configuration and assignment
    - Write Protect Polarity
    - SmartDetach™ Detach from USB when no Card Inserted for Notebook apps
    - Cover Switch operation for xD compliance
    - Inquiry Command operation
    - SD Write Protect operation
    - Older CF card support
    - Force USB 1.1 reporting
    - Internal or External Power FET operation
- Compatible with Microsoft WinXP, WinME, Win2K SP3, Apple OS10, Softconnex, and Linux Multi-LUN Mass Storage Class Drivers
- Win2K, Win98/98SE and Apple OS8.6 and OS9 Multi-LUN Mass Storage Class Drivers available from SMSC
- 128 Pin VTQFP Lead-free RoHS Compliant Package (1.0mm height, 14mm x14mm footprint)

<sup>1</sup>.xD Picture Card not applicable to USB2227

**ORDER NUMBERS:****USB2227/USB2228-NU-05 FOR 128 PIN, VTQFP LEAD-FREE ROHS COMPLIANT PACKAGE**

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

Copyright © 2007 SMSC or its subsidiaries. All rights reserved.

Circuit diagrams and other information relating to SMSC products are included as a means of illustrating typical applications. Consequently, complete information sufficient for construction purposes is not necessarily given. Although the information has been checked and is believed to be accurate, no responsibility is assumed for inaccuracies. SMSC reserves the right to make changes to specifications and product descriptions at any time without notice. Contact your local SMSC sales office to obtain the latest specifications before placing your product order. The provision of this information does not convey to the purchaser of the described semiconductor devices any licenses under any patent rights or other intellectual property rights of SMSC or others. All sales are expressly conditional on your agreement to the terms and conditions of the most recently dated version of SMSC's standard Terms of Sale Agreement dated before the date of your order (the "Terms of Sale Agreement"). The product may contain design defects or errors known as anomalies which may cause the product's functions to deviate from published specifications. Anomaly sheets are available upon request. SMSC products are not designed, intended, authorized or warranted for use in any life support or other application where product failure could cause or contribute to personal injury or severe property damage. Any and all such uses without prior written approval of an Officer of SMSC and further testing and/or modification will be fully at the risk of the customer. Copies of this document or other SMSC literature, as well as the Terms of Sale Agreement, may be obtained by visiting SMSC's website at <http://www.smsc.com>. SMSC is a registered trademark of Standard Microsystems Corporation ("SMSC"). Product names and company names are the trademarks of their respective holders.

**SMSC DISCLAIMS AND EXCLUDES ANY AND ALL WARRANTIES, INCLUDING WITHOUT LIMITATION ANY AND ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND AGAINST INFRINGEMENT AND THE LIKE, AND ANY AND ALL WARRANTIES ARISING FROM ANY COURSE OF DEALING OR USAGE OF TRADE. IN NO EVENT SHALL SMSC BE LIABLE FOR ANY DIRECT, INCIDENTAL, INDIRECT, SPECIAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES; OR FOR LOST DATA, PROFITS, SAVINGS OR REVENUES OF ANY KIND; REGARDLESS OF THE FORM OF ACTION, WHETHER BASED ON CONTRACT; TORT; NEGLIGENCE OF SMSC OR OTHERS; STRICT LIABILITY; BREACH OF WARRANTY; OR OTHERWISE; WHETHER OR NOT ANY REMEDY OF BUYER IS HELD TO HAVE FAILED OF ITS ESSENTIAL PURPOSE, AND WHETHER OR NOT SMSC HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.**



Datasheet

## Table of Contents

---

<b>Chapter 1</b>	<b>General Description</b> .....	<b>6</b>
<b>Chapter 2</b>	<b>Acronyms</b> .....	<b>7</b>
<b>Chapter 3</b>	<b>Pin Configuration</b> .....	<b>8</b>
<b>Chapter 4</b>	<b>Block Diagram</b> .....	<b>9</b>
<b>Chapter 5</b>	<b>Pin Descriptions</b> .....	<b>10</b>
5.1	PIN Descriptions .....	10
5.2	Buffer Type Descriptions .....	18
<b>Chapter 6</b>	<b>DC Parameters</b> .....	<b>20</b>
6.1	Maximum Guaranteed Ratings .....	20
6.2	Recommended Operating Conditions .....	21
6.3	Capacitance .....	23
<b>Chapter 7</b>	<b>Package Outlines</b> .....	<b>24</b>
<b>Chapter 8</b>	<b>GPIO Usage</b> .....	<b>25</b>

## List of Tables

Table 5.1	USB2227/USB2228 Buffer Type Descriptions . . . . .	18
Table 6.1	DC Electrical Characteristics . . . . .	21
Table 7.1	USB2227/USB2228 128-Pin VTQFP Package Parameters . . . . .	24
Table 8.1	GPIO Usage (ROM Rev -11) . . . . .	25



**Datasheet**

## List of Figures

Figure 3.1	USB2227/USB2228 128-Pin VTQFP .....	8
Figure 4.1	USB2227/USB2228 Block Diagram .....	9
Figure 7.1	USB2227/USB2228 128-Pin VTQFP Package Outline .....	24

## Chapter 1 General Description

The USB2227/USB2228 is a USB 2.0 Bulk Only Mass Storage Class Peripheral Controller intended for supporting CompactFlash (CF and CF Ultra I/II) in True IDE Mode only, SmartMedia (SM) and xD cards, Memory Stick (MS), Memory Stick DUO (MSDUO) and Memory Stick Pro (MSPRO), Secure Digital (SD), and MultiMediaCard (MMC) flash memory devices. It provides a single chip solution for the most popular flash memory cards in the market.

The device consists of a USB 2.0 PHY and SIE, buffers, Fast 8051 microprocessor with expanded scratchpad, and program SRAM, and CF, MS, SM and SD controllers. The SD controller supports both SD and MMC devices. SM controller supports both SM and xD cards.

Provisions for external Flash Memory up to 64K bytes for program storage is provided.

12K bytes of scratchpad SRAM and 768 Bytes of program SRAM are also provided.

Fifteen GPIO pins are provided for indicators, external serial EEPROM for OEM id and system configuration information, and other special functions.

Internal power FETs are provided to directly supply power to the xD/SM, MMC/SD and MS/MSPRO cards.

The internal ROM program is capable of implementing any combination of single or multi-LUN CF/SD/MMC/SM/MS reader functions with individual card power control and activity indication. SMSC also provides licenses\*\* for Win98 and Win2K drivers and setup utilities. Note: Please check with SMSC for precise features and capabilities for the current ROM code release.

\*Note: In order to develop, make, use, or sell readers and/or other products using or incorporating any of the SMSC devices made the subject of this document or to use related SMSC software programs, technical information and licenses under patent and other intellectual property rights from or through various persons or entities, including without limitation media standard companies, forums, and associations, and other patent holders may be required. These media standard companies, forums, and associations include without limitation the following: Sony Corporation (Memory Stick, Memory Stick Pro); SD3 LLC (Secure Digital); MultiMedia Card Association (MultiMediaCard); the SSFDC Forum (SmartMedia); the Compact Flash Association (Compact Flash); and Fuji Photo Film Co., Ltd., Olympus Optical Co., Ltd., and Toshiba Corporation (xD-Picture Card). SMSC does not make such licenses or technical information available; does not promise or represent that any such licenses or technical information will actually be obtainable from or through the various persons or entities (including the media standard companies, forums, and associations), or with respect to the terms under which they may be made available; and is not responsible for the accuracy or sufficiency of, or otherwise with respect to, any such technical information.

SMSC's obligations (if any) under the Terms of Sale Agreement, or any other agreement with any customer, or otherwise, with respect to infringement, including without limitation any obligations to defend or settle claims, to reimburse for costs, or to pay damages, shall not apply to any of the devices made the subject of this document or any software programs related to any of such devices, or to any combinations involving any of them, with respect to infringement or claimed infringement of any existing or future patents related to solid state disk or other flash memory technology or applications ("Solid State Disk Patents"). By making any purchase of any of the devices made the subject of this document, the customer represents, warrants, and agrees that it has obtained all necessary licenses under then-existing Solid State Disk Patents for the manufacture, use and sale of solid state disk and other flash memory products and that the customer will timely obtain at no cost or expense to SMSC all necessary licenses under Solid State Disk Patents; that the manufacture and testing by or for SMSC of the units of any of the devices made the subject of this document which may be sold to the customer, and any sale by SMSC of such units to the customer, are valid exercises of the customer's rights and licenses under such Solid State Disk Patents; that SMSC shall have no obligation for royalties or otherwise under any Solid State Disk Patents by reason of any such manufacture, use, or sale of such units; and that SMSC shall have no obligation for any costs or expenses related to the customer's obtaining or having obtained rights or licenses under any Solid State Disk Patents.

**SMSC MAKES NO WARRANTIES, EXPRESS, IMPLIED, OR STATUTORY, IN REGARD TO INFRINGEMENT OR OTHER VIOLATION OF INTELLECTUAL PROPERTY RIGHTS. SMSC DISCLAIMS AND EXCLUDES ANY AND ALL WARRANTIES AGAINST INFRINGEMENT AND THE LIKE.**

No license is granted by SMSC expressly, by implication, by estoppel or otherwise, under any patent, trademark, copyright, mask work right, trade secret, or other intellectual property right.

\*\*To obtain this software program the appropriate SMSC Software License Agreement must be executed and in effect. Forms of these Software License Agreements may be obtained by contacting SMSC.

## Chapter 2 Acronyms

**SM:** SmartMedia

**SMC:** SmartMedia Controller

**FM:** Flash Media

**FMC:** Flash Media Controller

**CF:** Compact Flash

**CFC:** CompactFlash Controller

**SD:** Secure Digital

**SDC:** Secure Digital Controller

**MMC:** MultiMediaCard

**MS:** Memory Stick

**MSC:** Memory Stick Controller

**TPC:** Transport Protocol Code.

**ECC:** Error Checking and Correcting

**CRC:** Cyclic Redundancy Checking

# Chapter 3 Pin Configuration

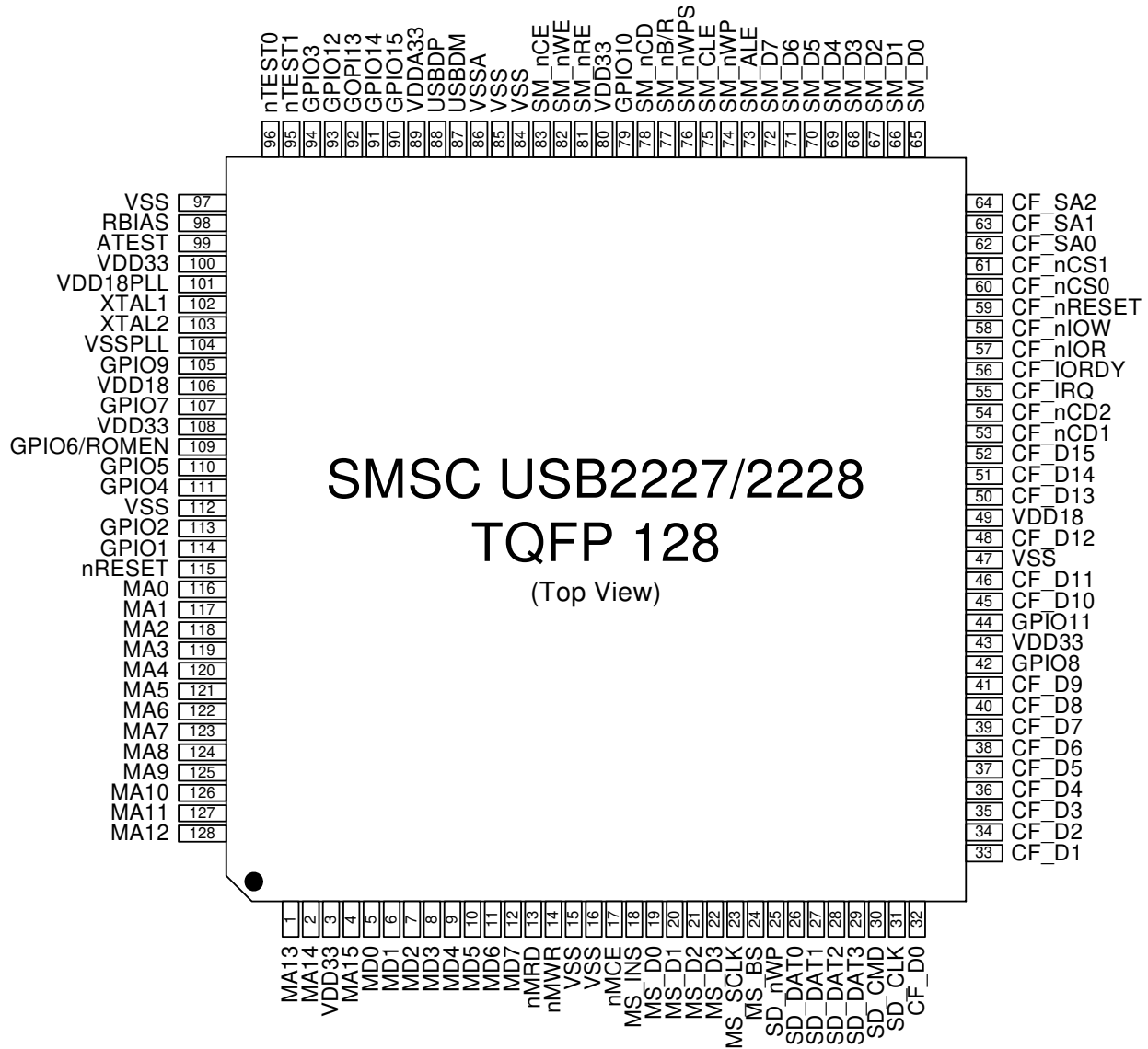


Figure 3.1 USB2227/USB2228 128-Pin VTQFP



# Chapter 4 Block Diagram

Revision 1.93 (10-08-07)

9  
 DATASHEET

SMSC USB2227/USB2228

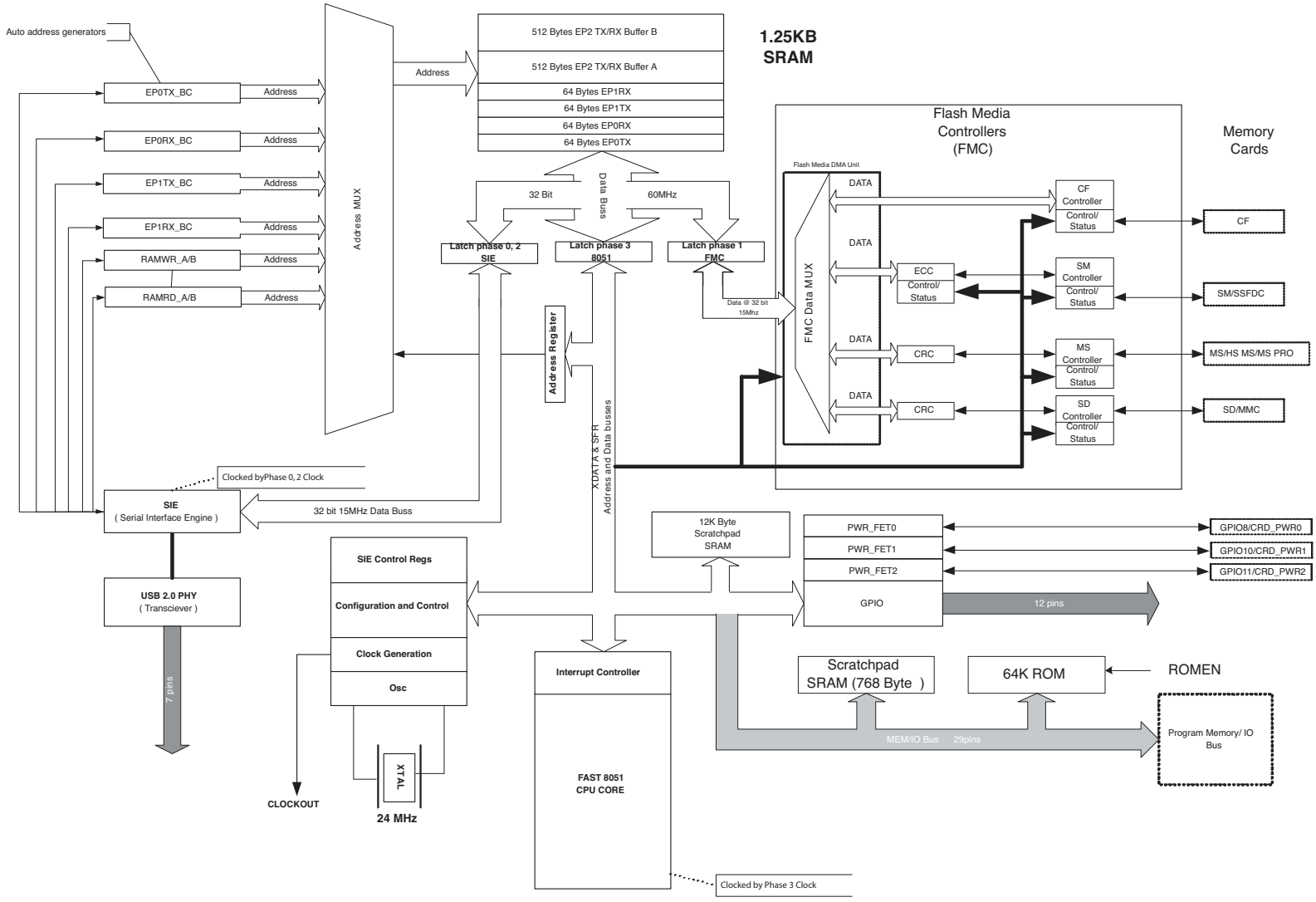


Figure 4.1 USB2227/USB2228 Block Diagram

## Chapter 5 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “n” symbol in the signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “n” is not present before the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signal. The term assert, or assertion indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation indicates that a signal is inactive.

### 5.1 PIN Descriptions

SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
<b>CompactFlash (In True IDE mode) INTERFACE</b>			
CF_nCS1	61	O8PU	CF Chip Select 1: This pin is the active low chip select 1 signal for the CF ATA device.
CF_nCS0	60	O8PU	CF Chip Select 0: This pin is the active low chip select 0 signal for the task file registers of CF ATA device in the True IDE mode.
CF_SA2	64	O8	CF Register Address 2: This pin is the register select address bit 2 for the CF ATA device.
CF_SA1	63	O8	CF Register Address 1: This pin is the register select address bit 1 for the CF ATA device.
CF_SA0	62	O8	CF Register Address 0: This pin is the register select address bit 0 for the CF ATA device.
CF_IRQ	55	IPD	CF Interrupt: This is the active high interrupt request signal from the CF device.
CF_D[15:8]	52 51 50 48 46 45 41 40	I/O8PD	CF Data 15-8: The bi-directional data signals CF_D15-CF_D8 in True IDE mode data transfer.  In the True IDE Mode, all of task file register operation occur on the CF_D[7:0], while the data transfer is on CF_D[15:0].  The bi-directional data signal has an internal weak pull-down resistor.

## Datasheet

SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
CF_D[7:0]	39 38 37 36 35 34 33 32	I/O8PD	CF Data 7-0: The bi-directional data signals CF_D7-CF_D0 in the True IDE mode data transfer. In the True IDE Mode, all of task file register operation occur on the CF_D[7:0], while the data transfer is on CF_D[15:0]. The bi-directional data signal has an internal weak pull-down resistor.
CF_IORDY	56	IPU	IO Ready: This pin is active high input signal. This pin has an internally controlled weak pull-up resistor.
CF_nCD2	54	IPU	CF Card Detection2: This card detection pin is connected to the ground on the CF device, when the CF device is inserted. This pin has an internally controlled weak pull-up resistor.
CF_nCD1	53	IPU	CF Card Detection1: This card detection pin is connected to ground on the CF device, when the CF device is inserted. This pin has an internally controlled weak pull-up resistor.
CF_nRESET	59	O8	CF Hardware Reset: This pin is an active low hardware reset signal to CF device.
CF_nIOR	57	O8	CF IO Read: This pin is an active low read strobe signal for CF device.
CF_nIOW	58	O8	CF IO Write Strobe: This pin is an active low write strobe signal for CF device.
<b>SmartMedia INTERFACE</b>			
SM_nWP	74	O8PD	SM Write Protect: This pin is an active low write protect signal for the SM device. This pin has a weak pull-down resistor that is permanently enabled.
SM_ALE	73	O8PD	SM Address Strobe: This pin is an active high Address Latch Enable signal for the SM device. This pin has a weak pull-down resistor that is permanently enabled.
SM_CLE	75	O8PD	SM Command Strobe: This pin is an active high Command Latch Enable signal for the SM device. This pin has a weak pull-down resistor that is permanently enabled.

SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
SM_D[7:0]	72 71 70 69 68 67 66 65	I/O8PD	SM Data 7-0:  These pins are the bi-directional data signal SM_D7-SM_D0.  The bi-directional data signal has an internal weak pull-down resistor.
SM_nRE	81	08PU	SM Read Enable:  This pin is an active low read strobe signal for SM device.  When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET.
		08	If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used, and should be connected to the applicable Card Power Supply).
SM_nWE	82	08PU	SM Write Enable:  This pin is an active low write strobe signal for SM device.  When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET.
		08	If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used, and should be connected to the applicable Card Power Supply).
SM_nWPS	76	IPU	SM Write Protect Switch:  A write-protect seal is detected, when this pin is low.  This pin has an internally controlled weak pull-up resistor.
SM_nB/R	77	I	SM Busy or Data Ready:  This pin is connected to the BSY/RDY pin of the SM device.  An external pull-up resistor is required on this signal. The pull-up resistor must be pulled up to the same power source that powers the SM/NAND flash device.
SM_nCE	83	08PU	SM Chip Enable:  This pin is the active low chip enable signal to the SM device.  When using the internal FET, this pin has an internal weak pull-up resistor that is tied to the output of the internal Power FET.
		08	If an external FET is used (Internal FET is disabled), then the internal pull-up is not available (external pull-ups must be used, and should be connected to the applicable Card Power Supply).
SM_nCD	78	IPU	SM Card Detection:  This is the card detection signal from SM device to indicate if the device is inserted.  This pin has an internally controlled weak pull-up resistor.

## Datasheet

SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
<b>MEMORY STICK INTERFACE</b>			
MS_BS	24	O8	MS Bus State: This pin is connected to the BS pin of the MS device. It is used to control the Bus States 0, 1, 2 and 3 (BS0, BS1, BS2 and BS3) of the MS device.
MS_SDIO/MS_D0	19	I/O8PD	MS System Data In/Out: This pin is a bi-directional data signal for the MS device. Most significant bit (MSB) of each byte is transmitted first by either MSC or MS device. The bi-directional data signal has an internal weak pull-down resistor.
MS_D1	20	I/O8PD	MS System Data In/Out: This pin is a bi-directional data signal for the MS device. This pin has internally controlled weak pull-up and pull-down resistors for various operational modes.
MS_D[3:2]	22 21	I/O8PD	MS System Data In/Out: This pin is a bi-directional data signal for the MS device. The bi-directional data signal has an internal weak pull-down resistor.
MS_INS	18	IPU	MS Card Insertion: This pin is the card detection signal from the MS device to indicate, if the device is inserted. This pin has an internally controlled weak pull-up resistor.
MS_SCLK	23	O8	MS System CLK: This pin is an output clock signal to the MS device. The clock frequency is software configurable.
<b>SD INTERFACE</b>			
SD_DAT[3:0]	29 28 27 26	I/O8PU	SD Data 3-0: These are bi-directional data signals. These pins have internally controlled weak pull-up resistors.
SD_CLK	31	O8	SD Clock: This is an output clock signal to SD/MMC device. The clock frequency is software configurable.
SD_CMD	30	I/O8PU	SD Command: This is a bi-directional signal that connects to the CMD signal of SD/MMC device. This pin has an internally controlled weak pull-up resistor.

SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
SD_nWP	25	IPD	SD Write Protected: This pin is an input signal with an internal weak pull-down. This pin has an internally controlled weak pull-down resistor.
<b>USB INTERFACE</b>			
USBDM USBDP	87 88	IO-U	USB Bus Data: These pins connect to the USB bus data signals.
RBIAS	98	I	USB Transceiver Bias: A 12.0kΩ, ± 1.0% resistor is attached from VSSA to this pin, in order to set the transceiver's internal bias currents.
ATEST	99	AIO	Analog Test: This signal is used for testing the analog section of the chip and should be connected to VDDA33 for normal operation.
VDD18PLL	101		1.8v Power for the PLL
VSSPLL	104		PLL Ground Reference: Ground Reference for 1.8v PLL power
VDDA33	89		3.3v Analog Power
VSSA	86		Analog Ground Reference: Analog Ground Reference for 3.3v Analog Power.
XTAL1/ CLKIN	102	ICLKx	Crystal Input/External Clock Input: 24Mhz Crystal or external clock input. This pin can be connected to one terminal of the crystal or can be connected to an external 24Mhz clock when a crystal is not used. <b>Note:</b> The MA[2:0] pins will be sampled while nRESET is asserted, and the value will be latched upon nRESET negation. This will determine the clock source and value.
XTAL2	103	OCLKx	Crystal Output: 24Mhz Crystal This is the other terminal of the crystal, or left open when an external clock source is used to drive XTAL1/CLKIN. It may not be used to drive any external circuitry other than the crystal circuit.
<b>MEMORY/IO INTERFACE</b>			
MD[7:0]	12 11 10 9 8 7 6 5	I/O8PU	Memory Data Bus: When ROMEN bit of GPIO_IN1 register = 0, these signals are used to transfer data between the internal CPU and the external program memory. These pins have internally controlled weak pull-up resistors.

## Datasheet

SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
MA[15:3]	4 2 1 128 127 126 125 124 123 122 121 120 119	O8	Memory Address Bus:  These signals address memory locations within the external memory.
MA2/ SEL_CLKDRV	118	I/O8PD	<p>Memory Address Bus:</p> <p>MA2 Addresses memory locations within the external memory.</p> <p>SEL_CLKDRV. During nRESET assertion, this pins will select the operating clock mode (crystal or externally driven clock source), and a weak pull-down resistor is enabled. When nRESET is negated, the value will be internally latched and this pin will revert to MA2 functionality, the internal pull-down will be disabled.</p> <p>'0' = Crystal operation (24MHz only) '1' = Externally driven clock source (24MHz or 48MHz)</p> <p><b>Note:</b> If the latched value is '1', then the MA2 pin is tri-stated when the following conditions are true:</p> <ol style="list-style-type: none"> <li>1. IDLE bit (PCON.0) is 1.</li> <li>2. INT2 is negated</li> <li>3. SLEEP bit of CLOCK_SEL is 1.</li> </ol> <p>If the latched value is '0', then the MA2 pin will function identically to the MA[15:3] pins at all times (other than during nRESET assertion).</p>

SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
MA[1:0]/CLK_SEL[1:0]	117 116	I/O8PD	Memory Address Bus: MA[1:0], These signals address memory locations within the external memory.
			SEL[1:0]. During nRESET assertion, these pins will select the operating frequency of the external clock, and the corresponding weak pull-down resistors are enabled. When nRESET is negated, the value on these pins will be internal latched and these pins will revert to MA[1:0] functionality, the internal pull-downs will be disabled.  SEL[1:0] = '00'. 24MHz SEL[1:0] = '01'. RESERVED SEL[1:0] = '10'. RESERVED SEL[1:0] = '11'. 48MHz  <b>Note:</b> If the latched value is '1', then the corresponding MA pin is tri-stated when the following conditions are true: <ol style="list-style-type: none"> <li>1. IDLE bit (PCON.0) is 1.</li> <li>2. INT2 is negated</li> <li>3. SLEEP bit of CLOCK_SEL is 1.</li> </ol> If the latched value is '0', then the corresponding MA pin will function identically to the MA[15:3] pins at all times (other than during nRESET assertion).
nMWR	14	O8	Memory Write Strobe: Program Memory Write; active low
nMRD	13	O8	Memory Read Strobe: Program Memory Read; active low
nMCE	17	O8	Memory Chip Enable: Program Memory Chip Enable; active low.  This signal is asserted, when any of the following conditions are no longer met: <ol style="list-style-type: none"> <li>1. IDLE bit (PCON.0) is 1.</li> <li>2. INT2 is negated</li> <li>3. SLEEP bit of CLOCK_SEL is 1.</li> </ol> <b>Note:</b> This signal is held to a logic 'high' while nRESET is asserted.
<b>MISC</b>			
GPIO1	114	I/O8	General Purpose I/O: This pin may be used either as input, edge sensitive interrupt input, or output.
GPIO2	113	I/O8	General Purpose I/O: This pin may be used either as input, edge sensitive interrupt input, or output.
GPIO3	94	I/O8	General Purpose I/O: This pin may be used either as input, edge sensitive interrupt input, or output.



## Datasheet

SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
GPIO4	111	I/O8	General Purpose I/O: This pin may be used either as input, edge sensitive interrupt input, or output.
GPIO5	110	I/O8	General Purpose I/O: This pin may be used either as input, edge sensitive interrupt input, or output.
GPIO6/ ROMEN	109	IPU	GPIO6, ROMEN: This pin has an internal weak pull-up resistor that is enabled or disabled by the state of nRESET. The pull-up is enabled when nRESET is active. The pull-up is disabled, when the nRESET is inactive (some clock cycles later, after the rising edge of nRESET).  The state of this pin is latched internally on the rising edge of nRESET to determine if internal or external program memory is used. The state latched is stored in ROMEN bit of GPIO_IN1 register.
		I/O8	After the rising edge of nRESET, this pin may be used as GPIO6 or RXD.  When pulled low via an external weak pull-down resistor, an external program memory should be connected to the memory data bus. The USB2227/USB2228 uses this external bus for program execution.  When this pin is left unconnected or pulled high by a weak pull-up resistor, the USB2227/USB2228 uses the internal ROM for program execution.
GPIO7	107	I/O8	General Purpose I/O: This pin may be used either as input, edge sensitive interrupt input, or output.
GPIO8/ CRD_PWR0	42	I/O8	General Purpose I/O or Card Power: GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			CRD_PWR: Card Power drive of 3.3V @ 100mA.
GPIO9	105	I/O8	General Purpose I/O: This pin may be used either as input, edge sensitive interrupt input, or output.
GPIO10/ CRD_PWR1	79	I/O8	General Purpose I/O or Card Power: GPIO: These pins may be used either as input, edge sensitive interrupt input, or output.
			CRD_PWR: Card Power drive of 3.3V @ 100mA.
GPIO11/ CRD_PWR2	44	I/O8	General Purpose I/O or Card Power: GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			CRD_PWR: Card Power drive of 3.3V @ 200mA.

SYMBOL	128-PIN VTQFP	BUFFER TYPE	DESCRIPTION
GPIO[15:12]	90 91 92 93	I/O8	General Purpose I/O: These pins may be used either as input, or output.
nRESET	115	IS	RESET input: This active low signal is used by the system to reset the chip. The active low pulse should be at least 1µs wide.
nTEST[1:0]	95 96	I	TEST input: These signals are used for testing the chip. User should normally tie them high externally, if the test function is not used.
<b>DIGITAL POWER, GROUNDS, and NO CONNECTS</b>			
VDD18	49 106		1.8v Digital Core Power: +1.8V Core power All VDD18 pins must be connected together on the circuit board.
VDD33	3 43 80 100 108		3.3v Power & Voltage Regulator Input: 3.3V Power & Regulator Input. pins 100 & 108 supply 3.3V power to the internal 1.8V regulators.
VSS	15 16 47 84 85 97 112		Ground: Ground Reference

**Notes:**

- Hot-insertion capable card connectors are required for all flash media. It is required for SD connector to have Write Protect switch. This allows the chip to detect MMC card.
- nMCE is normally asserted except when the 8051 is in standby mode.
- VDD18 (Pin 106) and VDD18PLL (Pin 101) must have a 10µF +/-20% Low-ESR (equivalent series resistance) <0.1 ohm bypass capacitor to VSSA. These capacitors must be as close to these pins as possible.

## 5.2 Buffer Type Descriptions

**Table 5.1 USB2227/USB2228 Buffer Type Descriptions**

BUFFER	DESCRIPTION
I	Input
IPU	Input with internal weak pull-up resistor.
IPD	Input with internal weak pull-down resistor.
IS	Input with Schmitt trigger

## Datasheet

Table 5.1 USB2227/USB2228 Buffer Type Descriptions (continued)

BUFFER	DESCRIPTION
I/O8	Input/Output buffer with 8mA sink and 8mA source.
I/O8PU	Input/Output buffer with 8mA sink and 8mA source, with an internal weak pull-up resistor.
I/O8PD	Input/Output buffer with 8mA sink and 8mA source, with an internal weak pull-down resistor.
O8	Output buffer with 8mA sink and 8mA source.
O8PU	Output buffer with 8mA sink and 8mA source, with an internal weak pull-up resistor.
O8PD	Output buffer with 8mA sink and 8mA source, with an internal weak pull-down resistor.
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I/O-U	Analog Input/Output Defined in USB specification
AIO	Analog Input/Output

## Chapter 6 DC Parameters

### 6.1 Maximum Guaranteed Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Storage Temperature	$T_A$	-55	150	°C	
Lead Temperature			325	°C	Soldering < 10 seconds
3.3V supply voltage	$V_{DD33}$ , $V_{DDA33}$	-0.5	4.0	V	
Voltage on GPIO3 & USBDP/DM pins		-0.5	$(3.3V \text{ supply voltage} + 2) \leq 6$	V	
Voltage on GPIO8,10&11		-0.5	$V_{DD33} + 0.3$	V	When internal power FET operation of these pins is enabled, these pins may be simultaneously shorted to ground or any voltage up to 3.63V indefinitely, without damage to the device as long as $V_{DD33}$ and $V_{DDA33}$ are less than 3.63V and $T_A$ is less than 70 °C.
Voltage on any signal pin		-0.5	$V_{DD33} + 0.3$	V	
Voltage on XTAL1		-0.5	4.0	V	
Voltage on XTAL2		-0.5	$V_{DD18} + 0.3$	V	

**Note:** Stresses above the specified parameters may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied.

**Note:** When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

## 6.2 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Operating Temperature	$T_A$	0	70	°C	
3.3V supply voltage	$V_{DD33}$ , $V_{DDA33}$	3.0	3.6	V	
Voltage on GPIO3 & USBDP/DM pins		-0.3	5.5	V	If any 3.3V supply voltage drops below 3.0V, then the MAX becomes: $(3.3V \text{ supply voltage}) + 0.5 \leq 5.5$
Voltage on any signal pin		-0.3	$V_{DD33}$	V	
Voltage on XTAL1		-0.3	$V_{DDA33}$	V	
Voltage on XTAL2		-0.3	$V_{DD18}$	V	

Table 6.1 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
<b>I,IPU &amp; IPD Type Input Buffer</b>						
Low Input Level	$V_{ILI}$			0.8	V	TTL Levels
High Input Level	$V_{IHI}$	2.0			V	
Pull Down	PD		72		$\mu A$	
Pull Up	PU		58		$\mu A$	
<b>IS Type Input Buffer</b>						
Low Input Level	$V_{ILI}$			0.8	V	TTL Levels
High Input Level	$V_{IHI}$	2.0			V	
Hysteresis	$V_{HYSI}$		500		mV	
<b>ICLK Input Buffer</b>						
Low Input Level	$V_{ILCK}$			0.4	V	
High Input Level	$V_{IHCK}$	2.2			V	
<b>Input Leakage</b> (All I and IS buffers)						
Low Input Leakage	$I_{IL}$	-10		+10	$\mu A$	$V_{IN} = 0$
High Input Leakage	$I_{IH}$	-10		+10	mA	$V_{IN} = V_{DD33}$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
<b>O8, O8PU &amp; O8PD Type Buffer</b>						
Low Output Level	$V_{OL}$			0.4	V	$I_{OL} = 8 \text{ mA @ } V_{DD33} = 3.3\text{V}$
High Output Level	$V_{OH}$	$V_{DD33} - 0.4$			V	$I_{OH} = -8\text{mA @ } V_{DD33} = 3.3\text{V}$
Output Leakage	$I_{OL}$	-10		+10	$\mu\text{A}$	$V_{IN} = 0 \text{ to } V_{DD33}$ (Note 6.1)
Pull Down	PD		72		$\mu\text{A}$	
Pull Up	PU		58		$\mu\text{A}$	
<b>I/O8, I/O8PU &amp; I/O8PD Type Buffer</b>						
Low Output Level	$V_{OL}$			0.4	V	$I_{OL} = 8 \text{ mA @ } V_{DD33} = 3.3\text{V}$
High Output Level	$V_{OH}$	$V_{DD33} - 0.4$			V	$I_{OH} = -8 \text{ mA @ } V_{DD33} = 3.3\text{V}$
Output Leakage	$I_{OL}$	-10		+10	$\mu\text{A}$	$V_{IN} = 0 \text{ to } V_{DD33}$ (Note 6.1)
Pull Down	PD		72		$\mu\text{A}$	
Pull Up	PU		58		$\mu\text{A}$	
<b>IO-U</b> (Note 6.2)						
<b>Integrated Power FET for GPIO8 &amp; GPIO10 (and GPIO11 when used with Firmware version -03 or older)</b>						
Output Current	$I_{OUT}$	100			mA	GPIO8 or 10; $V_{dropFET} = 0.23\text{V}$
Short Circuit Current Limit	$I_{SC}$			140	mA	GPIO8 or 10; $V_{outFET} = 0\text{V}$
On Resistance	$R_{DSON}$			2.1	$\Omega$	GPIO8 or 10; $I_{FET} = 70\text{mA}$
Output Voltage Rise Time	$t_{DSON}$			800	$\mu\text{s}$	GPIO8 or 10; $C_{LOAD} = 10\mu\text{F}$

## Datasheet

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
<b>Integrated Power FET for GPIO11 (only when used with Firmware version -04 or later)</b>						
Output Current	$I_{OUT}$	200			mA	GPIO11; $V_{drop_{FET}} = 0.46V$
Short Circuit Current Limit	$I_{SC}$			181	mA	GPIO11; $V_{out_{FET}} = 0V$
On Resistance	$R_{DSON}$			2.1	$\Omega$	GPIO11; $I_{FET} = 70mA$
Output Voltage Rise Time	$t_{DSON}$			800	$\mu s$	GPIO11; $C_{LOAD} = 10\mu F$
Supply Current Unconfigured	$I_{CCINIT}$		55	80	mA	
Supply Current Active (Full Speed)	$I_{CC}$		75	90	mA	
Supply Current Active (High Speed)	$I_{CC}$		75	100	mA	
Supply Current Standby	$I_{CSBY}$		305	420	$\mu A$	

**Note 6.1** Output leakage is measured with the current pins in high impedance.

**Note 6.2** See Appendix A for USB DC electrical characteristics.

**Note 6.3** The Maximum power dissipation parameters of the package should not be exceeded

**Note 6.4** The assignment of each Integrated Card Power FET to a designated Card Connector is controlled by both firmware and the specific board implementation. Firmware will default to the settings listed in [Table 8.1, "GPIO Usage \(ROM Rev -11\)," on page 25.](#)

## 6.3 Capacitance

$T_A = 25^\circ C$ ;  $f_c = 1MHz$ ;  $V_{DD18}, V_{DD18PLL} = 1.8V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	$C_{IN}$			20	pF	All pins except USB pins (and pins under test tied to AC ground)
Input Capacitance	$C_{IN}$			10	pF	
Output Capacitance	$C_{OUT}$			20	pF	

## Chapter 7 Package Outlines

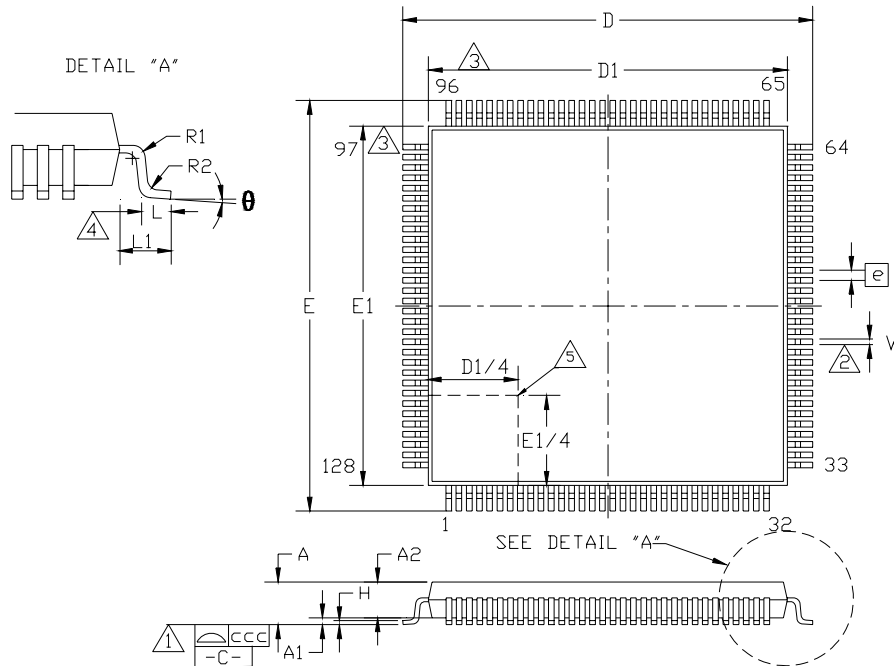


Figure 7.1 USB2227/USB2228 128-Pin VTQFP Package Outline

Table 7.1 USB2227/USB2228 128-Pin VTQFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.20	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	0.95	~	1.05	Body Thickness
D	15.80	~	16.20	X Span
D1	13.80	~	14.20	X body Size
E	15.80	~	16.20	Y Span
E1	13.80	~	14.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.40 Basic			Lead Pitch
q	0°	~	7°	Lead Foot Angle
W	0.13	0.18	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

**Notes:**

- Controlling Unit: millimeter.
- Tolerance on the true position of the leads is  $\pm 0.035$  mm maximum.  
Package body dimensions D1 and E1 do not include the mold protrusion.
- Maximum mold protrusion is 0.25 mm.
- Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
- Details of pin 1 identifier are optional but must be located within the zone indicated.



## Chapter 8 GPIO Usage

Table 8.1 GPIO Usage (ROM Rev -11)

NAME	ACTIVE LEVEL	SYMBOL	DESCRIPTION AND NOTE
GPIO1	H	Flash Media Activity LED/ xD_Door	Indicates media activity. Media or USB cable must not be removed with LED lit. Also may be used for xD Door functionality
GPIO2	H	EE_CS	Serial EE PROM chip select
GPIO3	H	V_BUS	USB V bus detect
GPIO4	H	EE_DIN/EE_DOUT/xDID	Serial EE PROM input/output and xD Identify
GPIO5	L	HS_IND/SD_CD	HS Indicator LED or SD Card Detect Switch input
GPIO6	H	A16/ROMEN	A16 address line connect for DFU or debug LED indicator optional.
GPIO7	H	EE_CLK/ UNCONF_LED	Serial EE PROM clock output or Unconfigured LED.
GPIO8	L	MS_PWR_CTRL/ CRD_PWR0	Memory Stick Card Power Control, or Internal Power FET0.
GPIO9	L	CF_PWR_CTRL	CompactFlash Card Power Control
GPIO10	L	SM_PWR_CTRL/ CRD_PWR1	SmartMedia Card Power Control, or Internal Power FET1.
GPIO11	L	SD/MMC_PWR_CTRL/ CRD_PWR2	SD/MMC Card Power Control, or Internal Power FET2.
GPIO12	H	MS_ACT_IND/ Media Activity	Memory Stick Activity Indicator, or Media Activity LED.
GPIO13	H	CF_ACT_IND	CompactFlash Activity Indicator
GPIO14	H	SM_ACT_IND	SmartMedia Activity Indicator
GPIO15	H	SD/MMC_ACT_IND	SD/MMC Activity Indicator