PT5810 Series

EXCALIBUR

20-A 3.3-V Input Adjustable Integrated Switching Regulator

SLTS174 - JANUARY 2003 - REVISED APRIL 2003

Features

- 3.3 V Input
- 20 A Output Current
- DSP Compatible
- Low-Profile (8 mm)
- >90 % Efficiency
- Output Margin Control (±5 %)
- Adjustable Output Voltage
- Pre-Bias Startup Capability
- On/Off Inhibit Function
- Over-Current Protection
- Thermal Shutdown
- Small Footprint (0.736 in², Suffix 'N')
- Surface Mount Compatible
- IPC Lead Free 2

Description

The PT5810 Excalibur™ series of integrated switching regulators (ISRs) combines outstanding power density with a comprehensive list of features. They are an ideal choice for applications where board space is a premium and performance cannot be compromised. These modules provide a full 20 A of output current, yet are housed in a low-profile, 18-pin, package that is almost half the size of the previous product generation. The integral copper case construction requires no heatsink, and offers the advantages of solderability and a small footprint (0.736 in² for suffix 'N'). Both through-hole and surface mount pin configurations are available.

The PT5810 series operates from a 3.3-V input bus to provide a convenient point-of-load power source for the industry's latest high-performance DSPs and microprocessors. The series includes output voltage options as low as 1.0 VDC.

Other features include external output voltage adjustment, a ±5 % margin control, on/off inhibit, short circuit protection, thermal shutdown, and a differential remote sense.

Ordering Information

PT5812❒	= 2.5 Volts
PT5813❒	= 1.8 Volts
PT5814❒	= 1.5 Volts
PT5815❒	= 1.2 Volts
PT5816❒	= 1.0 Volts

PT Series Suffix (PT1234x)

Case/Pin Configuration	Order Suffix	Package Code
Vertical	**N**	(EPP)
Horizontal	**A**	(EPQ)
SMD	**C**	(EPS)

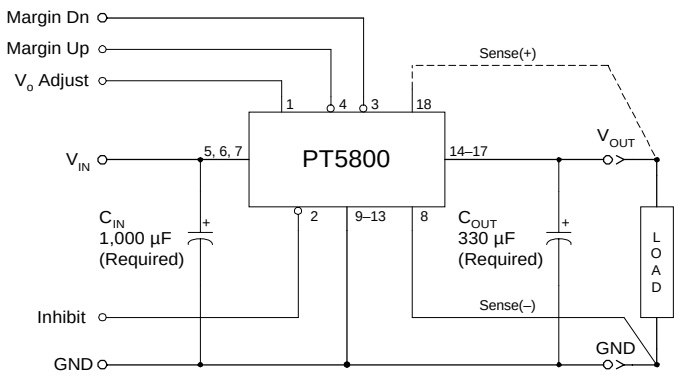
(Reference the applicable package code drawing for the dimensions and PC board layout)

Pin-Out Information

Pin	Function
1	V_o Adjust
2	Inhibit*
3	Margin Dn*
4	Margin Up*
5	V_{in}
6	V_{in}
7	V_{in}
8	Sense(–)
9	GND
10	GND
11	GND
12	GND
13	GND
14	V_{out}
15	V_{out}
16	V_{out}
17	V_{out}
18	Sense(+)

** Denotes negative logic:*
Open = Normal operation
Ground = Function active

Standard Application



C_{in} = Required 1,000 µF
C_{out} = Required 330 µF

Specifications (Unless otherwise stated, T_a =25 °C, V_{in} =3.3 V, V_{out} =1.8 V, C_{in} =1,000 µF, C_{out} =330 µF, and I_o =$I_o$max)

Characteristics	Symbols	Conditions	PT5810 SERIES Min	Typ	Max	Units
Output Current	I_o		0	—	20	A
Input Voltage Range	V_{in}	Over I_o range	2.95 (1)	—	3.65	V
Set-Point Voltage Tolerance	V_o tol		—	—	±2	%V_o
Temperature Variation	ΔReg_{temp}	–40°C <T_a < +85 °C	—	±0.5	—	%V_o
Line Regulation	ΔReg_{line}	Over V_{in} range	—	±4	—	mV
Load Regulation	ΔReg_{load}	Over I_o range	—	±2	—	mV
Total Output Variation	ΔReg_{tot}	Includes set-point, line, load, –40°C ≤ T_a ≤ +85 °C	—	—	±3	%V_o
Efficiency	η	I_o =12 A PT5812 (2.5 V)	—	93	—	%
		PT5813 (1.8 V)	—	90	—	
		PT5814 (1.5 V)	—	89	—	
		PT5815 (1.2 V)	—	87	—	
		PT5816 (1.0 V)	—	84	—	
V_o Ripple (pk-pk)	V_r	20 MHz bandwidth	—	20	—	mVpp
Transient Response		1 A/µs load step, 50 to 100 % $I_o$max,				
	t_{tr}	Recovery Time	—	50	—	µSec
	ΔV_{tr}	V_o over/undershoot	—	120	—	mV
Over-Current Threshold	I_{TRIP}	Reset, followed by auto-recovery	—	30	—	A
Output Voltage Adjust	V_o adj	With V_o Adjust	—	±15 (2)	—	%
		With Margin Up/Dn	—	±5	—	
Switching Frequency	f_s	Over V_{in} and I_o ranges	250	300	350	kHz
Inhibit Control (pin 2)		Referenced to GND (pins 9–13)				V
Input High Voltage	V_{IH}		V_{in} –0.5	—	Open (3)	
Input Low Voltage	V_{IL}		–0.2	—	0.6	
Input Low Current	I_{IL}	Pin 2 to GND	—	–0.2	—	mA
Standby Input Current	I_{in} standby	Pin 2 to GND	—	5	—	mA
External Input Capacitance	C_{in}		1,000 (4)	—	—	µF
External Output Capacitance	C_{out}		330 (5)	—	5,000	µF
Operating Temperature Range	T_a	Over V_{in} range	–40 (5)	—	+85 (6)	°C
Over-Temperature Protection	OTP	Measured at center of case, auto-reset	—	110	—	°C
Solder Reflow Temperature	T_{reflow}	Surface temprature of module pins or case	—	—	215 (7)	°C
Storage Temperature	T_s	—	-40	—	+125	°C
Reliability	MTBF	Per Bellcore TR-332 50% stress, T_a =40°C, ground benign	5.8	—	—	10^6 Hrs
Mechanical Shock		Mil-STD-883D, Method 2002.3 Half Sine, mounted to a fixture	—	500	—	G's
Mechanical Vibration		Mil-STD-883D, Method 2007.2, 20-2000 Hz, PCB mounted	—	20 (8)	—	G's
Weight	—	—	—	20	—	grams
Flammability	—	Materials meet UL 94V-0				

Notes: *(1) The minimum input voltage is equal to 2.95 V or Vout + 0.75 V, whichever is greater.*
(2) This is a typical value. For the adjustment limits of a specific model consult the related application note on output voltage adjustment.
(3) The Inhibit control (pin 2) has an internal pull-upto V_{in}, and if left open-circuit the module will operate when input power is applied. A small low-leakage (<100nA) MOSFET is recommended to control this input. See application notes for more information.
(4) A 1,000 µF electrolytic input capacitor is required for proper operation. This capacitor must be rated for a minimumm of 0.7 Arms of ripple current.
(5) For operation below 0 °C, C_{OUT} must have stable characteristics. Use either low-ESR tantalum or Oscon® type capacitors.
(6) See SOA curves or consult factory for the appropriate derating.
(7) During solder reflow of SMD package version do not elevate the module case, pins, or internal component temperatures above a peak of 215 °C. For further guidance refer to the application note, "Reflow Soldering Requirements for Plug-in Power Surface Mount Products," (SLTA051)
(8) The case pins on the through-hole package types (suffixes N & A) must be soldered. For more information see the applicable package outline drawing.

Pin Descriptions

Vin: The positive supply voltage input for the module with respect to the common ground *(GND)*.

Vout: This is the regulated output voltage from the module with respect to the common ground (*GND*).

GND: The common node to which the input, output, and external control signals are referenced.

Sense(–): Provides the regulator with the ability to sense the set-point voltage directly across the load. For optimum output voltage accuracy this pin should always be connected to *GND*, even for applications that demand a relatively light load.

Sense(+): When used with *Sense(–)*, the regulation circuitry will compensate for voltage drop between the converter and the load. The pin may be left open circuit, but connecting it to V_{out} will optimize load regulation.

Inhibit*: This is an open-collector (open-drain) negative logic input that is referenced to *GND*. Pulling this pin to *GND* disables the module's output voltage. If *Inhibit** is left open-circuit, the output will be active whenever a valid input source is applied.

V_o Adjust: This pin is used to trim the output voltage to a value within the range of ±10 % of nominal. The adjustment method uses an external resistor. The resistor is connected from *V_o Adjust* to either the *(-)Sense* or *(+)Sense*, in order to adjust the output up or down, respectively.

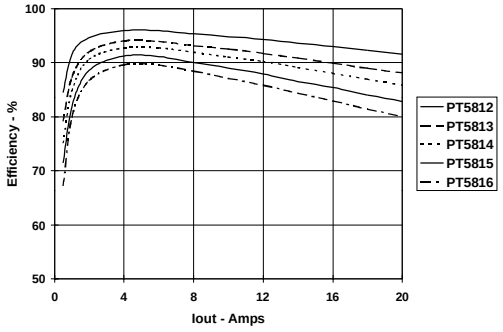
Margin Dn*: When this open-collector (open-drain) input is asserted to *GND*, the output voltage is automatically decreased by 5 % from the nominal. This feature is used in applications where the load circuit must be tested for operation at the extreme values of its supply voltage tolerance.

Margin Up*: This is an open-collector (open-drain) input. When this is asserted to *GND*, the output voltage is automatically increased by 5 % from the nominal.

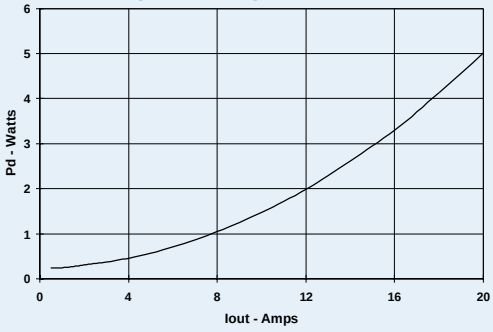
Typical Characteristics

Performance Data; V_{in} =3.3 V (See Note A)

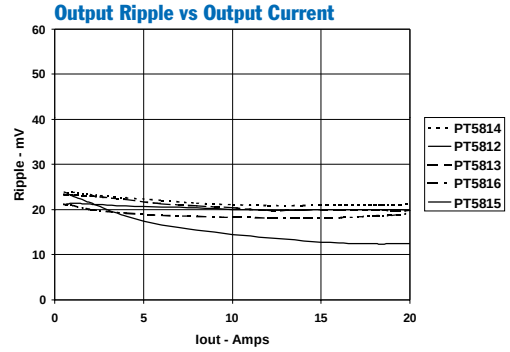
Efficiency vs Output Current



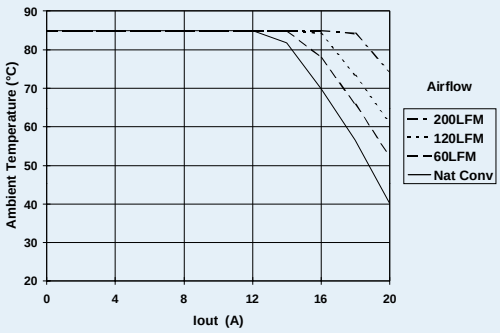
Power Dissipation vs Output Current



Output Ripple vs Output Current



Safe Operating Curves; V_{in} =3.3 V (See Note B)



Note A: *Characteristic data has been developed from actual products tested at 25 °C. This data is considered typical data for the ISR.*
Note B: *SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.*

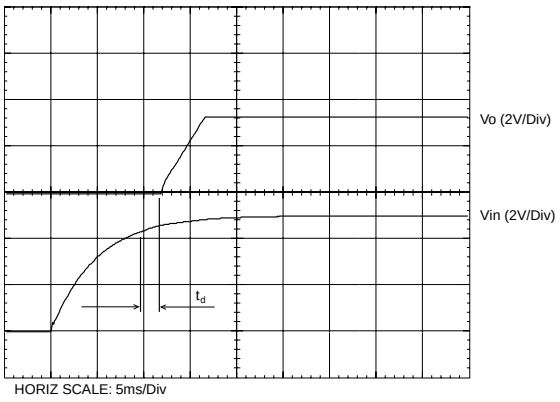
Operating Features and System Considerations for the PT5800 & PT5810 Regulator Series

The PT5800 (5-V input) and the PT5810 (3.3-V input) series of integrated switching regulators (ISRs) provide step-down voltage conversion for output loads of up to 20 A.

Power up & Soft-Start Timing

Following either the application of a valid input source voltage, or the removal of a ground signal to the *Inhibit** control pin (with input power applied), the regulator will initiate a soft-start power up. The soft start slows the rate at which the output voltage rises, and also introduces a short time delay, t_d (approx. 2 ms). Figure 1-1 shows the power-up characteristic of a PT5801 (3.3 V) with a 10-A load.

Figure 1-1



Differential Remote Sense

Connecting the *Sense(+)* and *Sense(-)* pins to the load circuit allows the regulator to compensate for limited amounts of 'IR' voltage drop. This voltage drop is caused by current flowing through the connection resistance between the regulator and the 'point of regulation' some distance away. Leaving the sense pins disconnected will not damage the regulator or load circuitry. An internal 15 Ω resistor, connected between each sense pin and its corresponding output node, keeps the output voltage in regulation. However, it is important to connect *Sense(–)* to *GND* locally, as this provides a return path for the regulator's internal bias currents.

With the sense leads connected, the difference between the voltage measured at V_{out} and *GND* pins, and that measured from *Sense(+)* to *Sense(–)*, is the amount of IR drop being compensated by the regulator. This should be limited to 0.6 V. (0.3 V maximum between pins 17 & 18, and also between pins 8 & 9).

Note: The remote sense feature is not designed to compensate for the forward drop of non-linear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connections they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

Over-Current Protection

To protect against load faults, the regulators incorporate output over-current protection. Applying a load that exceeds the regulator's over-current threshold (see data sheet specifications) will cause the regulated output to shut down. Following shutdown the ISR will periodically attempt to recover by initiating a soft-start power-up. This is often described as a "hiccup" mode of operation, whereby the module continues in the cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the converter automatically recovers and returns to normal operation.

Over-Temperature Protection

An on-board temperature sensor protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold (see data sheet specifications), the regulator's *Inhibit** control is automatically pulled low. This disables the regulator, allowing the output voltage to drop to zero as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the the sensed temperature decreases by about 10 °C below the trip point.

Note: The over-temperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and will reduce the long-term reliability of the module. Always operate the regulator within the specified Safe Operating Area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

Startup of the PT5800 & PT5810 Series ISRs with Back-Feeding Source (Pre-Bias Capability)

In complex digital systems an external voltage can sometimes be present at the output of the regulator during power up. For example, this voltage may be backfed through a dual-supply logic component such as an FPGA or ASIC. Another path might be via a clamp diode (to a lower supply voltage) as part of a power-up sequencing implementation.

Although the PT5800 (5-V input) and PT5810 (3.3-V input) series of regulators will sink current under steady-state operating conditions, they will not do so during startup [1] as long as certain conditions are maintained [2]. This feature allows these regulators to start up while an external voltage is simultaneously applied to the output. Figure 2-1 is an application schematic that demonstrates this capability. The waveforms in Figure 2-2 show the behavior of the circuit as input power is applied. Note that the plot of the regulator output current (I_o) is approximately zero up to the timestamp 'A', even though a voltage is initially backfed to the output via the 3.3-V input supply and diodes D_1 & D_2. The regulator sources current [3] when it begins raising the output above the back-fed voltage to its nominal regulation value.

Notes

1. Startup includes both the application of a valid input source voltage, or the removal of a ground signal from the *Inhibit** control (pin 2) with a valid input source applied. The output of the regulator is effectively off (tri-state), during the period that the *Inhibit** control is held low.
2. To ensure that the regulator does not sink current, the input voltage must always be greater or equal to the output voltage throughout the power-up and power-down sequence.
3. If an external source backfeeding the regulator's output is greater than the nominal regulation voltage, the output will begin sinking current at the end of its soft-start power-up sequence. If this current exceeds the rated output, the module could be overstressed.

Figure 2-2; Power-up Waveforms with Back-Feeding Source

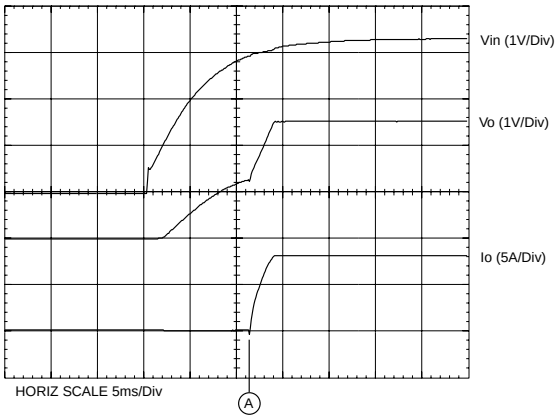
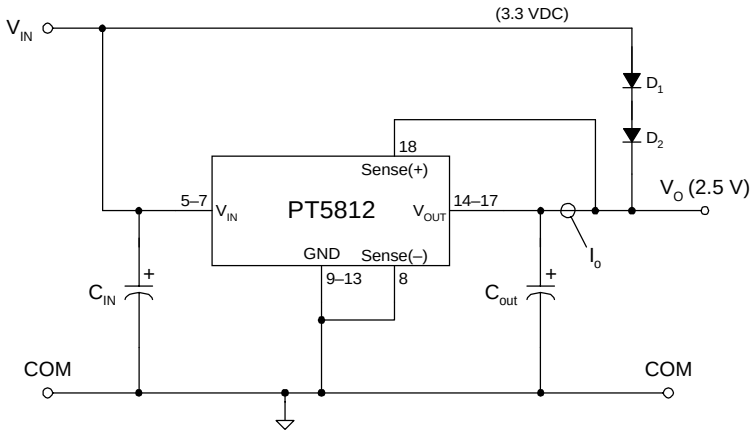


Figure 2-1; Schematic Demonstrating Startup into Pre-Bias Capability



Capacitor Recommendations for the PT5800 & PT5810 Step-Down Regulator Series

Input Capacitor:

The recommended input capacitance is determined by a 700-mA ripple current rating and the following minimum capacitance requirements.

- PT5800 = 820 µF minimum capacitance
- PT5810 = 1000 µF minimum capacitance

Ripple current and <100 mΩ equivalent series resistance (ESR) values are the major considerations, along with temperature, when designing with different types of capacitors. Tantalum capacitors have a recommended minimum voltage rating of twice the maximum DC voltage + AC ripple. This is necessary to ensure reliability for input voltage bus applications

Output Capacitors

The ESR of the capacitors is less than 100mΩ. Electrolytic capacitors have marginal ripple performance at frequencies greater than 400 kHz, but excellent low frequency transient response. Above the ripple frequency ceramic capacitors are necessary. Ceramic capacitors improve the transient response and reduce any high frequency noise components apparent during high current excursions. Preferred low-ESR electrolytic capacitor part numbers are identified in Table 3-1.

Tantalum Capacitors (Optional Output Capacitors)

Tantalum type capacitors can be used for the output but only the AVX TPS series, Sprague 593D/594/595 series, or Kemet T495/T510 series. These capacitors are recommended over many other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution the TAJ series by AVX is not recommended. This series has considerably higher ESR, reduced power dissipation, and lower ripple current capability. The TAJ series is less reliable than the AVX TPS series when determining power dissipation capability. Tantalum or Oscon® types are recommended for applications where ambient temperatures fall below 0°C.

Capacitor Table

Table 2-1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The number of capacitors required at both the input and output buses is identified for each capacitor type.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (Equivalent Series Resistance) at 100 kHz are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

Table 3-1; Input/Output Capacitors

Capacitor Vendor/Series	Capacitor Characteristics					Quantity		
	Working Voltage	Value (µF)	(ESR) Equivalent Series Resistance	Ripple Current I(rms)max @105°C	Physical Size (mm)	Input Bus	Output Bus	Vendor Part Number
Panasonic FC (Radial) FK (SMT)	10V 10V 10V 35V	1000 560 1000 470	0.068Ω 0.090Ω 0080Ω 0.060Ω	1050mA 755mA 850mA 1100mA	10×16 10×12.5 10×10.2 12.5×13.5	1 2 1 2	1 1 1 1	EEUFC1C102 EEUFC1A561 EEVFK1A102P EEVFK1V471Q
United Chemi-con LXZ/LXV Series FX Series	16V 10V 10V	470 1000 680	0.090Ω 0.068Ω 0.015Ω	760mA 1050mA 4735mA	10×12.5 10×16 10×10.5	2 1 2	1 1 1	LXZ16VB471M10X12LL LXZ10VB102M10X16LL 10FX680M
Nichicon PL/PM Series NX Series (SMT)	10V 16V 10V	1000 560 330	0.065Ω 0.080Ω 0.024Ω	1040mA 920mA 3770mA	12.5×15 12.5×15 10×8	1 2 3	1 1 1	UPM1A102MHH6 UPM1C 561MHH6 PNX1A330MCR1GS
Sanyo Os-con: SP SVP (SMT)	10V 10V	470 560	0.015Ω 0.013Ω	>4500mA >5200mA	10×10.5 11×12.7	2 2	1 1	10SP470**M** 10SVP560M
AVX Tantalum TPS (SMT)	10V 10V	470 470	0.045Ω 0.060Ω	1723mA 1826mA	7.3L ×5.7W ×4.1H	2 2	1 1	TPSE477M010R00**4**5 TPSV477M010R0060
Kemet Polymer Tantalum T520/T530Series (SMT)	10V 10V	330 330	0.040Ω 0.015Ω	1800mA >3800mA	7.3×4.3×4	3 3	1 1	T520X337M010AS T530X337M010AS
Sprague Tantalum 594D Series (SMT)	10V	680	0.090Ω	1660mA	7.2×6×4.1	2	1	595D687X0010R2T

Using the Inhibit Control of the PT5800 & PT5810 Series of Step-Down ISRs

For applications requiring output voltage On/Off control, the PT5800 & PT5810 series of ISRs incorporate an inhibit function. This function can be used wherever there is a requirement for the output voltage from the ISR to be turned off. The On/Off function is provided by the *Inhibit** control (pin 2).

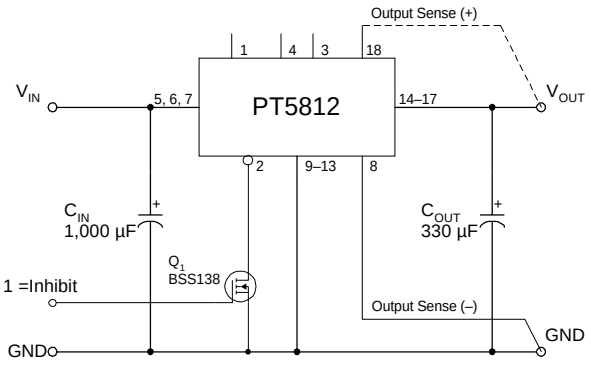
The ISR functions normally with pin 2 open-circuit, providing a regulated output whenever a valid source voltage is applied between V_{in} (pins 5–7) and *GND* (pins 9–13). When a low-level ground signal is applied to pin 2, the regulator output is turned off [2].

Figure 4-1 shows the typical application of the *Inhibit** function. Note the discrete transistor (Q_1). The *Inhibit** control has its own internal pull-up to $+V_{in}$ potential. An open-collector or open-drain device is recommended to control this input [1]. The voltage thresholds are given in Table 4-1.

Table 4-1; Inhibit Control Requirements

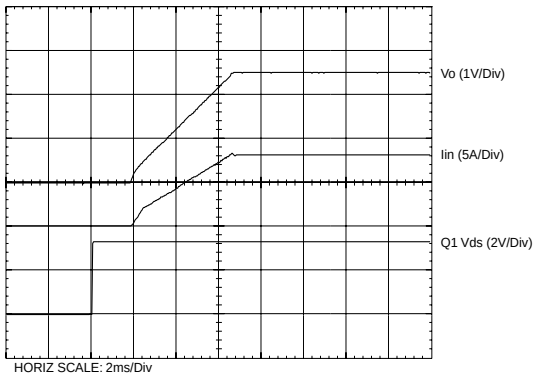
Parameter	Min	Typ	Max
Enable (V_{IH})	V_{in} – 0.5 V	—	Open
Disable (V_{IL})	–0.2 V	—	+0.6 V
I_{IL}	—	–0.2 mA	—

Figure 4-1



Turn-On Time: In the circuit of Figure 4-1, turning Q_1 on applies a low-voltage to the *Inhibit** control (pin 2) and disables the output of the regulator [2]. If Q_1 is then turned off, the ISR executes a soft-start power up. Power up consists of a short delay (approx. 2msec), followed by a period in which the output voltage rises to its full regulation voltage. The module produces a regulated output voltage within 10msec. Figure 4-2 shows the typical rise in both the output voltage and input current for a PT5812 (2.5 V), following the turn-off of Q_1. The turn off of Q_1 corresponds to the rise in the waveform, Q_1 V_{ds}. The waveforms were measured with a 3.3 VDC input voltage, and 10-A load.

Figure 4-2



Notes:

1. Use an open-collector device with a breakdown voltage of at least 10 V (preferably a discrete transistor) for the *Inhibit** input. A pull-up resistor is not necessary. To disable the output voltage the control pin should be pulled low to less than +0.8 VDC.
2. When a ground signal is applied to the *Inhibit** control (pin 2) the module output is turned off (tri-state). The output voltage decays to zero as the load impedance discharges the output capacitors.

Adjusting the Output Voltage of the PT5800 & PT5810 Step-Down Series of Regulators

Using Margin Up/ Margin Down

The *Margin Up** (pin 4) and *Margin Dn** (pin 3) control inputs allow the output voltage to be easily adjusted by up to ±5 % of the nominal set-point voltage. To activate, simply connect the appropriate control input to the *Sense(–)* (pin 8), or the local starpoint ground. Either a logic level MOSFET or a p-channel JFET is recommended for this purpose. For further information see the related application note on this feature.

Using the 'V_o Adjust' Control

For a more permanent and precise adjustment, use the *Vo Adjust* control (pin 1). The *V_o Adjust* control allows adjustment in any increment by up to ±10% of the set-point. The adjustment method requires the addition of a single external resistor. Table 5-1 gives the allowable adjustment range for each model of the series as V_a (min) and V_a (max). The value of the external resistor can either be calculated using the formulas given below, or simply selected from the range of values provided in Table 5-2. Refer to Figure 5-1 for the placement of the required resistor. Use the resistor R_1 to adjust up, and the resistor (R_2) to adjust down.

Adjust Up: An increase in the output voltage is obtained by adding a resistor R_1, between *V_o Adjust* (pin 1) and *Sense(–)* (pin 8). See Figure 5-1.

Adjust Down: Add a resistor (R_2), between *V_o Adjust* (pin 1) and *Sense(+)* (pin 18). See Figure 5-1.

Notes:

1. Use a 1% (or better) tolerance resistor in either the R_1 or (R_2) location. Place the resistor as close to the ISR as possible.
2. Never connect capacitors from *V_o Adjust* to either *GND* or *V_{out}*. Any capacitance added to the *V_o Adjust* pin will affect the stability of the ISR.
3. If the remote sense feature is not being used, the adjust resistor (R_2) can be connected to *V_{out}*, (pins 14-17) instead of *Sense (+)*.
4. The PT5812 may not be adjusted higher than the nominal output voltage of 2.5 V. There is insufficient input voltage between V_{in} and V_{out} to accommodate an increase in the output voltage.

V_o Adjust Resistor Calculations

The values of R_1 [adjust up] and (R_2) [adjust down] can also be calculated using the following formulas. Again, use Figure 5-1for the placement of the required resistor; either R_1 or (R_2) as appropriate.

$$R_1 = \frac{V_r \cdot R_o}{V_a - V_o} - 24.9 \quad k\Omega$$

$$(R_2) = \frac{R_o (V_a - V_r)}{V_o - V_a} - 24.9 \quad k\Omega$$

Where: V_o = Original output voltage
V_a = Adjusted output voltage
V_r = The reference voltage in Table 5-1
R_o = The resistance constant in Table 5-1

Figure 5-1; V_o Adjust Resistor Placement

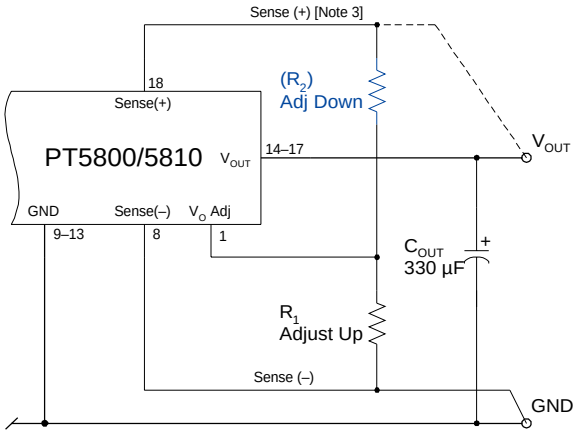


Table 5-1

ISR OUTPUT VOLTAGE ADJUSTMENT RANGE AND FORMULA PARAMETERS

Series Pt. No.						
5.0V Bus	**PT5801**	**PT5802**	**PT5803**	**PT5804**	**PT5805**	**PT5806**
3.3V Bus	**N/A**	**PT5812 4**	**PT5813**	**PT5814**	**PT5815**	**PT5816**
V_o (nom)	3.3 V	2.5 V	1.8 V	1.5 V	1.2 V	1.0 V
V_a (min)	2.6 V	2.0 V	1.52 V	1.31 V	1.1 V	0.94 V
V_a (max)	3.63 V	2.8 V #	2.1 V	1.82 V	1.52 V	1.32 V
V_r	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V
R_o (kΩ)	10.2	10.7	10.2	9.76	10.0	10.2

The PT5812 should not be adjusted higher than its nominal output voltage of 2.5 V. See note 4.

Table 5-2

ISR ADJUSTMENT RESISTOR VALUES

Series Pt. No.						
5.0V Bus	**PT5801**	**PT5802**		**PT5803**	**PT5804**	**PT5805**	**PT5806**
3.3V Bus	**N/A**	**PT5812**		**PT5813**	**PT5814**	**PT5815**	**PT5816**
V_o (nom)	**3.3 V**	**2.5 V**		**1.8 V**	**1.5 V**	**1.2 V**	**1.0V**
V_a (req.d)			**V_a (req.d)**				
3.60	2.3 kΩ		2.100	2.3 kΩ			
3.55	7.7 kΩ		2.050	7.7 kΩ			
3.50	15.9 kΩ		2.000	15.9 kΩ			
3.45	29.5 kΩ		1.950	29.5 kΩ			
3.40	56.7 kΩ		1.900	56.7 kΩ			
3.35	138.0 kΩ		1.850	138.0 kΩ			
3.30			1.800		1.1 kΩ		
3.25	(475.0) kΩ		1.750	(169.0) kΩ	6.3 kΩ		
3.20	(220.0) kΩ		1.700	(66.9) kΩ	14.1 kΩ		
3.15	(135.0) kΩ		1.650	(32.9) kΩ	27.2 kΩ		
3.10	(92.4) kΩ		1.600	(15.9) kΩ	53.2 kΩ		
3.05	(66.9) kΩ		1.550	(5.7) kΩ	131.0 kΩ		
3.00	(49.9) kΩ		1.500			1.8 kΩ	
2.95	(37.5) kΩ		1.475		(239.0) kΩ	4.2 kΩ	
2.90	(28.6) kΩ		1.450		(102.0) kΩ	7.1 kΩ	
2.85	(21.6) kΩ		1.425		(56.4) kΩ	10.7 kΩ	
2.80	(15.9) kΩ	3.6 kΩ	1.400		(33.7) kΩ	15.1 kΩ	
2.75	(11.3) kΩ	9.3 kΩ	1.375		(20.0) kΩ	20.8 kΩ	
2.70	(7.4) kΩ	17.9 kΩ	1.350		(10.9) kΩ	28.4 kΩ	
2.65	(4.1) kΩ	32.2 kΩ	1.325		(4.4) kΩ	39.1 kΩ	
2.60	(1.3) kΩ	60.7 kΩ	1.300			55.1 kΩ	2.3 kΩ
2.550	[Note 4]	146.0 kΩ	1.275			81.8 kΩ	4.8 kΩ
2.500			1.250			135.0 kΩ	7.7 kΩ
2.450		(321.0) kΩ	1.225			295.0 kΩ	11.4 kΩ
2.400		(146.0) kΩ	1.200				15.9 kΩ
2.350		(85.7) kΩ	1.175			(125.0) kΩ	21.7 kΩ
2.300		(55.3) kΩ	1.150			(45.1) kΩ	29.5 kΩ
2.250		(37.2) kΩ	1.125			(18.4) kΩ	40.4 kΩ
2.200		(25.0) kΩ	1.100			(5.1) kΩ	56.7 kΩ
2.150		(16.4) kΩ	1.075				83.9 kΩ
2.100		(9.9) kΩ	1.050				138.0 kΩ
2.050		(4.8) kΩ	1.025				302.0 kΩ
2.000		(0.8) kΩ	1.000				
			0.975				(46.5) kΩ
			0.950				(5.7) kΩ

R_1 = Black R_2 = (Blue)

Using the Margin Up/Down Controls on the PT5800 & PT5810 Regulator Series

The PT5800 & PT5810 series of integrated switching regulator modules incorporate *Margin Up** (pin 4) and *Margin Dn** (pin 3) control inputs. These controls allow the output voltage set point to be momentarily adjusted [1], either up or down, by a nominal 5 %. This provides a convenient method for dynamically testing the load circuit's power supply voltage over its operating margin or range. Note that the ±5 % change is also applied to any adjustment of the output voltage, if made, using the V_o *Adjust* (pin 1).

The 5 % adjustment is made by driving the appropriate margin control input directly to the ground reference at *Sense(-)* (pin 8) [2]. An low-leakage open-drain device, such as a MOSFET or a p-channel JFET is recommended for this purpose. Adjustments of less than 5 % can also be accommodated by adding series resistors to the control inputs (See Figure 6-1). The value of the resistor can be selected from Table 6-1, or calculated using the following formula.

Resistor Value Calculation

To reduce the margin adjustment to something less than 5 %, series padding resistors are required (See R_D and R_U in Figure 6-1). For the same amount of adjustment, the resistor value calculated for R_U and R_D will be the same. The formulas is as follows.

$$R_U/R_D = \frac{499}{\Delta\%} - 99.8 \quad k\Omega$$

Where $\Delta\%$ = The desired amount of margin adjust in percent.

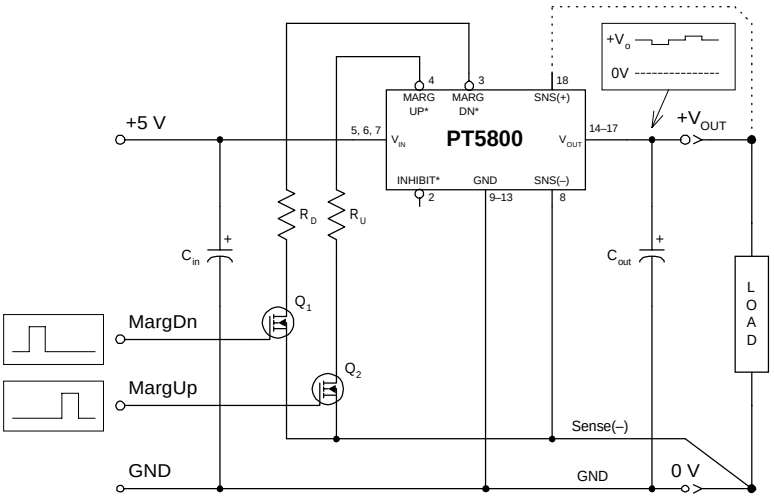
Notes:

1. The *Margin Up** and *Margin Dn** controls were not intended to be activated simultaneously. If they are their affects on the output voltage may not completely cancel, resulting in a slight shift in the output voltage set point.
2. When possible use the *Sense(-)* (pin 8) as the ground reference. This will produce a more accurate adjustment of the output voltage at the load circuit terminals. *GND* (pins 9-13) can be used if the *Sense(-)* pin is connected to *GND* near the regulator.

Table 6-1; Margin Up/Down Resistor Values

PADDING RESISTOR VALUES	
% Adjust	**R_U / R_D**
5	0.0 kΩ
4	24.9 kΩ
3	66.5 kΩ
2	150.0 kΩ
1	397.0 kΩ

Figure 6-1; Margin Up/Down Application Schematic



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