AK4611

4/8-Channel Audio CODEC

GENERAL DESCRIPTION

The AK4611 is a single chip audio CODEC that includes four ADC channels and eight DAC channels. The converters are designed with Enhanced Dual Bit architecture for the ADC's, and Advanced Multi-Bit architecture for the DAC, enabling very low noise performance. Fabricated on a low power process, the AK4611 operates off of a +3.3V analog supply and a +1.8V digital supply. The AK4611 supports both single-ended and differential inputs and outputs. A wide range of applications can be realized, including home theater, pro audio and car audio. The AK4611 is available in an 80-pin LQFP package.

FEATURES

1. 4channel 24bit ADC
- **128x Oversampling**
- **Linear Phase Digital Anti-Alias Filter**
- **Analog Anti-Alias Filter for Single-Ended Input and Differential Input**
- **ADC S/(N+D)**
  - **92dB: Single-Ended Input**
  - **97dB: Differential Input**
- **ADC DR, S/N**
  - **103dB: Single-Ended Input**
  - **104dB: Differential Input**
- **Digital HPF for offset cancellation**
- **I/F format: MSB justified, I^2S or TDM**
- **Overflow flag**

2. 8channel 24bit DAC
- **128x Oversampling**
- **Linear Phase 24bit 8 times Digital Filter**
- **Analog Smoothing Filter for Single-Ended Output**
- **DAC S/(N+D)**
  - **94dB: Single-Ended Output**
  - **100dB: Differential Output**
- **DAC DR, S/N**
  - **105dB: Single-Ended Output**
  - **108dB: Differential Output**
- **Individual channel digital volume with 256 levels and 0.5dB steps**
- **Soft mute**
- **De-emphasis for 32kHz, 44.1kHz and 48kHz**
- **Zero Detect Function**
- **I/F format: MSB justified, LSB justified (16bit, 20bit, 24bit), I^2S or TDM**

3. Sampling Frequency
- **Normal Speed Mode: 32kHz to 48kHz**
- **Double Speed Mode: 64kHz to 96kHz**
- **Quad Speed Mode: 128kHz to 192kHz**

4. Master / Slave mode

5. Master clock
- **Slave mode: 256fs, 384fs or 512fs (Normal Speed Mode: fs=32kHz ~ 48kHz)**
  256fs (Double Speed Mode: fs=64kHz ~ 96kHz)
  128fs (Quad Speed Mode: fs=128kHz ~ 192kHz)
- **Master mode: 256fs or 512fs (Normal Speed Mode: fs=32kHz ~ 48kHz)**
  256fs (Double Speed Mode: fs=64kHz ~ 96kHz)
  128fs (Quad Speed Mode: fs=128kHz ~ 192kHz)

6. 4-wire Serial and I^2C Bus µP I/F for mode setting

7. Power Supply
- **Analog Power Supply: AVDD1, AVDD2 = 3.0 ~ 3.6V**
- **Digital Power Supply: DVDD = 1.6 ~ 2.0V**
- **I/O Buffer Power Supply: TVDD1, TVDD2 = 1.6 ~ 3.6V**

8. Power Supply Current : 81 mA (fs=48kHz)

9. Ta = -20 ~ 85°C (AK4611EQ), - 40 ~ 105°C (AK4611VQ)

10. Package: 80pin LQFP (0.5mm pitch)

■ Block Diagram

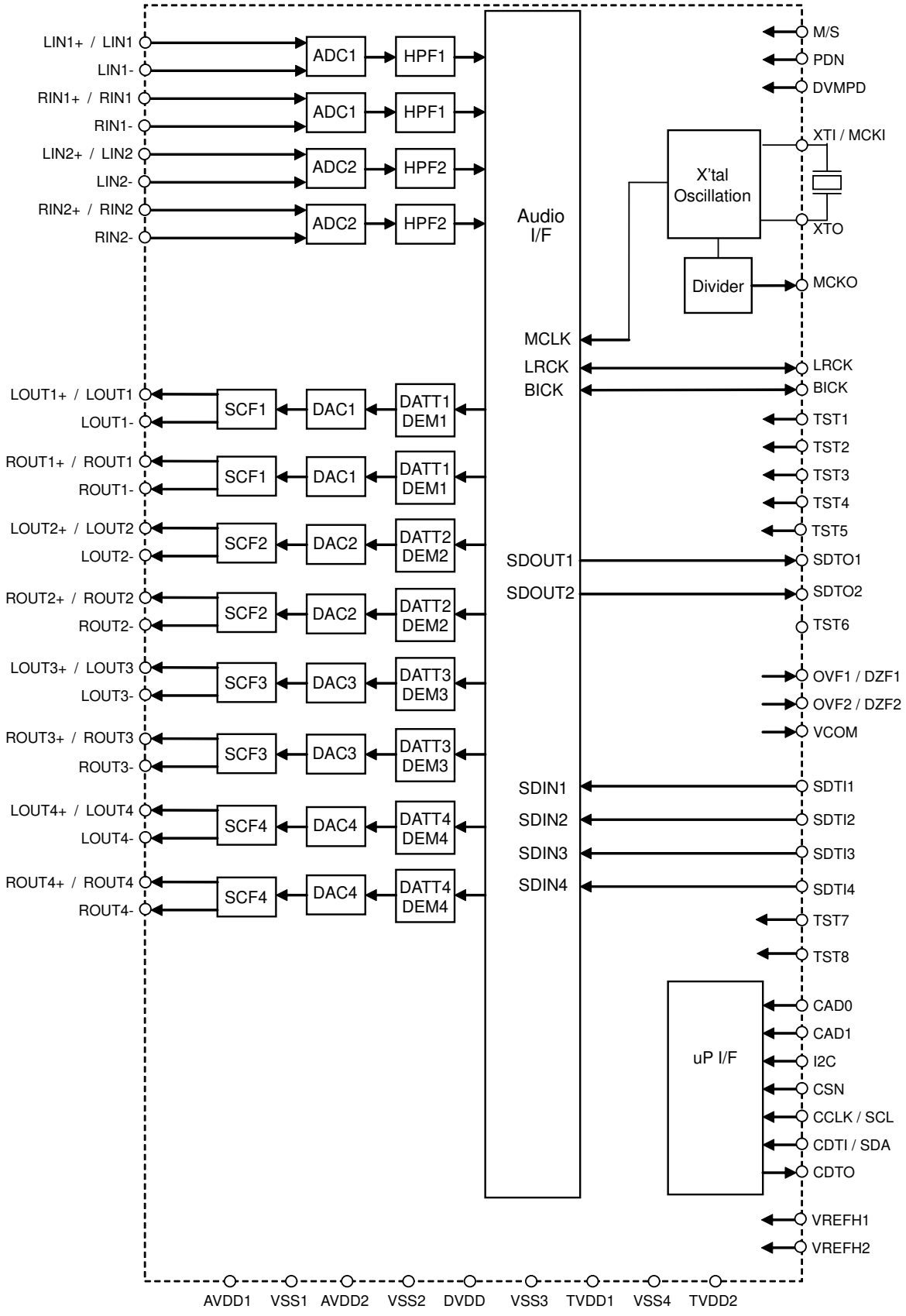


Figure 1. Block Diagram

■ Ordering Guide

AK4611EQ	-20 ~ +85°C	80pin LQFP (0.5mm pitch)
AK4611VQ	-40 ~ +105°C	80pin LQFP (0.5mm pitch)
AKD4611	Evaluation Board for AK4611	

■ Pin Layout

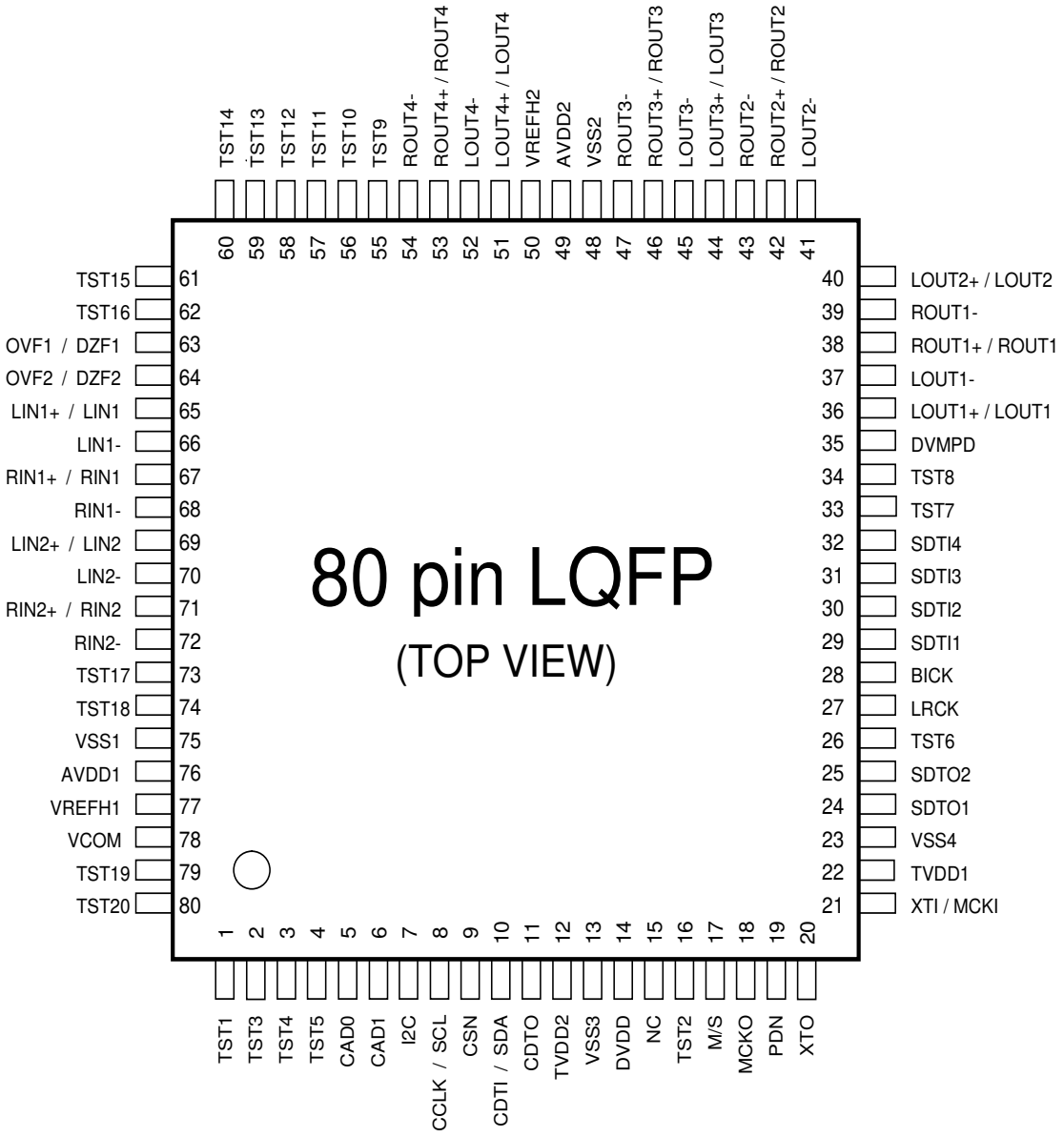


Figure 2. Pin Layout

■ Compatibility with AK4628

1. Functions

Function	AK4628	AK4611
Number of ADC channel	2-channel	4-channel
Number of DAC channel	8-channel	8-channel
Input	Single	Single or Diff
Output	Single	Single or Diff
I/F Format	I2S, LJ, RJ(20/24bit), TDM	I2S, LJ, RJ(16/20/24bit), TDM
TDM512	No	Fs=48kHz
XTAL OSC	No	Yes
Parallel / Serial Select Pin	Yes	No
Control Data Output Pin	No	Yes
Ta	-40 ~ +85°C	-40 ~ +105°C
Package	44pinLQFP	80pinLQFP

2. Power Supply

Voltage Name	AK4628	AK4611
AVDD	4.5 ~ 5.5V	No
AVDD1	No	3.0 ~ 3.6V
AVDD2	No	3.0 ~ 3.6V
DVDD	4.5 ~ 5.5V	1.6 ~ 2.0V
TVDD	2.7 ~ 5.5V	No
TVDD1	No	1.6 ~ 3.6V
TVDD2	No	1.6 ~ 3.6V

3. Specification

Parameter	AK4628	AK4611
Fs (AD/DA)	96k / 192k	192k / 192k
THD+N (AD/DA)	Single: 92 / 90 Differential : - / -	Single: 92 / 94 Differential : 97 / 100
S/N (AD/DA)	Single: 102 / 106 Differential : - / -	Single: 103 / 105 Differential: 104 / 108
Output DATT	128 level	256 level
µP I/F	100k I2C, 3wire	400k I2C, 4wire

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	TST1	I	Test Pin This pin must be connected to VSS4.
2	TST3	I	Test Pin This pin must be connected to TVDD2.
3	TST4	I	Test Pin This pin must be connected to VSS4.
4	TST5	I	Test Pin This pin must be connected to VSS4.
5	CAD0	I	Chip Address 0 Pin
6	CAD1	I	Chip Address 1 Pin
7	I2C	I	µP I/F Mode Select Pin "L": 4-wire Serial, "H": I^2C Bus
8	CCLK	I	Control Data Clock Pin in serial control mode I2C = "L": CCLK (4-wire Serial)
	SCL	I	Control Data Clock Pin in serial control mode I2C = "H": SCL (I^2C Bus)
9	CSN	I	Chip Select Pin in 4-wire serial control mode This pin must be connected to TVDD2 at I^2C bus control mode
10	CDTI	I	Control Data Input Pin in serial control mode I2C = "L": CDTI (4-wire Serial)
	SDA	I/O	Control Data Input Pin in serial control mode I2C = "H": SDA (I^2C Bus)
11	CDTO	O	Control Data Output Pin in 4-wire serial control mode
12	TVDD2	-	Input / Output Buffer Power Supply 1 Pin, 1.6V~3.6V
13	VSS3		Ground Pin, 0V
14	DVDD	-	Digital Power Supply Pin, 1.6V~2.0V
15	NC	-	No Connection. No internal bonding. This pin must be connected to the ground.
16	TST2	I	Test Pin This pin must be connected to VSS4.
17	M/S	I	Master Mode Select Pin "L": Slave Mode "H": Master Mode
18	MCKO	O	Master Clock Output Pin
19	PDN	I	Power-Down & Reset Pin When "L", the AK4611 is powered-down and the control registers are reset to default state. If the state of CAD1-0 changes, then the AK4611 must be reset by PDN.
20	XTO	O	X'tal Output Pin
21	XTI	I	X'tal Input Pin
	MCKI	I	External Master Clock Input Pin
22	TVDD1	-	Input / Output Buffer Power Supply 1 Pin, 1.6V~3.6V
23	VSS4	-	Digital Ground Pin, 0V
24	SDTO1	O	Audio Serial Data Output 1 Pin
25	SDTO2	O	Audio Serial Data Output 2 Pin
26	TST6	O	Test Pin This pin must be open.
27	LRCK	I/O	Input /Output Channel Clock Pin
28	BICK	I/O	Audio Serial Data Clock Pin
29	SDTI1	I	Audio Serial Data Input 1 Pin
30	SDTI2	I	Audio Serial Data Input 2 Pin
31	SDTI3	I	Audio Serial Data Input 3 Pin
32	SDTI4	I	Audio Serial Data Input 4 Pin
33	TST7	I	Test Pin This pin must be connected to VSS4.

No.	Pin Name	I/O	Function
34	TST8	I	Test Pin This pin must be connected to VSS4.
35	DVMPD	I	DAC output VCOM voltage power down pin "L": DAC outputs are VCOM voltage "H": DAC outputs are Hi-Z.
36	LOUT1+	O	Lch Analog Positive Output 1 Pin (DOE1 bit = "H")
	LOUT1	O	Lch Analog Output 1 Pin (DOE1 bit = "L")
37	LOUT1-	O	Lch Analog Negative Output 1 Pin (When DOE1 bit = "L", this pin must be open.)
38	ROUT1+	O	Rch Analog Positive Output 1 Pin (DOE1 bit = "H")
	ROUT1	O	Rch Analog Output 1 Pin (DOE1 bit = "L")
39	ROUT1-	O	Rch Analog Negative Output 1 Pin (When DOE1 bit = "L", this pin must be open.)
40	LOUT2+	O	Lch Analog Positive Output 2 Pin (DOE2 bit = "H")
	LOUT2	O	Lch Analog Output 2 Pin (DOE2 bit = "L")
41	LOUT2-	O	Lch Analog Negative Output 2 Pin (When DOE2 bit = "L", this pin must be open.)
42	ROUT2+	O	Rch Analog Positive Output 2 Pin (DOE2 bit = "H")
	ROUT2	O	Rch Analog Output 2 Pin (DOE2 bit = "L")
43	ROUT2-	O	Rch Analog Negative Output 2 Pin (When DOE2 bit = "L", this pin must be open.)
44	LOUT3+	O	Lch Analog Positive Output 3 Pin (DOE3 bit = "H")
	LOUT3	O	Lch Analog Output 3 Pin (DOE3 bit = "L")
45	LOUT3-	O	Lch Analog Negative Output 3 Pin (When DOE3 bit = "L", this pin must be open.)
46	ROUT3+	O	Rch Analog Positive Output 3 Pin (DOE3 bit = "H")
	ROUT3	O	Rch Analog Output 3 Pin (DOE3 bit = "L")
47	ROUT3-	O	Rch Analog Negative Output 3 Pin (When DOE3 bit = "L", this pin must be open.)
48	VSS2	-	Ground Pin, 0V
49	AVDD2	-	Analog Power Supply Pin, 3.0V~3.6V
50	VREFH2	I	Positive Voltage Reference Input Pin, AVDD2
51	LOUT4+	O	Lch Analog Positive Output 4 Pin (DOE4 bit = "H")
	LOUT4	O	Lch Analog Output 4 Pin (DOE4 bit = "L")
52	LOUT4-	O	Lch Analog Negative Output 4 Pin (When DOE4 bit = "L", this pin must be open.)
53	ROUT4+	O	Rch Analog Positive Output 4 Pin (DOE4 bit = "H")
	ROUT4	O	Rch Analog Output 4 Pin (DOE4 bit = "L")
54	ROUT4-	O	Rch Analog Negative Output 4 Pin (When DOE4 bit = "L", this pin must be open.)
55	TST9	O	Test Pin This pin must be open.
56	TST10	O	Test Pin This pin must be open.
57	TST11	O	Test Pin This pin must be open.
58	TST12	O	Test Pin This pin must be open.
59	TST13	O	Test Pin This pin must be open.
60	TST14	O	Test Pin This pin must be open.
61	TST15	O	Test Pin This pin must be open.
62	TST16	O	Test Pin This pin must be open.
63	OVF1	O	Analog Input Overflow Detect 1 Pin (Note 1) This pin goes to "H" if the analog input of Lch or Rch overflows.
	DZF1	O	Zero Input Detect 1 Pin (Note 2) When the input data of the group 1 follow total 8192 LRCK cycles with "0" input data, this pin goes to "H". And when RSTN bit is "0", PMDAC bit is "0", this pin goes to "H".

No.	Pin Name	I/O	Function
64	OVF2	O	Analog Input Overflow Detect 2 Pin (Note 1) This pin goes to "H" if the analog input of Lch or Rch overflows.
	DZF2	O	Zero Input Detect 2 Pin (Note 2) When the input data of the group 2 follow total 8192 LRCK cycles with "0" input data, this pin goes to "H". And when RSTN bit is "0", PMDAC bit is "0", this pin goes to "H".
65	LIN1+	I	Lch Analog Positive Input 1 Pin (DIE1 bit = "H")
	LIN1	I	Lch Analog Input 1 Pin (DIE1 bit = "L")
66	LIN1-	-	Lch Analog Negative Input 1 Pin (When DIE1 bit = "L", this pin must be open.) (Note 3)
67	RIN1+	I	Rch Analog Positive Input 1 Pin (DIE1 bit = "H")
	RIN1	I	Rch Analog Input 1 Pin (DIE1 bit = "L")
68	RIN1-	-	Rch Analog Negative Input 1 Pin (When DIE1 bit = "L", this pin must be open.) (Note 3)
69	LIN2+	I	Lch Analog Positive Input 2 Pin (DIE2 bit = "H")
	LIN2	I	Lch Analog Input 2 Pin (DIE2 bit = "L")
70	LIN2-	-	Lch Analog Negative Input 2 Pin (When DIE2 bit = "L", this pin must be open.) (Note 3)
71	RIN2+	I	Rch Analog Positive Input 2 Pin (DIE2 bit = "H")
	RIN2	I	Rch Analog Input 2 Pin (DIE2 bit = "L")
72	RIN2-	-	Rch Analog Negative Input 2 Pin (When DIE2 bit = "L", this pin must be open.) (Note 3)
73	TST17	I	Test Pin This pin must be open.
74	TST18	I	Test Pin This pin must be open.
75	VSS1	-	Ground Pin, 0V
76	AVDD1	-	Analog Power Supply Pin, 3.0V~3.6V
77	VREFH1	I	Positive Voltage Reference Input Pin, AVDD1
78	VCOM	O	Common Voltage Output Pin, AVDD1x1/2 Large external capacitor around 2.2μF is used to reduce power-supply noise.
79	TST19	I	Test Pin This pin must be open.
80	TST20	I	Test Pin This pin must be open.

Note 1. This pin becomes OVF pin when OVFE bit is set to "1".
Note 2. This pin becomes DZF pin when OVFE bit is set to "0".
Note 3. This pin becomes analog negative input pin in differential input mode, and becomes output pin invert the positive input pin in single-end input mode. This pin must be open in single-end input mode.
Note 4. All digital input pins except for pull-down must not be left floating.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=VSS4=0V; Note 5)

Parameter			Symbol	min	max	Unit
Power Supplies	Analog		AVDD1,2	-0.3	4.2	V
	Digital		DVDD	-0.3	2.2	V
	Output buffer		TVDD1,2	-0.3	4.2	V
Input Current (any pins except for supplies)			IIN	-	±10	mA
Analog Input Voltage			VINA	-0.3	AVDD1,2+0.3	V
Digital Input Voltage (TST2,M/S,PDN,XTI/MCKI,LRCK,BICK, SDTI1,SDTI2,SDTI3,SDTI4,TST7,TST8, DVMPD pins)			VIND1	-0.3	TVDD1+0.3	V
(TST1,TST3,TST4,TST5,CAD0,CAD1,I2C, CCLK/SCL,CSN,CDTI/SDA pins)			VIND2	-0.3	TVDD2+0.3	V
Ambient Temperature (power applied)		AK4611EQ	Ta	-20	85	°C
		AK4611VQ	Ta	-40	105	°C
Storage Temperature			Tstg	-65	150	°C

Note 5. All voltages with respect to ground. VSS1, VSS2, VSS3 and VSS4 must be connected to the same analog ground plane. AVDD1 and AVDD2 must be the same voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=VSS4=0V; Note 5)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 6)	Analog	AVDD1,2	3.0	3.3	3.6	V
	Digital	DVDD	1.6	1.8	2.0	V
	I/O buffer 1 (Stereo Mode & Normal Speed Mode)	TVDD1	DVDD	3.3	3.6	V
	I/O buffer 1 (Except Stereo Mode & Normal Speed Mode)	TVDD1	3.0	3.3	3.6	V
	I/O buffer 2	TVDD2	DVDD	3.3	3.6	V

Note 6. The power up sequence between AVDD1, AVDD2, DVDD, TVDD1 and TVDD2 is not critical. Each power supplies should be powered up during the PDN pin = "L". The PDN pin should be "H" after all power supplies are powered up. All power supplies should be powered on, only a part of these power supplies cannot be powered off. (Power off means power supplies equal to ground or power supplies are floating.) Do not turn off only the AK4611 under the condition that a surrounding device is powered on and the I2C bus is in use.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD1=AVDD2=TVDD1=TVDD2=3.3V, DVDD =1.8V; VSS1=VSS2=0V; VREFH1=AVDD1, VREFH2=AVDD2; fs=48kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement Frequency=20Hz~20kHz at 48kHz, 20Hz~40kHz at fs=96kHz, 20Hz~40kHz at fs=192kHz; unless otherwise specified)

Parameter			min	typ	max	Unit
ADC Analog Input Characteristics (single inputs)						
Resolution					24	Bits
S/(N+D)	fs=48kHz BW=20kHz	-1dBFS	84	92		dB
		-60dBFS		40		
	fs=96kHz BW=40kHz	-1dBFS	83	91		dB
		-60dBFS		37		
	fs=192kHz BW=40kHz	-1dBFS		91		
		-60dBFS		37		
DR	(-60dBFS with A-weighted)		95	103		dB
S/N	(A-weighted)		95	103		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Gain Drift				40	-	ppm/°C
Input Voltage	AIN=0.65xVREFH1		1.94	2.15	2.37	Vpp
Input Resistance			7	9		kΩ
Power Supply Rejection		(Note 7)		50		dB
ADC Analog Input Characteristics (differential inputs)						
S/(N+D)	fs=48kHz BW=20kHz	-1dBFS	88	97		dB
		-60dBFS		40		dB
	fs=96kHz BW=40kHz	-1dBFS	86	94		
		-60dBFS		37		
	fs=192kHz BW=40kHz	-1dBFS		94		
		-60dBFS		37		
DR	(-60dBFS with A-weighted)		96	104		dB
S/N	(A-weighted)		96	104		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Gain Drift				40	-	ppm/°C
Input Voltage	AIN=0.65xVREFH1	(Note 8)	±1.94	±2.15	±2.37	Vpp
Input Resistance			11	13		kΩ
Power Supply Rejection		(Note 7)		50		dB
Common Mode Rejection Ratio (CMRR)		(Note 9)	74			dB
DAC Analog Output Characteristics (single outputs)						
Resolution					24	Bits
S/(N+D)	fs=48kHz BW=20kHz	0dBFS	84	94		dB
		-60dBFS		44		
	fs=96kHz BW=40kHz	0dBFS	86	92		
		-60dBFS		41		
	fs=192kHz BW=40kHz	0dBFS		92		
		-60dBFS		41		
DR	(-60dBFS with A-weighted)		97	105		dB
S/N	(A-weighted)		97	105		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Gain Drift				20	-	ppm/°C
Output Voltage	AOUT=0.63xVREFH2		1.87	2.08	2.29	Vpp
Load Resistance		(AC Load)	5			kΩ
Load Capacitance					30	pF
Power Supply Rejection		(Note 7)		50		dB

DAC Analog Output Characteristics (differential outputs)						
S/(N+D)	fs=48kHz BW=20kHz	0dBFS	90	100		dB
		-60dBFS		45		
	fs=96kHz BW=40kHz	0dBFS	88	98		
		-60dBFS		42		
	fs=192kHz BW=40kHz	0dBFS		98		
		-60dBFS		42		
DR (-60dBFS with A-weighted)			100	108		dB
S/N (A-weighted)			100	108		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0	0.5	dB
Gain Drift				20	-	ppm/°C
Output Voltage	AOUT=0.63xVREFH2 (Note 8)		±1.87	±2.08	±2.29	Vpp
Load Resistance (Note 10)			2			kΩ
Load Capacitance					30	pF
Power Supply Rejection (Note 7)				50		dB

Note 7. PSR is applied to AVDD1, AVDD2, DVDD, TVDD1 and TVDD2 with 1kHz, 50mVpp. VREFH1 and VREFH2 pins are held a constant voltage +3.3V.

Note 8. This value is (LIN+) – (LIN-) and (RIN+) – (RIN-). The voltage is proportional to VREFH1, VREFH2 voltage.

Note 9. VREFH1 and VREFH2 are held +3.3V, the input bias voltage is set to AVDD1, 2 x 0.5. The 1kHz, 0.96Vpp signal is applied to LIN- and LIN+ with same phase (e.g. shorted) or RIN- and RIN+. The CMRR is measured as the attenuation level from 0dB = -7dBFS (since the normal 0.96Vpp = -7dBFS). This value is guaranteed but not tested.

Note 10. For AC-load. In the case of DC-load is 5kΩ.

Note 11. This value is Load Capacitance for output pin to GND. In differential mode, this value should be estimated to be twice, because Load Capacitance exists to GND and between the differential pin.

Parameter		min	typ	max	Unit
Power Supplies					
Power Supply Current					
Normal Operation (PDN pin = "H")					
AVDD1+AVDD2	fs=48kHz, 96kHz, 192kHz		63.0	125.0	mA
DVDD	fs=48kHz		12.0	24.0	mA
	fs=96kHz		17.0	35.0	mA
	fs=192kHz		28.0	55.0	mA
TVDD1+TVDD2	fs=48kHz		6.0	8.0	mA
	fs=96kHz		7.0	9.5	mA
	fs=192kHz		7.0	9.5	mA
Power-down mode					
(PDN pin = "L", DVMPD = "L") (Note 12)					
AVDD1+AVDD2+DVDD+TVDD1+TVDD2			200	550	μA
(PDN pin = "L", DVMPD = "H") (Note 12)					
AVDD1+AVDD2+DVDD+TVDD1+TVDD2			10	200	μA

Note 12. In the power-down mode, all digital input pins including clock pins are held VSS3 (TST1, TST3, TST4, TST5, CAD0, CAD1, I2C, CSN, CCLK, CDTI pins), VSS4 (TST2, M/S, MCKI, LRCK, BICK, SDTI1, SDTI2, SDTI3, SDTI4,TST7, TST8).

FILTER CHARACTERISTICS (fs=48kHz)

(Ta= Tmin ~ Tmax; AVDD1=AVDD2=3.0~ 3.6V, DVDD=1.6~ 2.0V, TVDD1=TVDD2=1.6~ 3.6V; DEM=OFF)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 13)	±0.1dB	PB	0	-	18.9	kHz
	−0.2dB		-	20.0	-	kHz
	−3.0dB		-	23.0	-	kHz
Stopband (Note 13)		SB	28	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 14)		GD	-	16	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 13)	−3dB	FR	-	1.0	-	Hz
	−0.1dB		-	6.5	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 13)	±0.06dB	PB	0	-	21.8	kHz
	−6.0dB		-	24.0	-	kHz
Stopband (Note 13)		SB	26.2	-	-	kHz
Passband Ripple		PR	-	-	±0.06	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 14)		GD	-	22	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response (Note 15)	20kHz	FR	-	-0.1	-	dB

FILTER CHARACTERISTICS (fs=96kHz)

(Ta= Tmin ~ Tmax; AVDD1=AVDD2=3.0~ 3.6V, DVDD=1.6~ 2.0V, TVDD1=TVDD2=1.6~ 3.6V; DEM=OFF)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 13)	±0.1dB	PB	0	-	37.8	kHz
	−0.2dB		-	40.0	-	kHz
	−3.0dB		-	46.0	-	kHz
Stopband (Note 13)		SB	56	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 14)		GD	-	16	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 13)	−3dB	FR	-	2.0	-	Hz
	−0.1dB		-	13.0	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 13)	±0.06dB	PB	0	-	43.6	kHz
	−6.0dB		-	48.0	-	kHz
Stopband (Note 13)		SB	52.4	-	-	kHz
Passband Ripple		PR	-	-	±0.06	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 14)		GD	-	22	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response (Note 15)	40kHz	FR	-	-0.3	-	dB

FILTER CHARACTERISTICS (fs=192kHz)

(Ta= Tmin ~ Tmax; AVDD1=AVDD2=3.0~ 3.6V, DVDD=1.6~ 2.0V, TVDD1=TVDD2=1.6~ 3.6V; DEM=OFF)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 13)	±0.1dB	PB	0	-	56.6	kHz
	−0.2dB		-	57.0	-	kHz
	−3.0dB		-	90.3	-	kHz
Stopband (Note 13)		SB	112	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 14)		GD	-	16	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 13)	−3dB	FR	-	4.0	-	Hz
	−0.1dB		-	26.0	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 13)	±0.06dB	PB	0	-	87.0	kHz
	−6.0dB		-	96.0	-	kHz
Stopband (Note 13)		SB	104.9	-	-	kHz
Passband Ripple		PR	-	-	±0.06	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 14)		GD	-	22	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response (Note 15)	80kHz	FR	-	-1	-	dB

Note 13. The passband and stopband frequencies scale with fs (sampling frequency). For example, ADC: Passband (±0.1dB) = 0.39375 x fs (@ fs=48kHz), DAC: Passband (±0.06dB) = 0.45412 x fs.

Note 14. The calculated delay time is resulting from digital filtering. For the ADC, this time is from the input of an analog signal to the setting of 24bit data for both channels to the ADC output register. For the DAC, this time is from setting the 24 bit data both channels at the input register to the output of an analog signal.

Note 15. The reference frequency is 1kHz.

DC CHARACTERISTICS

(Ta= Tmin ~ Tmax; AVDD1=AVDD2=3.0~3.6; DVDD=1.6~2.0V; TVDD1=TVDD2=1.6~3.6V)

Parameter	Symbol	min	typ	max	Unit
TVDD1,TVDD2 ≤2.2V					
High-Level Input Voltage					
(TST2, M/S, PDN, MCKI, LRCK, BICK, SDTI1, SDTI2, SDTI3, SDTI4,TST7, TST8, DVMPD pins)	VIH	80%TVDD1	-	-	V
(TST1,TST3,TST4,TST5,CAD0,CAD1,I2C, CSN,CCLK, CDTI pins)	VIH	80%TVDD2	-	-	V
Low-Level Input Voltage					
(TST2, M/S, PDN, MCKI, LRCK, BICK, SDTI1, SDTI2, SDTI3, SDTI4,TST7, TST8, DVMPD pins)	VIL	-	-	20%TVDD1	V
(TST1,TST3,TST4,TST5,CAD0,CAD1,I2C, CSN,CCLK, CDTI pins)	VIL	-	-	20%TVDD2	V
TVDD1,TVDD2 > 2.2V					
High-Level Input Voltage					
(TST2, M/S, PDN, MCKI, LRCK, BICK, SDTI1, SDTI2, SDTI3, SDTI4,TST7, TST8, DVMPD pins)	VIH	70%TVDD1	-	-	V
(TST1,TST3,TST4,TST5,CAD0,CAD1,I2C, CSN,CCLK, CDTI pins)	VIH	70%TVDD2	-	-	V
Low-Level Input Voltage					
(TST2, M/S, PDN, MCKI, LRCK, BICK, SDTI1, SDTI2, SDTI3, SDTI4,TST7, TST8, DVMPD pins)	VIL	-	-	30%TVDD1	V
(TST1,TST3,TST4,TST5,CAD0,CAD1,I2C, CSN,CCLK, CDTI pins)	VIL	-	-	30%TVDD2	V
High-Level Output Voltage					
(SDTO1,SDTO2,TST6, LRCK, BICK, MCKO pins: Iout=-100μA)	VOH	TVDD1-0.5	-	-	V
(CDTO pin: Iout=-100μA)	VOH	TVDD2-0.5	-	-	V
(DZF1/OVF1, DZF2/OVF2 pins: Iout=-100μA)		AVDD2-0.5			V
Low-Level Output Voltage					
(SDTO1,SDTO2,TST6, LRCK, BICK, MCKO, CDTO, DZF1, DZF2/OVF pins: Iout= 100μA)	VOL	-	-	0.5	V
(SDA pin, 2.0V≤TVDD2≤3.6V Iout= 3mA)	VOL	-	-	0.4	V
(SDA pin, 1.6V≤TVDD2<2.0V Iout= 3mA)	VOL			20%TVDD2	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta= Tmin ~ Tmax; AVDD1=AVDD2=3.0~3.6; DVDD=1.6~2.0V; TVDD1=1.6~3.6V, TVDD2=1.6~3.6V; C_L=20pF; unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit
Master Clock Timing					
Crystal Resonator					
Frequency	fXTAL	11.2896		24.576	MHz
MCKO Output					
Frequency (TVDD1 ≥3.0V)	fMCK	5.6448		24.576	MHz
Duty	dMCK	40	50	60	%
External Clock					
256fsn:	fCLK	8.192		12.288	MHz
Pulse Width Low	tCLKL	32			ns
Pulse Width High	tCLKH	32			ns
384fsn:	fCLK	12.288		18.432	MHz
Pulse Width Low	tCLKL	22			ns
Pulse Width High	tCLKH	22			ns
512fsn, 256fsd, 128fsq:	fCLK	16.384		24.576	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
MCKO Output					
Frequency	fMCK	4.096		12.288	MHz
(TVDD1 ≥3.0V)	fMCK	12.288		24.576	MHz
Duty (Note 16)	dMCK	40	50	60	%
LRCK Timing (Slave mode)					
Stereo mode **(TDM1 bit = "0", TDM0 bit = "0")**					
Normal Speed Mode	fsn	32		48	kHz
Double Speed Mode	fsd	64		96	kHz
Quad Speed Mode	fsq	128		192	kHz
Duty Cycle	Duty	45		55	%
TDM512 mode (Note 17) **(TDM1 bit = "0", TDM0 bit = "1")**					
LRCK frequency	fsn	32		48	kHz
"H" time	tLRH	1/512fs			ns
"L" time	tLRL	1/512fs			ns
TDM256 mode (Note 18) **(TDM1 bit = "1", TDM0 bit = "0")**					
LRCK frequency	fsd	64		96	kHz
"H" time	tLRH	1/256fs			ns
"L" time	tLRL	1/256fs			ns
TDM128 mode (Note 19) **(TDM1 bit = "1", TDM0 bit = "1")**					
LRCK frequency	fsq	128		192	kHz
"H" time	tLRH	1/128fs			ns
"L" time	tLRL	1/128fs			ns

Parameter	Symbol	min	typ	max	Unit
LRCK Timing (Master Mode)					
Stereo mode					
(TDM1 bit = "0", TDM0 bit = "0")					
Normal Speed Mode	fsn	32		48	kHz
Double Speed Mode	fsd	64		96	kHz
Quad Speed Mode	fsq	128		192	kHz
Duty Cycle	Duty	-	50	-	%
TDM512 mode (Note 17)					
(TDM1 bit = "0", TDM0 bit = "1")					
LRCK frequency	fsn	32		48	kHz
"H" time (Note 20)	tLRH		1/16fs		ns
TDM256 mode (Note 18)					
(TDM1 bit = "1", TDM0 bit = "0")					
LRCK frequency	fsd	64		96	kHz
"H" time (Note 20)	tLRH		1/8fs		ns
TDM128 mode (Note 19)					
(TDM1 bit = "1", TDM0 bit = "1")					
LRCK frequency	fsq	128		192	kHz
"H" time (Note 20)	tLRH		1/4fs		ns

Note 16. Except the case of DIV bit = "0".
Note 17. Please use for Normal Speed mode. Master clock should be input the 512fs in Master mode.
Note 18. Please use for Double Speed mode.
Note 19. Please use for Quad Speed mode.
Note 20. If the format is I^2S, it is "L" time.

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing (Slave mode)					
Stereo mode (TDM1 bit = "0", TDM0 bit = "0")					
(TVDD1= 1.6V~3.6V)					
BICK Period	tBCK	324			ns
BICK Pulse Width Low	tBCKL	130			ns
Pulse Width High	tBCKH	130			ns
LRCK Edge to BICK "↑" (Note 21)	tLRB	20			ns
BICK "↑" to LRCK Edge (Note 21)	tBLR	20			ns
LRCK to SDTO(MSB) (Except I^{2}S mode)	tLRS			80	ns
BICK "↓" to SDTO	tBSD			80	ns
SDTI Hold Time	tSDH	50			ns
SDTI Setup Time	tSDS	50			ns
(TVDD1= 3.0V~3.6V)					
BICK Period	tBCK	81			ns
BICK Pulse Width Low	tBCKL	33			ns
Pulse Width High	tBCKH	33			ns
LRCK Edge to BICK "↑" (Note 21)	tLRB	23			ns
BICK "↑" to LRCK Edge (Note 21)	tBLR	23			ns
LRCK to SDTO(MSB) (Except I^{2}S mode)	tLRS			23	ns
BICK "↓" to SDTO	tBSD			23	ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
TDM512 mode (TDM1 bit = "0", TDM0 bit = "1")					
(TVDD1= 3.0V~3.6V) (Note 17)					ns
BICK Period	tBCK	40			ns
BICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
LRCK Edge to BICK "↑" (Note 21)	tLRB	10			ns
BICK "↑" to LRCK Edge (Note 21)	tBLR	10			ns
SDTO Setup time BICK "↑"	tBSS	6			ns
SDTO Hold time BICK "↑"	tBSH	5			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
TDM256 mode (TDM1 bit = "1", TDM0 bit = "0")					
(TVDD1= 3.0V~3.6V) (Note 18)					
BICK Period	tBCK	40			ns
BICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
LRCK Edge to BICK "↑" (Note 21)	tLRB	10			ns
BICK "↑" to LRCK Edge (Note 21)	tBLR	10			ns
SDTO Setup time BICK "↑"	tBSS	6			ns
SDTO Hold time BICK "↑"	tBSH	5			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
TDM128 mode (TDM1 bit = "1", TDM0 bit = "1")					
(TVDD1= 3.0V~3.6V) (Note 19)					
BICK Period	tBCK	40			ns
BICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
LRCK Edge to BICK "↑" (Note 21)	tLRB	10			ns
BICK "↑" to LRCK Edge (Note 21)	tBLR	10			ns
SDTO Setup time BICK "↑"	tBSS	6			ns
SDTO Hold time BICK "↑"	tBSH	5			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing (Master mode)					
Stereo mode (TDM1 bit = "0", TDM0 bit = "0")					
(TVDD1= 1.6V~3.6V)					
BICK Frequency	fBCK	-	64fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–40	-	40	ns
BICK "↓" to SDTO	tBSD	–70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
(TVDD1= 3.0V~3.6V)					
BICK Frequency	fBCK	-	64fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–23	-	23	ns
BICK "↓" to SDTO	tBSD	–23	-	23	ns
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns
TDM512 mode (TDM1 bit = "0", TDM0 bit = "1")					
(TVDD1= 3.0V~3.6V) (Note 17)					
BICK Frequency	fBCK	-	512fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	-10		10	ns
SDTO Setup time BICK "↑"	tBSS	6	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	-	ns
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns
TDM256 mode (TDM1 bit = "1", TDM0 bit = "0")					
(TVDD1= 3.0V~3.6V) (Note 18)					
BICK Frequency	fBCK	-	256fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–10	-	10	ns
SDTO Setup time BICK "↑"	tBSS	6	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	-	ns
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns
TDM128 mode (TDM1 bit = "1", TDM0 bit = "1")					
(TVDD1= 3.0V~3.6V) (Note 19)					
BICK Frequency	fBCK	-	128fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–10	-	10	ns
SDTO Setup time BICK "↑"	tBSS	6	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	-	ns
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns

Note 21. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Unit
Control Interface Timing (4-wire Serial mode):					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
CDTO Delay	tDCD			50	ns
CSN "↑" to CDTO Hi-Z	tCCZ			70	ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 22)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 23)	tPD	150			ns
PDN "↑" to SDTO valid (Note 24)	tPDV		518		1/fs

Note 22. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 23. The AK4611 can be reset by setting the PDN pin to "L" upon power-up.
Note 24. These cycles are the numbers of LRCK rising from the PDN pin rising.
Note 25. I^2C-bus is a trademark of NXP B.V.

■ Timing Diagram

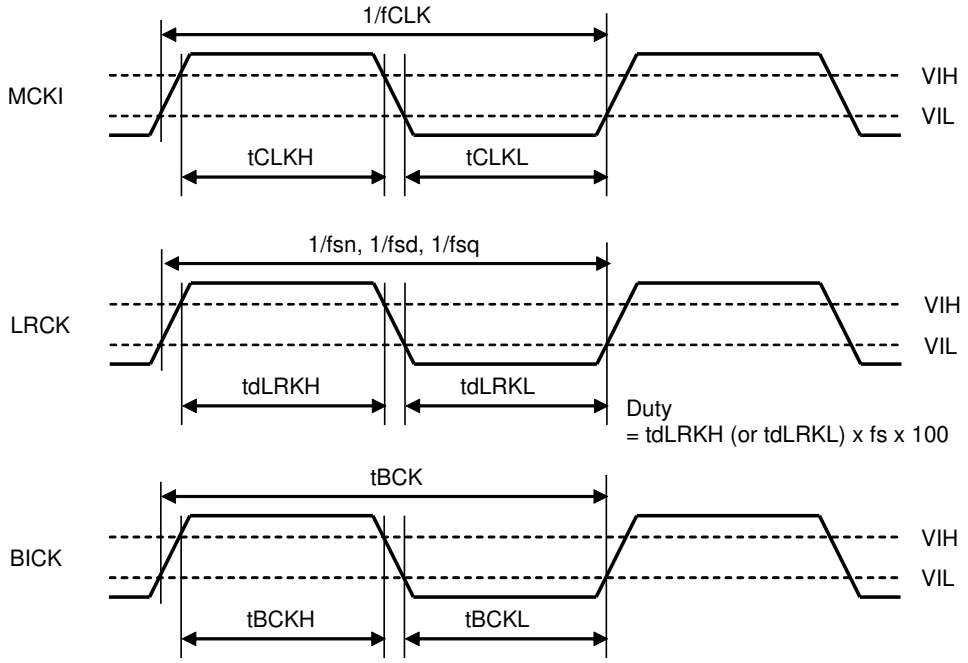


Figure 3. Clock Timing (TDM1/0 bit = "00" & Slave mode)

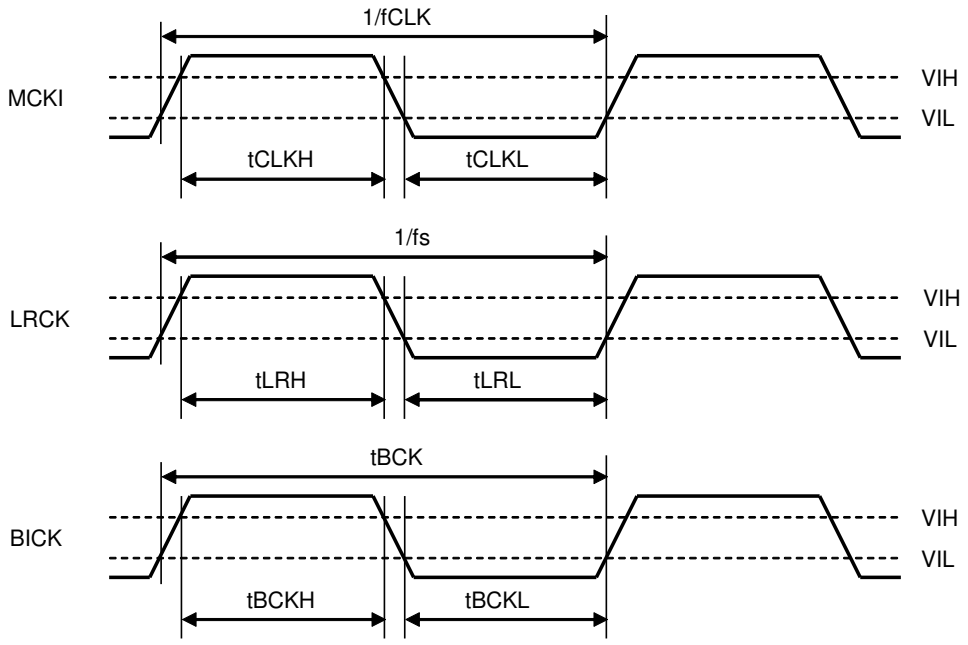


Figure 4. Clock Timing (Except TDM1/0 bit = "00" & Slave mode)

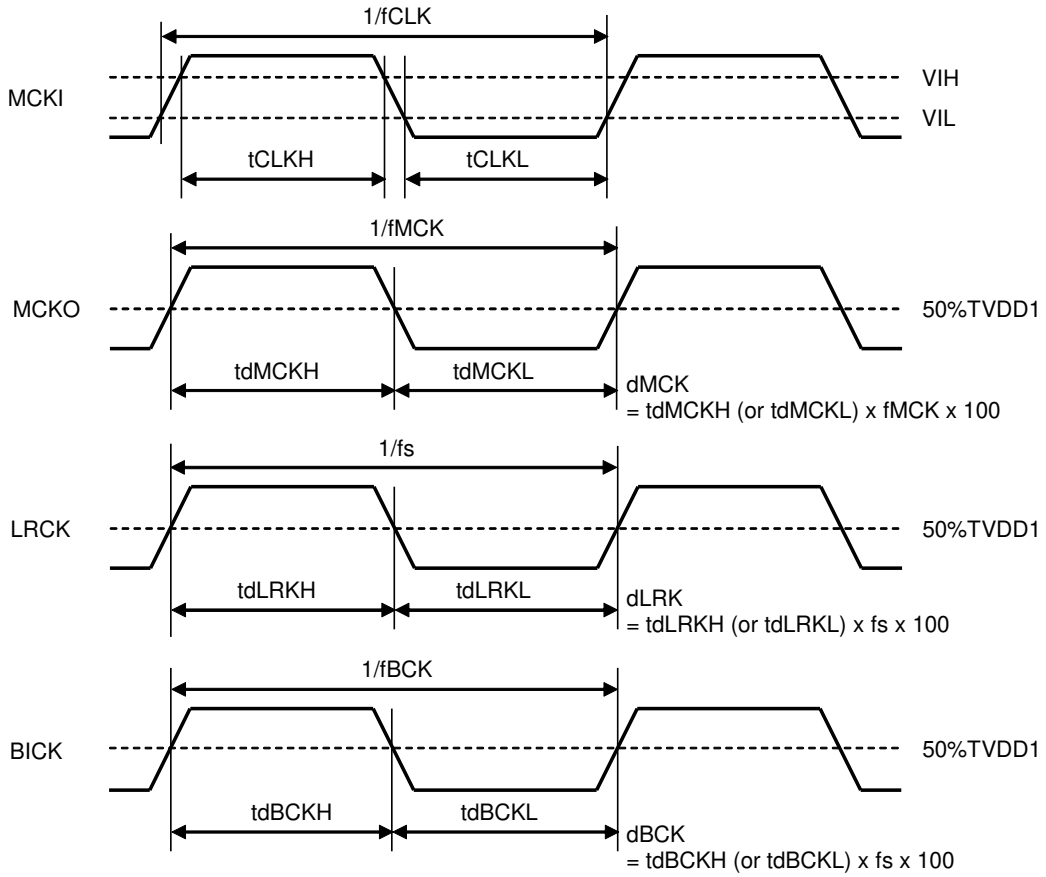


Figure 5. Clock Timing (TDM1/0 bit = "00" & Master mode)

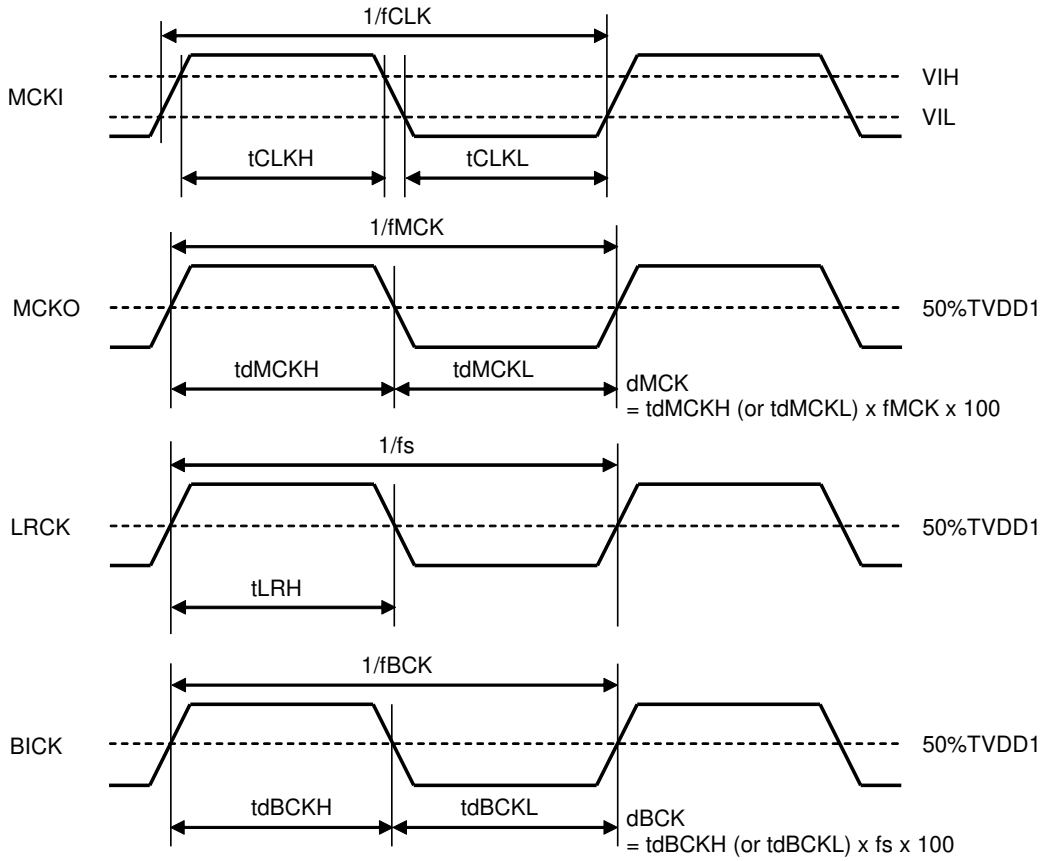


Figure 6. Clock Timing (Except TDM1/0 bit = "00" & Master mode)

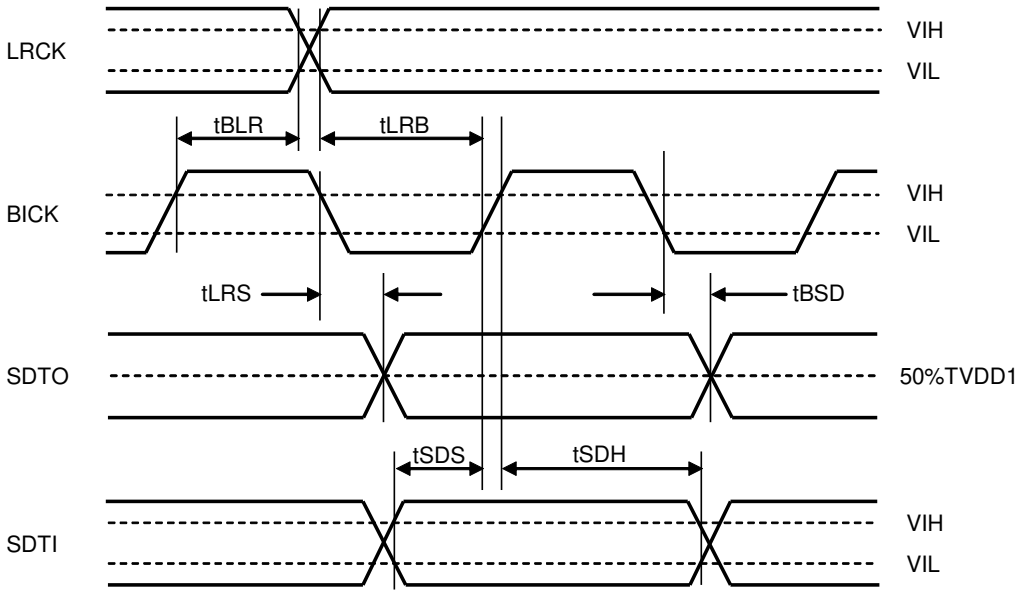


Figure 7. Audio Interface Timing (TDM1/0 bit = "00" & Slave mode)

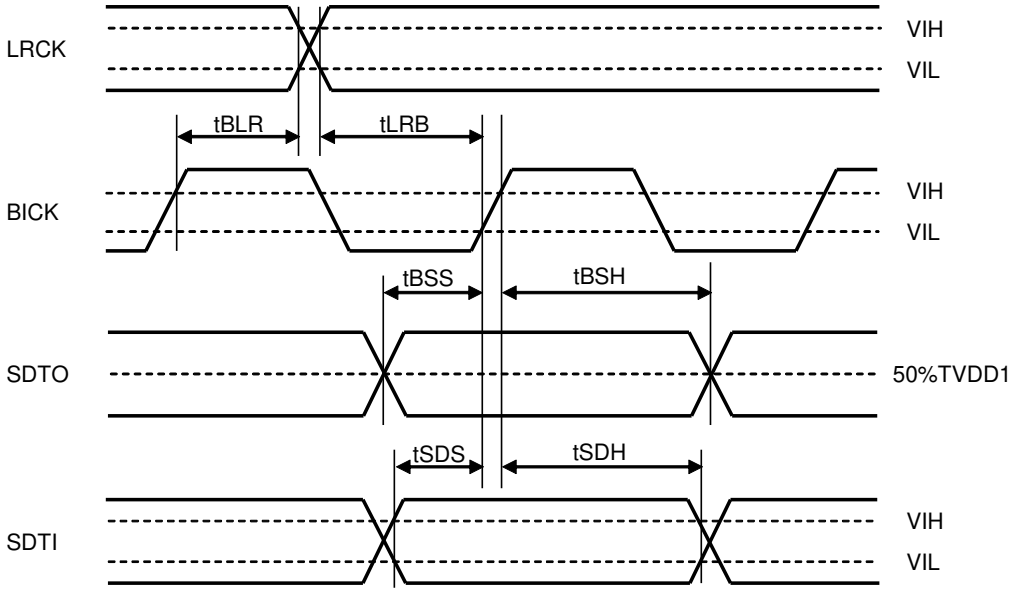


Figure 8. Audio Interface Timing (Except TDM1/0 bit = "00" & Slave mode)

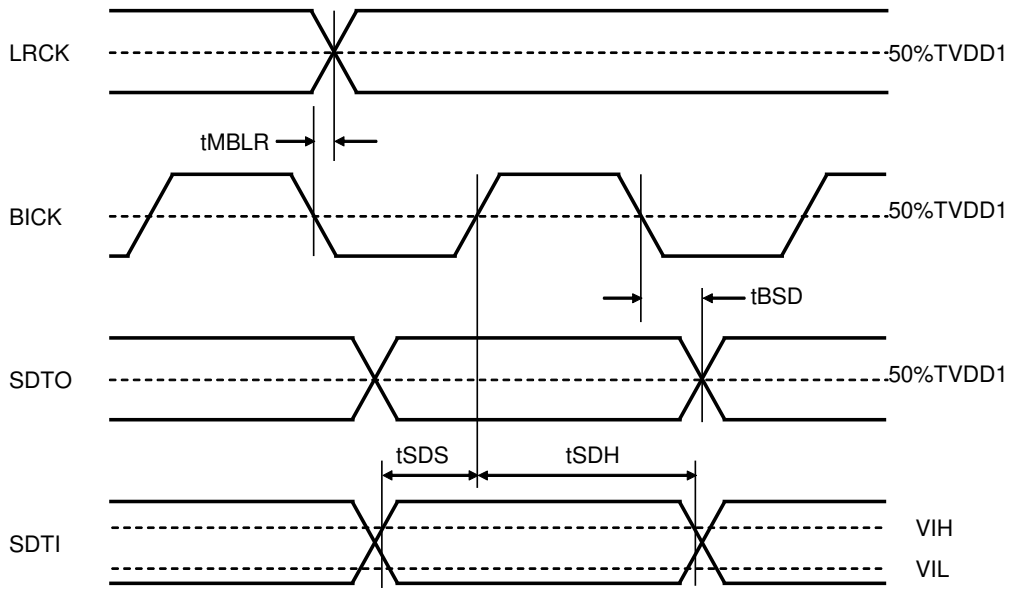


Figure 9. Audio Interface Timing (TDM1/0 bit = "00" & Master mode)

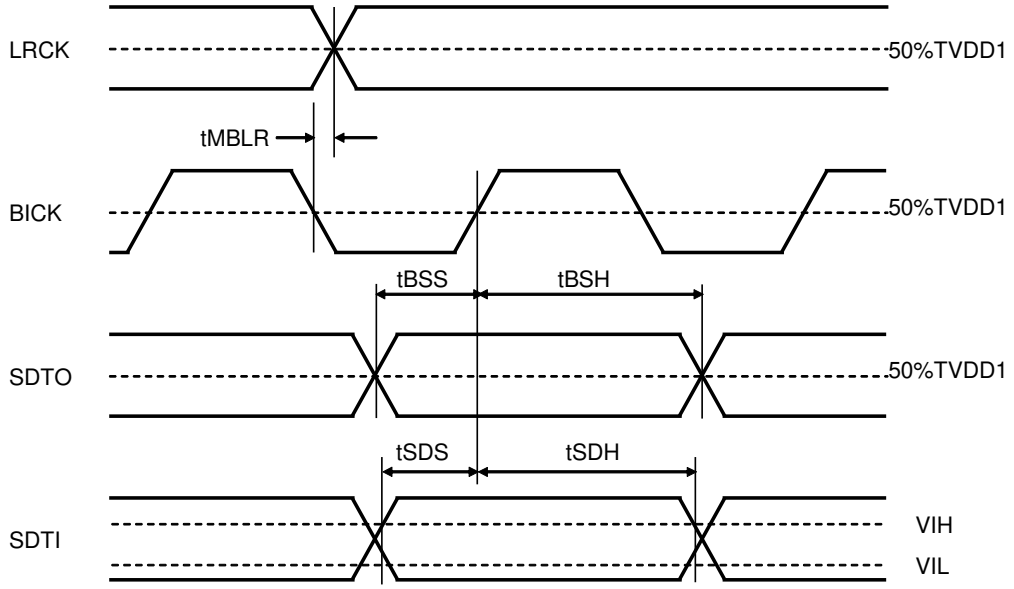


Figure 10. Audio Interface Timing (Except TDM1/0 bit = "00" & Master mode)

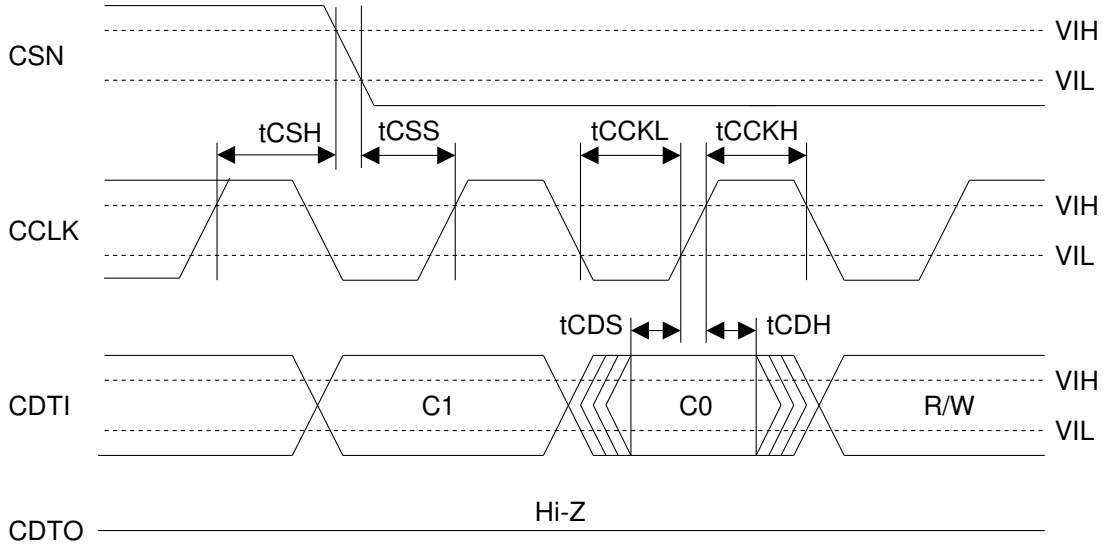


Figure 11. WRITE Command Input Timing (4-wire Serial mode)

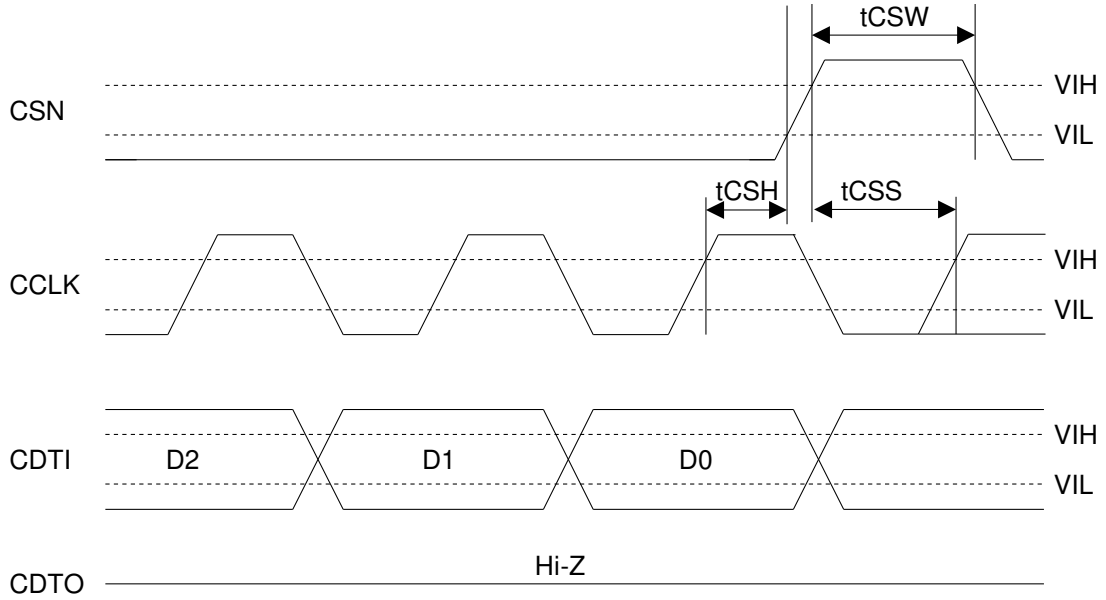


Figure 12. WRITE Data Input Timing (4-wire Serial mode)

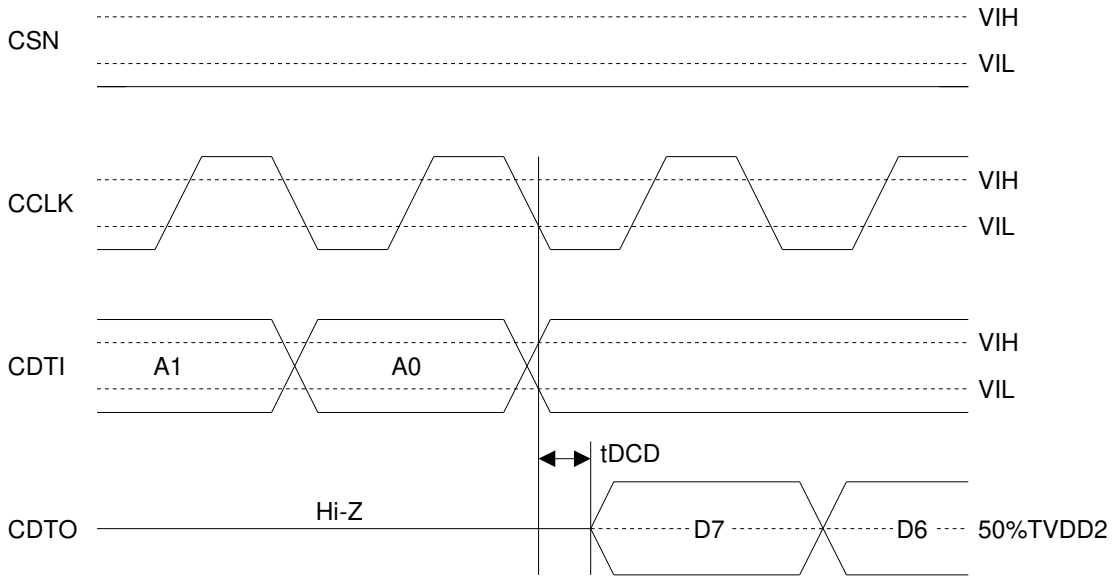


Figure 13. Read Data Output Timing1(4-wire Serial mode)

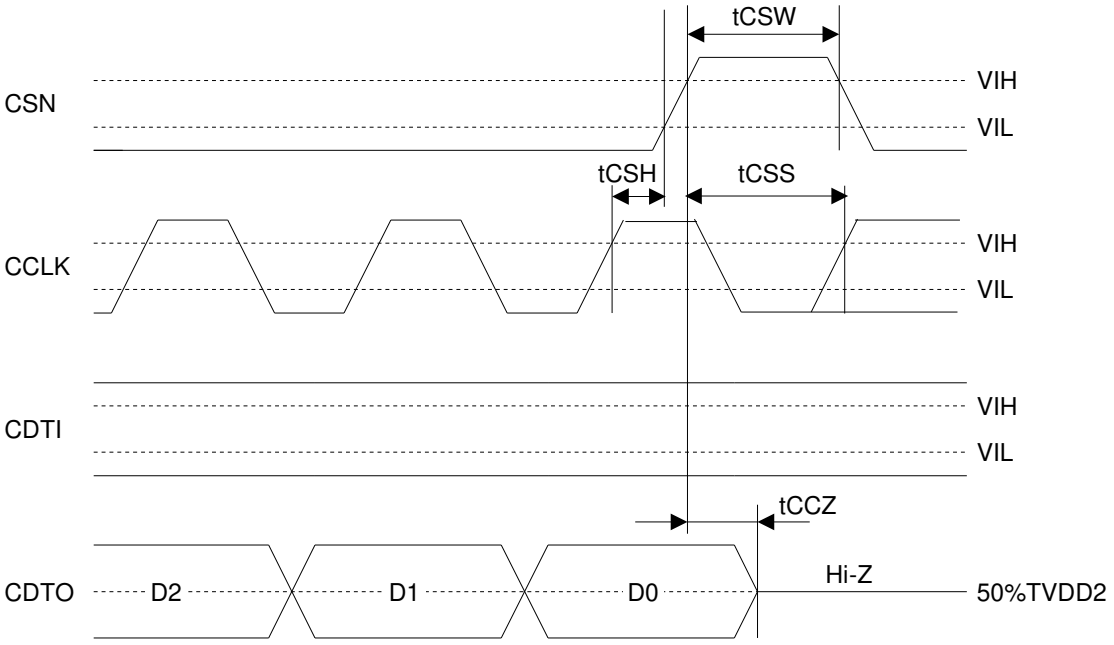


Figure 14. Read Data Output Timing2(4-wire Serial mode)

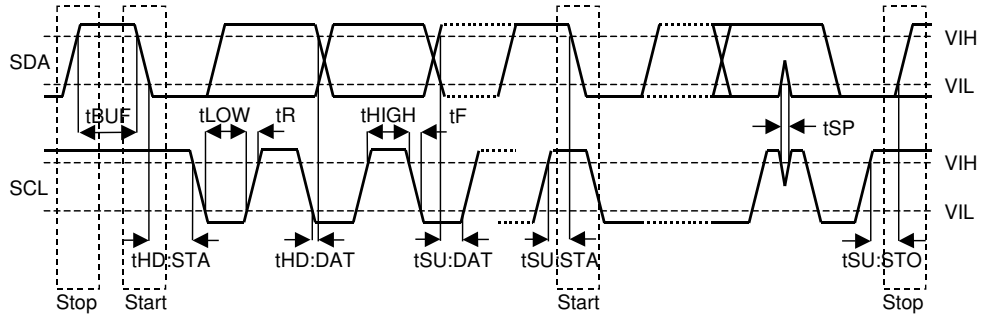


Figure 15. I^{2}C Bus mode Timing

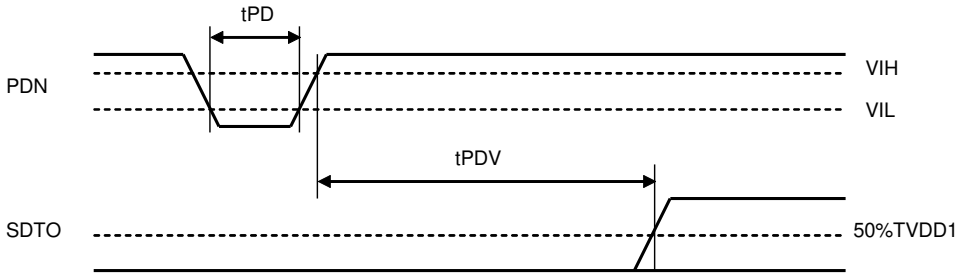


Figure 16. Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock

It is possible to select the clock source either extra clock input or X'tal input for the AK4611. (Figure 17, Figure 18) The external clocks which are required to operate the AK4611 in slave mode are MCLK, LRCK and BICK. MCLK should be synchronized with LRCK but the phase is not critical. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS bit= "0": Default), the sampling speed is set by DFS0, DFS1 (Table 1). The frequency of MCLK at each sampling speed is set automatically. (Table 3, Table 4, Table 5). In Auto Setting Mode (ACKS bit= "1"), as MCLK frequency is detected automatically (Table 6) and the internal master clock attains the appropriate frequency (Table 7), so it is not necessary to set DFS.

In master mode, only MCLK is required. Master Clock Input Frequency should be set with the CKS1-0 bits, and the sampling speed should be set by the DFS1-0 bits. The frequencies and the duties of the clocks (LRCK, BICK) are not stabile immediately after setting CKS1-0 bits and DFS1-0 bits up.

After exiting reset at power-up in slave mode, the AK4611 is in power-down mode until MCLK and LRCK are input.

If the clock is stopped, click noise occurs when restarting the clock. Mute the digital output externally if the click noise influences system applications.

DFS1	DFS0	Sampling Speed Mode (fs)		
0	0	Normal Speed Mode	32kHz~48kHz	(default)
0	1	Double Speed Mode	64kHz~96kHz	
1	0	Quad Speed Mode	128kHz~192kHz	
1	1	N/A	-	

(N/A: Not available)

Table 1. Sampling Speed (Manual Setting Mode)

CKS1	CKS0	Normal Speed Mode	Double Speed Mode	Quad Speed Mode	
0	0	256fs	256fs	128fs	
0	1	384fs	256fs	128fs	
1	0	512fs	256fs	128fs	(default)
1	1	512fs	256fs	128fs	

Table 2. Master Clock Input Frequency Select (Master Mode)

LRCK	MCLK (MHz)			BICK (MHz)
fs	256fs	384fs	512fs	64fs
32.0kHz	8.1920	12.2880	16.3840	2.0480
44.1kHz	11.2896	16.9344	22.5792	2.8224
48.0kHz	12.2880	18.4320	24.5760	3.0720

Table 3. System Clock Example (Normal Speed Mode @Manual Setting Mode)

LRCK	MCLK (MHz)	BICK (MHz)
fs	256fs	64fs
88.2kHz	22.5792	5.6448
96.0kHz	24.5760	6.1440

Table 4. System Clock Example (Double Speed Mode @Manual Setting Mode)

LRCK	MCLK (MHz)	BICK (MHz)
fs	128fs	64fs
176.4kHz	22.5792	11.2896
192.0kHz	24.5760	12.2880

Table 5. System Clock Example (Quad Speed Mode @Manual Setting Mode)

MCLK	Sampling Speed Mode
512fs	Normal Speed Mode
256fs	Double Speed Mode
128fs	Quad Speed Mode

Table 6. Sampling Speed (Auto Setting Mode)

LRCK	MCLK (MHz)			Sampling Speed Mode
fs	128fs	256fs	512fs	
32.0kHz	-	-	16.3840	Normal Speed Mode
44.1kHz	-	-	22.5792	
48.0kHz	-	-	24.5760	
88.2kHz	-	22.5792	-	Double Speed Mode
96.0kHz	-	24.5760	-	
176.4kHz	22.5792	-	-	Quad Speed Mode
192.0kHz	24.5760	-	-	

Table 7. System Clock Example (Auto Setting Mode)

■ Clock Source

The clock for the XTI pin can be generated by the two methods.

1) External clock

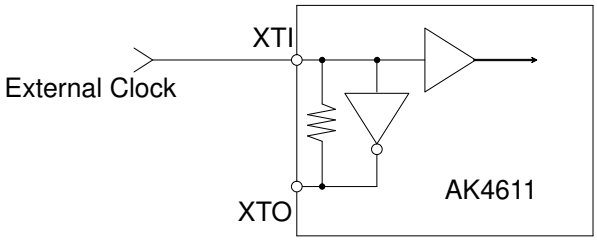


Figure 17. External clock mode

Note: Input clock must not exceed TVDD1.

2) X'tal

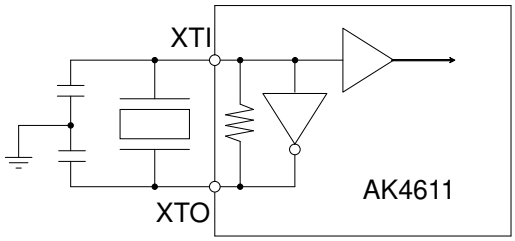


Figure 18. X'tal mode
Note: External capacitance depends on the crystal oscillator (Typ. 10pF)
TVDD1 should be used in the range of 3.0 ~ 3.6V in X'tal mode.

■ Differential / Single-End Input selection

The AK4611 supports the differential input (Figure 19) by setting DIE1-2 bits = "1", supports the single-end input (Figure 20) by setting DIE1-2 bits = "0". In differential input mode, two input pins must not be connected to a signal input in combination with a VCOM voltage. When single-end input mode, L/RIN1-/2- pins should be open, because L/RIN1-/2- pins output an invert signal of the input signal. The AK4611 includes an anti-aliasing filter (RC filter) for both differential input and the single-end input.

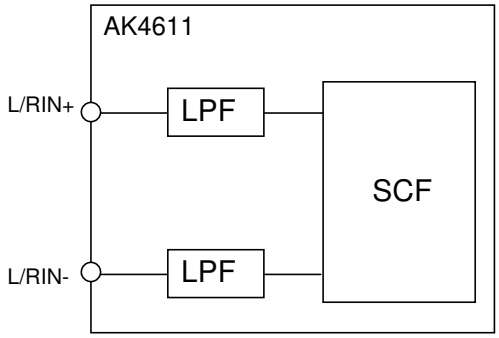


Figure 19. Differential Input (DIE1-2 bit = "1")

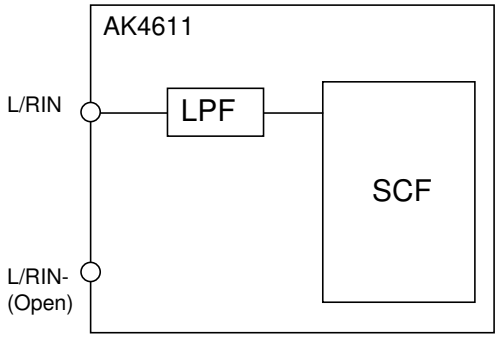


Figure 20. Single-end Input (DIE1-2 bit = "0")

■ Differential / Single-End Output selection

The AK4611 supports the differential output (Figure 21) by setting DOE1-4 bits = "1", and the single-end output (Figure 22) by setting DOE1-4 bits = "0". When single-end output mode, L/ROUT1-4 pins should be open, because of L/ROUT1-4 pins outputs VCOM voltage. The internal analog filters remove most of the noise beyond the audio passband generated by the delta-sigma modulator of a DAC in single-end input mode. There is no internal analog filter for differential output. Use external analog filters if needed to remove this noise.

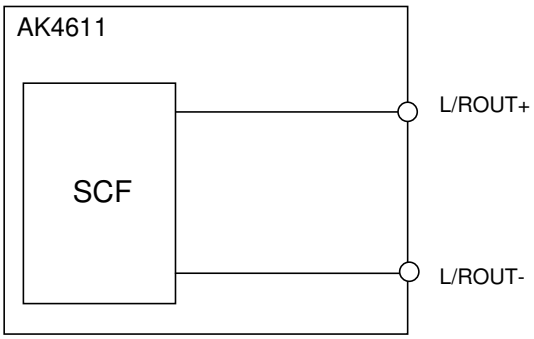


Figure 21. Differential Output (DOE1-4 bit = "1")

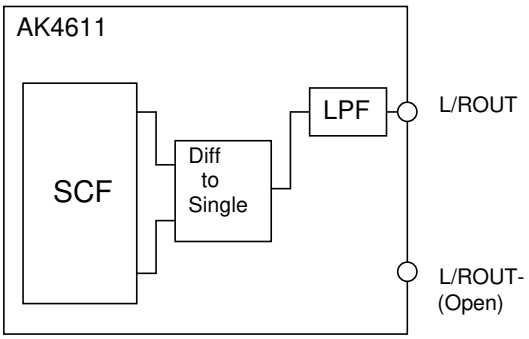


Figure 22. Single-end Output (DOE1-4 bit = "0")

■ De-emphasis Filter

The AK4611 has a digital de-emphasis filter (tc=50/15μs) by an IIR filter. The de-emphasis filter supports only Normal Speed Mode. This filter corresponds to three sampling frequencies (32kHz, 44.1kHz, 48kHz). De-emphasis of each DAC can be set individually by registers, DAC1(SDTI1), DAC2(SDTI2), DAC3(SDTI3), DAC4(SDTI4).

Mode	Sampling Speed Mode	DEM11 (DEM61-21)	DEM10 (DEM60-20)	DEM
0	Normal Speed Mode	0	0	44.1kHz
1	Normal Speed Mode	0	1	OFF
2	Normal Speed Mode	1	0	48kHz
3	Normal Speed Mode	1	1	32kHz

(default)

Table 8. De-emphasis control

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz at fs=48kHz and scales with the sampling rate (fs).

■ Master Clock Output

The AK4611 has a master clock output pin. If DIV bit = "1", the MCKO pin output the frequency divided in half.

DIV	MCKO
0	XTI x1
1	XTI x1/2

(default)

Table 9. The select of Master clock output frequency

■ Master Mode and Slave Mode

Master Mode and Slave Mode are selected by setting the M/S pin. (Master Mode= "H", Slave Mode= "L")
LRCK and BICK pins are outputs in Master Mode (M/S pin= "H")
LRCK and BICK pins are inputs in Slave Mode (M/S pin= "L")

PDN	M/S pin	LRCK pin	BICK pin
L	L	Input	Input
	H	"L" Output	"L" Output
H	L	Input	Input
	H	Output	Output

Table 10. LRCK and BICK pins

■ Audio Serial Interface Format

(1) Stereo Mode

When TDM1-0 bits = "00", ten modes can be selected by the DIF2-0 bits as shown in Table 11. In all modes the serial data is MSB-first, 2's compliment format. The data SDTO1-2 is clocked out on the falling edge of BICK and the SDTI1-4 is latched on the rising edge of BICK.

Mode3/4/8/9/13/14/18/19/23/24/28/29/33/34/38/39 in SDTI input formats can be used for 16-20bit data by zeroing the unused LSBs.

Mode	M/S	TDM1	TDM0	DIF2	DIF1	DIF0	SDTO1-2	SDTI1-4	LRCK		BICK		
										I/O		I/O	
0	0	0	0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	I	≥ 32fs	I	
1	0	0	0	0	0	1	24bit, Left justified	20bit, Right justified	H/L	I	≥ 48fs	I	
2	0	0	0	0	1	0	24bit, Left justified	24bit, Right justified	H/L	I	≥ 48fs	I	
3	0	0	0	0	1	1	24bit, Left justified	24bit, Left justified	H/L	I	≥ 48fs	I	
4	0	0	0	1	0	0	24bit, I^2S	24bit, I^2S	L/H	I	≥ 48fs	I	(default)
5	1	0	0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
6	1	0	0	0	0	1	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
7	1	0	0	0	1	0	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
8	1	0	0	0	1	1	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	
9	1	0	0	1	0	0	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	

Table 11. Audio data formats (Stereo mode)

Note. TVDD1 which is the Power of I/O buffer should be kept in the range of 1.6V~3.6V at Normal Speed Mode in Stereo Mode. TVDD1 should be kept in the range of 3.0V~3.6V at Double Speed Mode and Quad Speed Mode.

(2) TDM Mode

The audio serial interface format is set in TDM mode by the TDM1-0 bits = "01". Five modes can be selected by the DIF2-0 bits as shown in Table 12. In all modes the serial data is MSB-first, 2's compliment format. The SDTO1 is clocked out on the rising edge of BICK and the SDTI1/2/3 are latched on the rising edge of BICK. In the TDM512 mode (fs = 48kHz), the serial data of all ADC (four channels) is output to the SDTO1 pin. SDTO2 pin = "L". And the serial data of all DAC (eight channels) is input to the SDTI1 pin. The input data to SDTI2-4 pins are ignored. BICK should be fixed to 512fs. "H" time and "L" time of LRCK should be 1/512fs at least.
TDM256 mode can be set by TDM1-0 bits as show in Table 13. In the TDM256 mode (fs = 96kHz), the serial data of all ADC (four channels) is output to the SDTO1 pin. SDTO2 pin = "L". And the serial data of DAC (eight channels; L1, R1, L2, R2, L3, R3, L4, R4) is input to the SDTI1 pin. The input data to SDTI2-4 pins are ignored. BICK should be fixed to 256fs. "H" time and "L" time of LRCK should be 1/256fs at least. TDM128 mode can be set by TDM1-0 bits as show in Table 14.
In TDM128 mode (fs=192kHz), the serial data of four ADC (four channels; L1, R1, L2, R2) is output to the SDTO1 pin. The SDTO2 pin = "L". And the serial data of DAC (four channels; L1, R1, L2, R2) is input to the SDTI1 pin and the serial data of DAC (four channels; L3, R3, L4, R4) is input to the SDTI2 pin. The input data to SDTI3-4 pins are ignored. BICK should be fixed to 128fs. "H" time and "L" time of LRCK should be 1/128fs at least.

Mode	M/S	TDM1	TDM0	DIF2	DIF1	DIF0	SDTO1-2	SDTI1-4	LRCK		BICK	
										I/O		I/O
10	0	0	1	0	0	0	24bit, Left justified	16bit, Right justified	↑	I	512fs	I
11	0	0	1	0	0	1	24bit, Left justified	20bit, Right justified	↑	I	512fs	I
12	0	0	1	0	1	0	24bit, Left justified	24bit, Right justified	↑	I	512fs	I
13	0	0	1	0	1	1	24bit, Left justified	24bit, Left justified	↑	I	512fs	I
14	0	0	1	1	0	0	24bit, I^2S	24bit, I^2S	↓	I	512fs	I
15	1	0	1	0	0	0	24bit, Left justified	16bit, Right justified	↑	O	512fs	O
16	1	0	1	0	0	1	24bit, Left justified	20bit, Right justified	↑	O	512fs	O
17	1	0	1	0	1	0	24bit, Left justified	24bit, Right justified	↑	O	512fs	O
18	1	0	1	0	1	1	24bit, Left justified	24bit, Left justified	↑	O	512fs	O
19	1	0	1	1	0	0	24bit, I^2S	24bit, I^2S	↓	O	512fs	O

Table 12. Audio data formats (TDM512 mode)

Mode	M/S	TDM1	TDM0	DIF2	DIF1	DIF0	SDTO1-2	SDTI1-4	LRCK		BICK	
										I/O		I/O
20	0	1	0	0	0	0	24bit, Left justified	16bit, Right justified	↑	I	256fs	I
21	0	1	0	0	0	1	24bit, Left justified	20bit, Right justified	↑	I	256fs	I
22	0	1	0	0	1	0	24bit, Left justified	24bit, Right justified	↑	I	256fs	I
23	0	1	0	0	1	1	24bit, Left justified	24bit, Left justified	↑	I	256fs	I
24	0	1	0	1	0	0	24bit, I^2S	24bit, I^2S	↓	I	256fs	I
25	1	1	0	0	0	0	24bit, Left justified	16bit, Right justified	↑	O	256fs	O
26	1	1	0	0	0	1	24bit, Left justified	20bit, Right justified	↑	O	256fs	O
27	1	1	0	0	1	0	24bit, Left justified	24bit, Right justified	↑	O	256fs	O
28	1	1	0	0	1	1	24bit, Left justified	24bit, Left justified	↑	O	256fs	O
29	1	1	0	1	0	0	24bit, I^2S	24bit, I^2S	↓	O	256fs	O

Table 13. Audio data formats (TDM256 mode)

Mode	M/S	TDM1	TDM0	DIF2	DIF1	DIF0	SDTO1-2	SDTI1-4	LRCK		BICK	
										I/O		I/O
30	0	1	1	0	0	0	24bit, Left justified	16bit, Right justified	↑	I	128fs	I
31	0	1	1	0	0	1	24bit, Left justified	20bit, Right justified	↑	I	128fs	I
32	0	1	1	0	1	0	24bit, Left justified	24bit, Right justified	↑	I	128fs	I
33	0	1	1	0	1	1	24bit, Left justified	24bit, Left justified	↑	I	128fs	I
34	0	1	1	1	0	0	24bit, I^2S	24bit, I^2S	↓	I	128fs	I
35	1	1	1	0	0	0	24bit, Left justified	16bit, Right justified	↑	O	128fs	O
36	1	1	1	0	0	1	24bit, Left justified	20bit, Right justified	↑	O	128fs	O
37	1	1	1	0	1	0	24bit, Left justified	24bit, Right justified	↑	O	128fs	O
38	1	1	1	0	1	1	24bit, Left justified	24bit, Left justified	↑	O	128fs	O
39	1	1	1	1	0	0	24bit, I^2S	24bit, I^2S	↓	O	128fs	O

Table 14. Audio data formats (TDM128 mode)

Note. TVDD1 should be used in the range of 3.0V~3.6V in TDM mode.

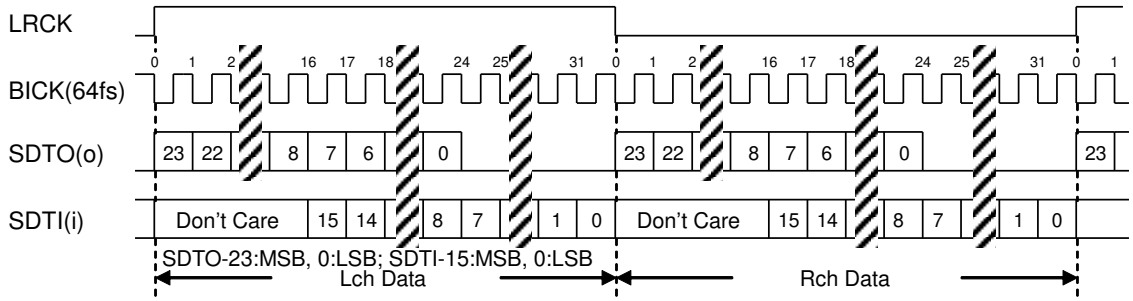


Figure 23. Mode 0/5 Timing (Stereo Mode)

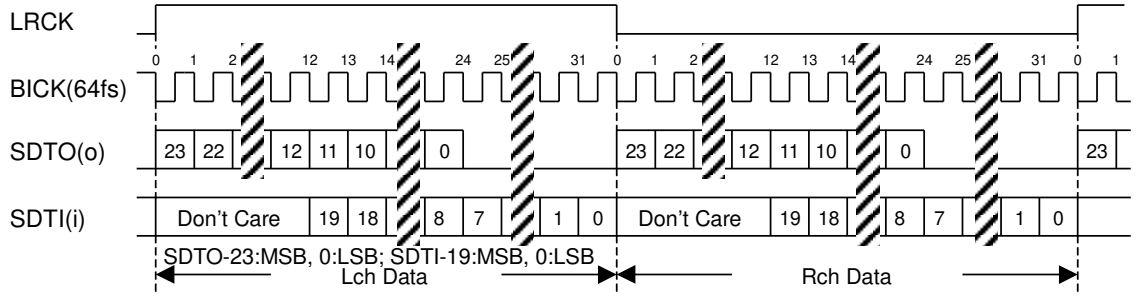


Figure 24. Mode 1/6 Timing (Stereo Mode)

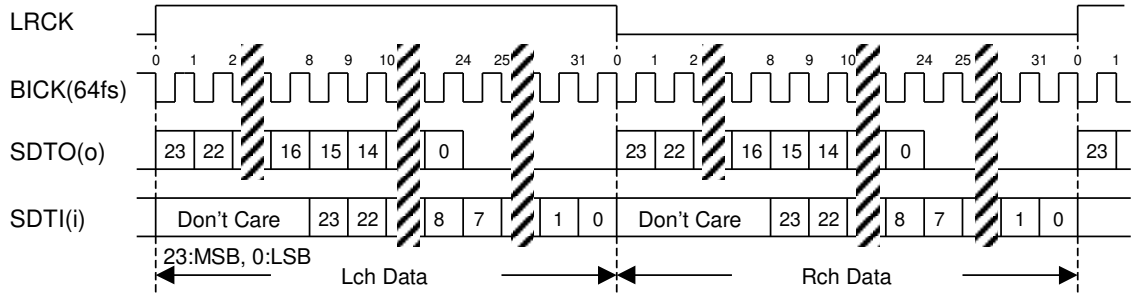


Figure 25. Mode 2/7 Timing (Stereo Mode)

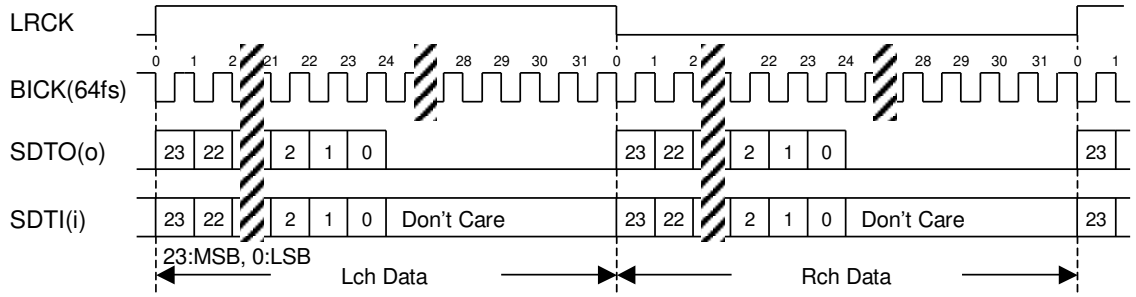


Figure 26. Mode 3/8 Timing (Stereo Mode)

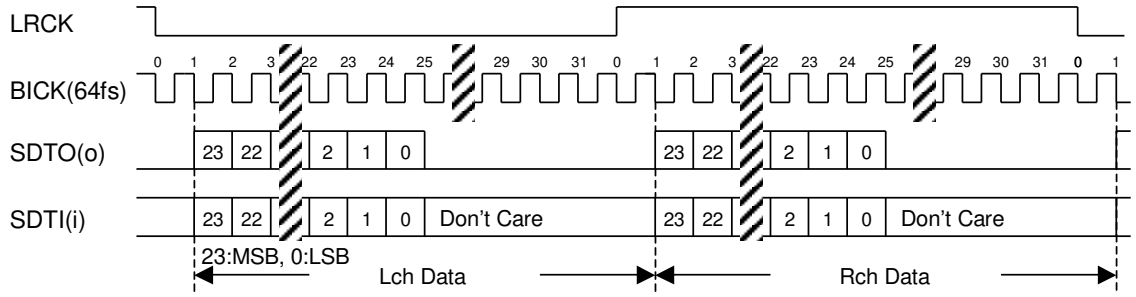


Figure 27. Mode 4/9 Timing (Stereo Mode)

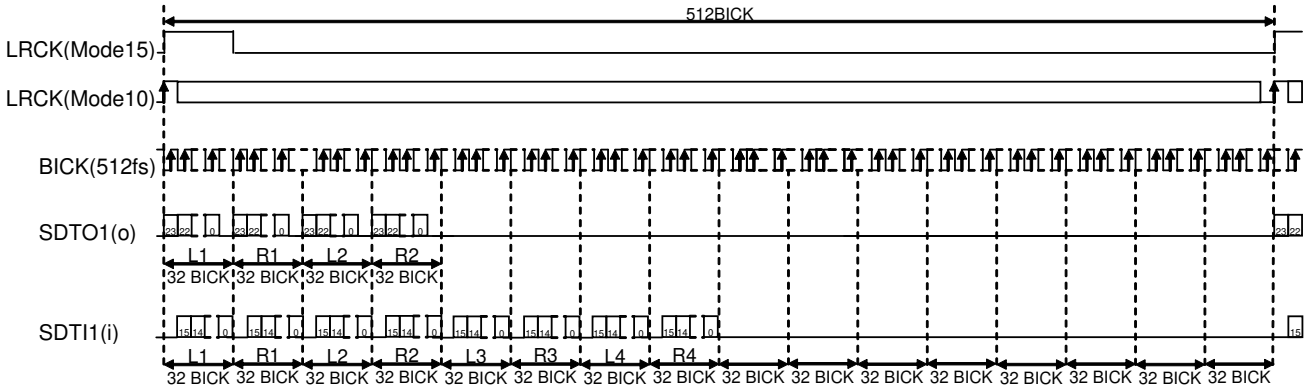


Figure 28. Mode 10/15 Timing (TDM512 Mode)

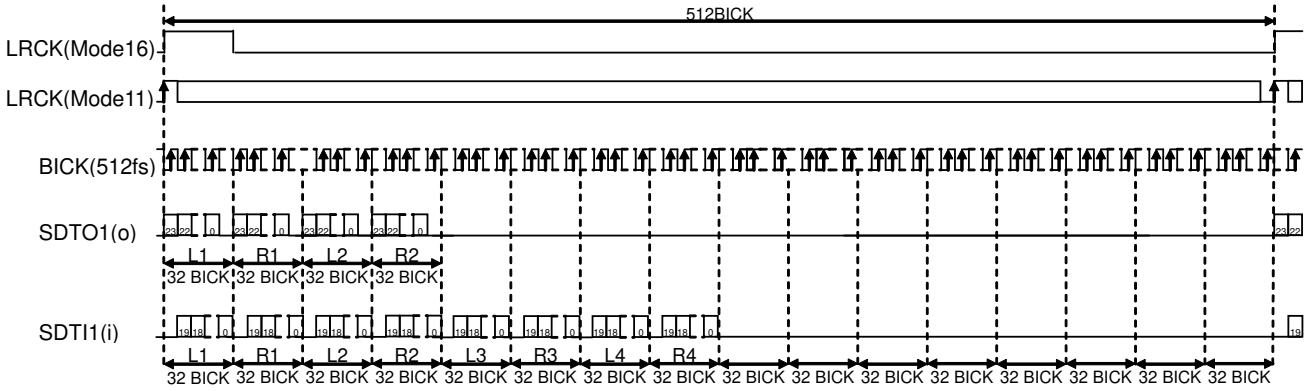


Figure 29. Mode 11/16 Timing (TDM512 Mode)

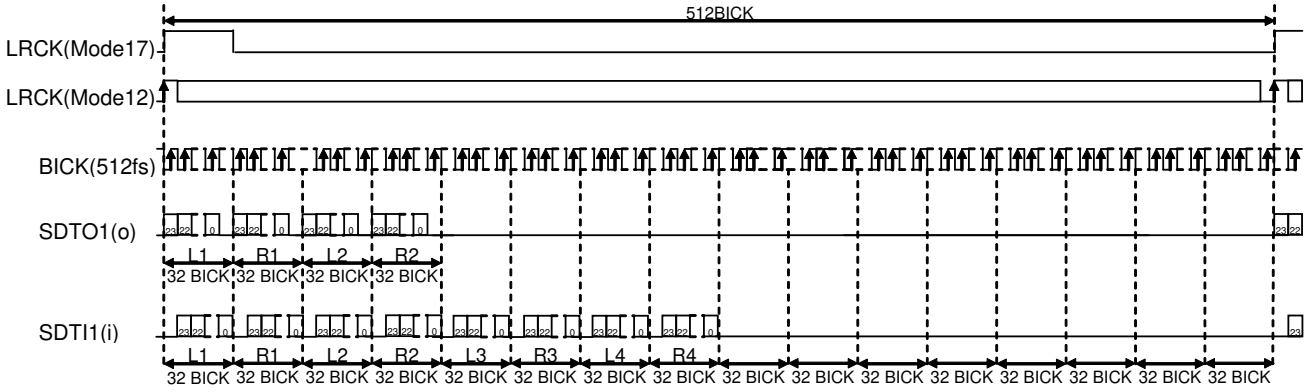


Figure 30. Mode 12/17 Timing (TDM512 Mode)

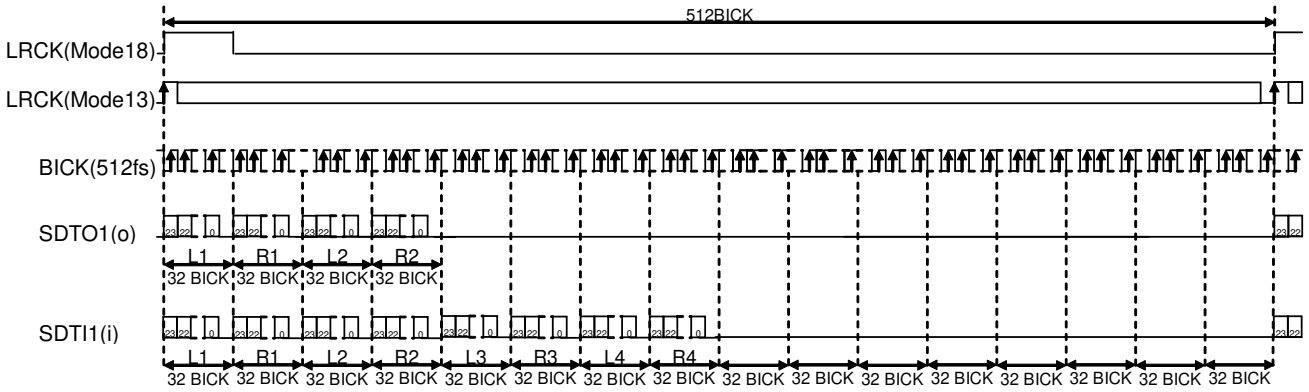


Figure 31. Mode 13/18 Timing (TDM512 Mode)

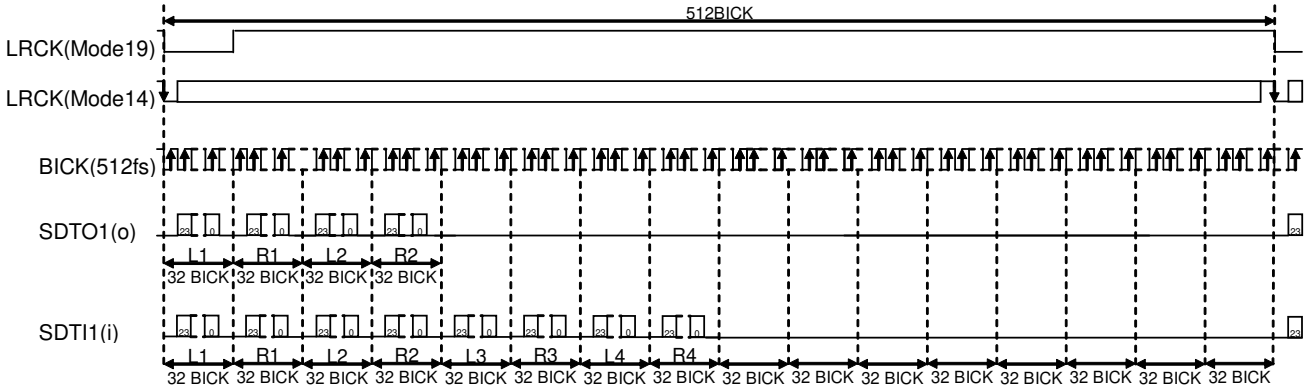


Figure 32. Mode 14/19 Timing (TDM512 Mode)

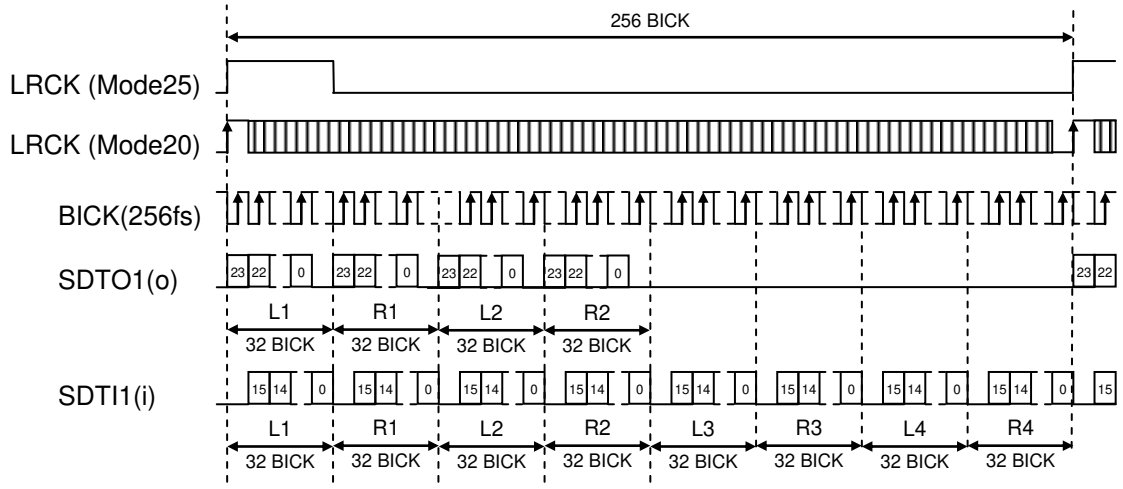


Figure 33. Mode 20/25 Timing (TDM256 Mode)

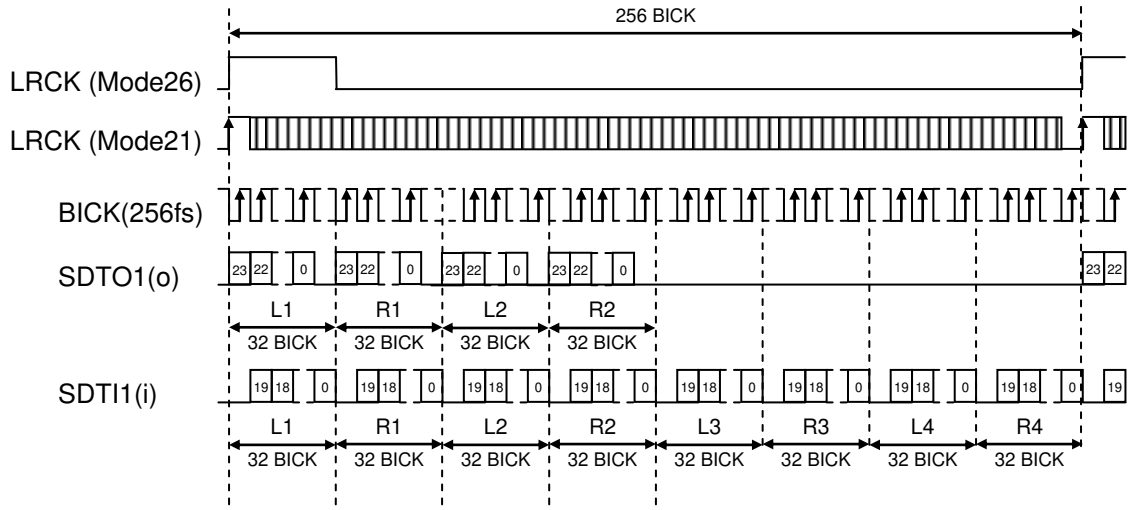


Figure 34. Mode 21/26 Timing (TDM256 Mode)

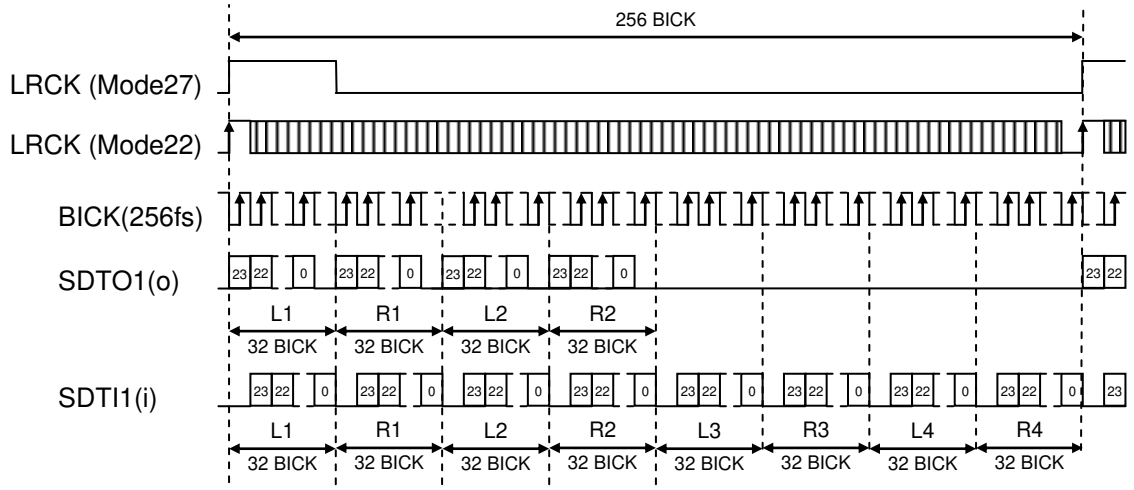


Figure 35. Mode 22/27 Timing (TDM256 Mode)

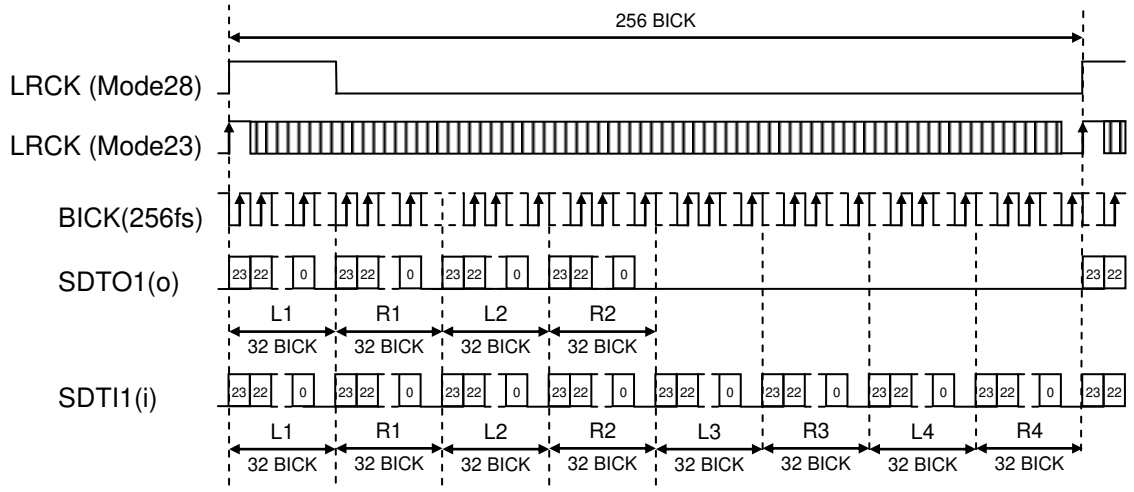


Figure 36. Mode 23/28 Timing (TDM256 Mode)

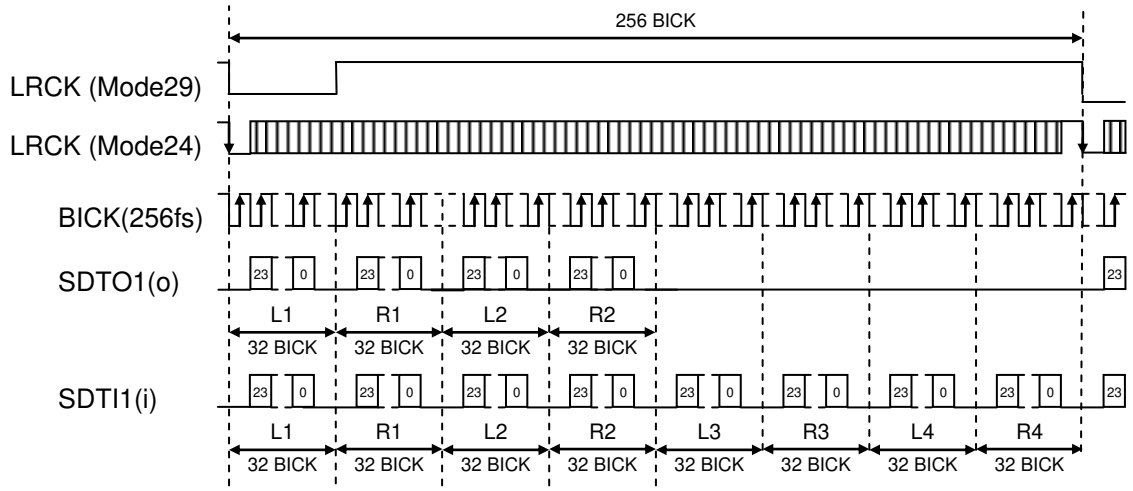


Figure 37. Mode 24/29 Timing (TDM256 Mode)

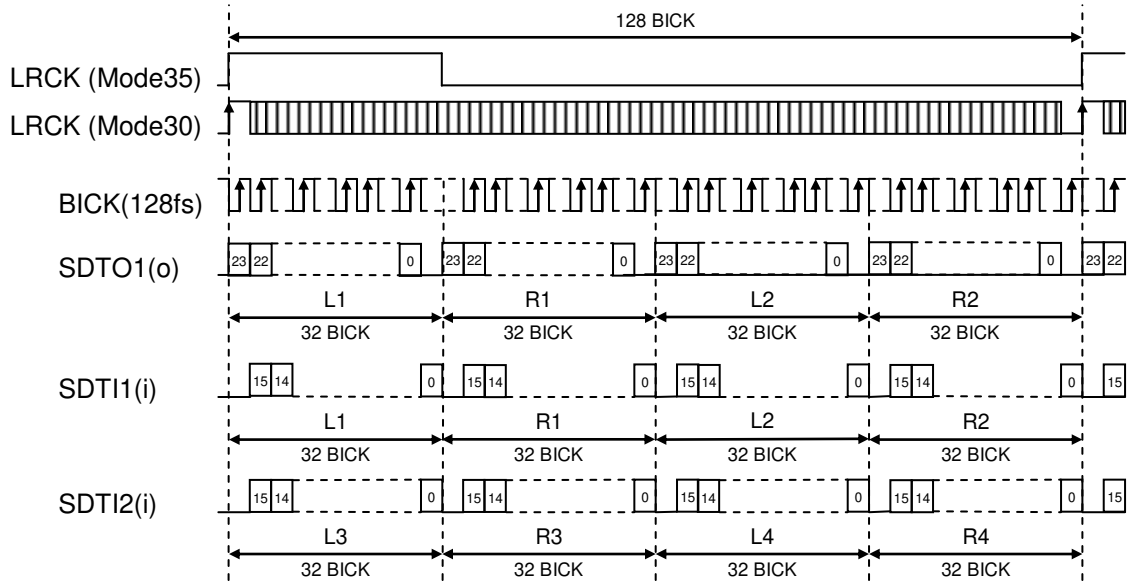


Figure 38. Mode 30/35 Timing (TDM128 Mode)

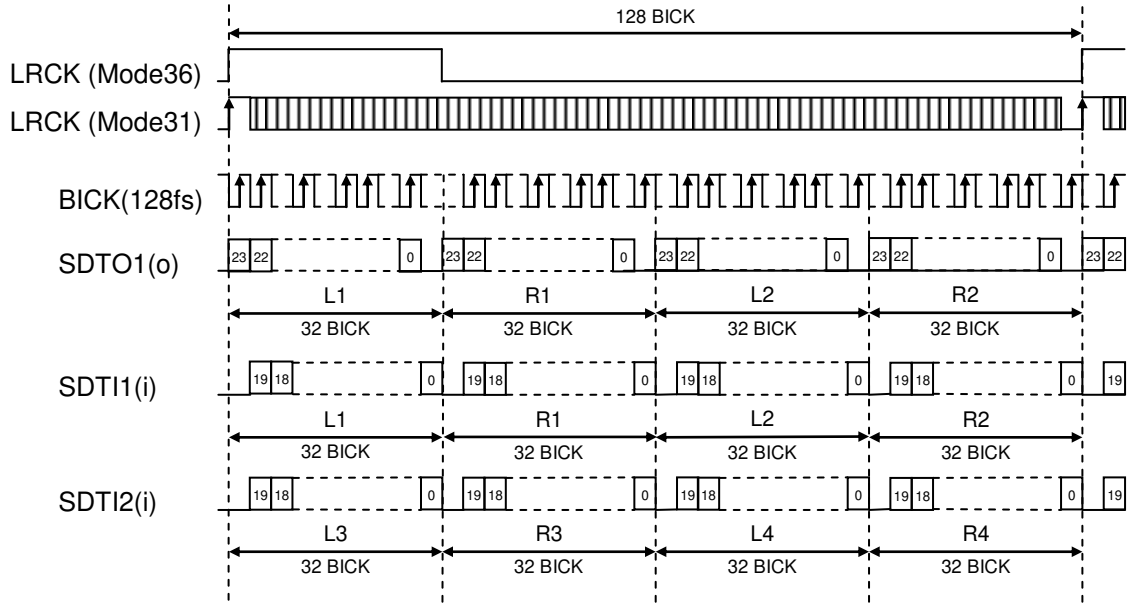


Figure 39. Mode 31/36 Timing (TDM128 Mode)

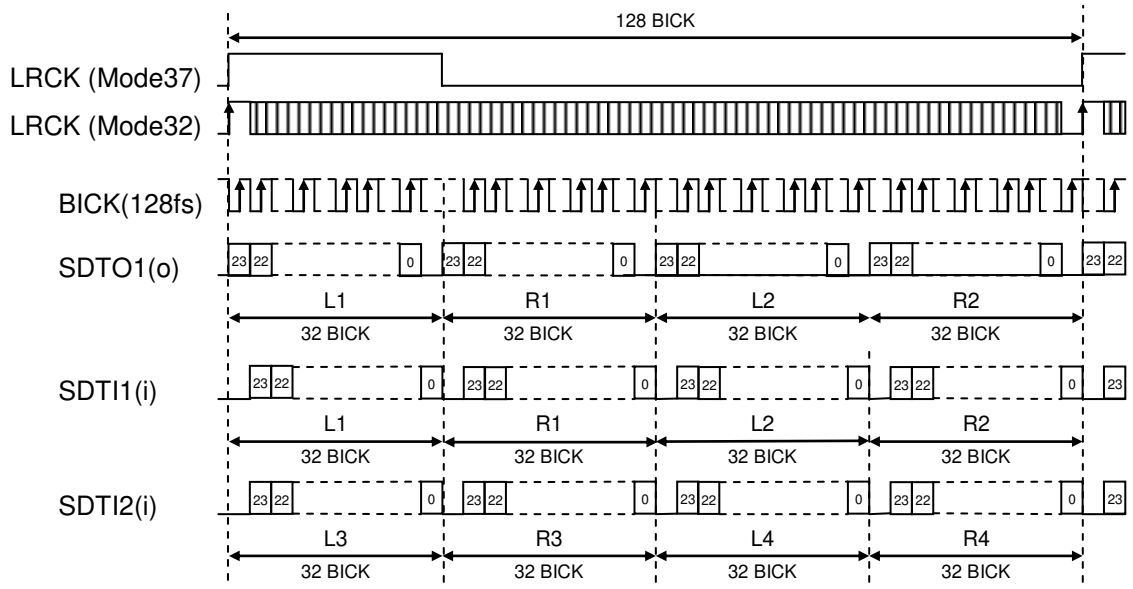


Figure 40. Mode 32/37 Timing (TDM128 Mode)

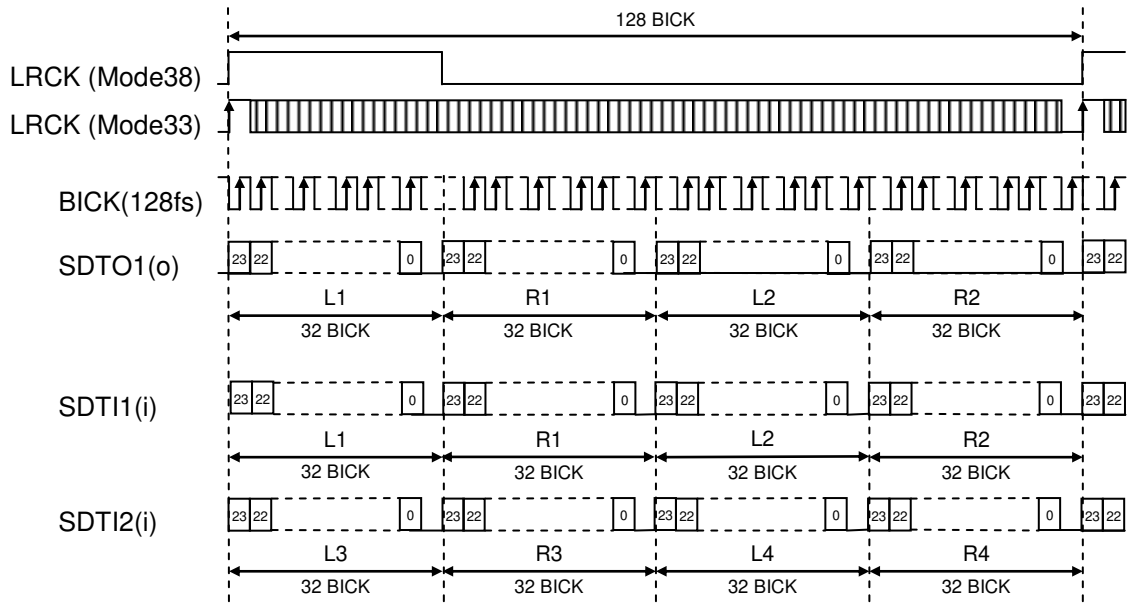


Figure 41. Mode 33/38 Timing (TDM128 Mode)

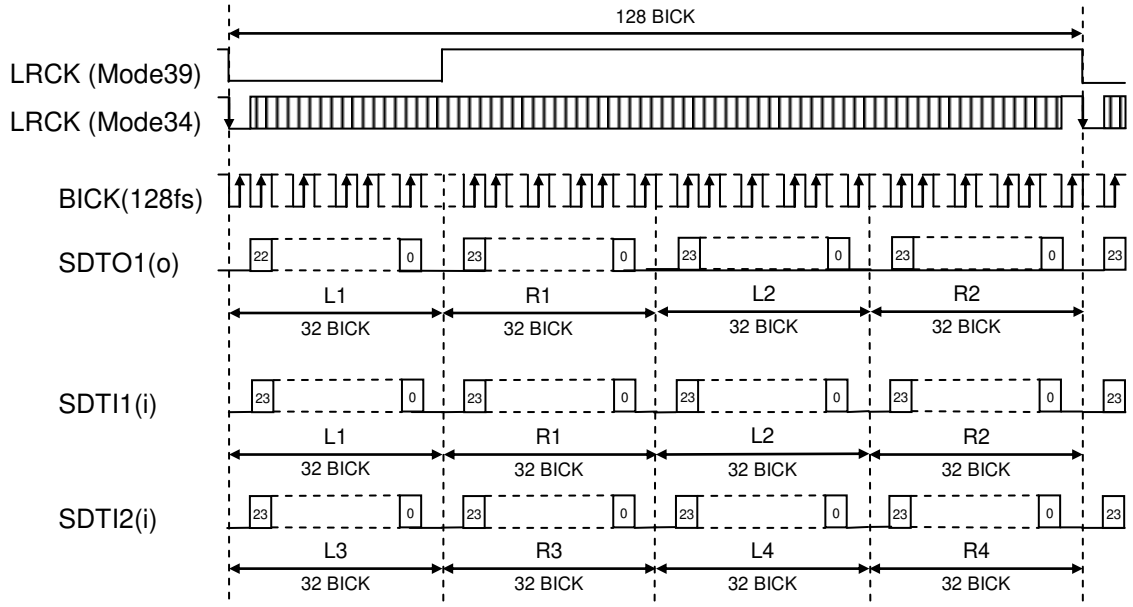


Figure 42. Mode 34/39 Timing (TDM128 Mode)

■ Overflow Detection

The AK4611 has an overflow detect function for the analog input. The overflow detect function is enabled when the OVFE bit is set to "1". Overflow detection is applied to the analog input of each channel, and the result is OR'd. OVF1/2 pins goes to "H" according to the group set by OVFM2-0 bits, if analog input of Lch or Rch overflows (more than -0.3dBFS). When the analog input is overflowed, the output signal of OVF1/2 pins have the same group delay as ADC (GD = 16/fs = 333μs @fs=48kHz). OVF1/2 pins are "L" for 518/fs (=11.8ms @fs=48kHz) after PDN = "↑", and then overflow detection is enabled.

Mode	OVFM2	OVFM1	OVFM0	LIN1 or RIN1	LIN2 or RIN2
0	0	0	0	OVF1	OVF1
1	0	0	1	OVF1	OVF2
2	0	1	0	-	OVF1
3	0	1	1	OVF2	-
4	1	0	0	OVF2	OVF2
5	1	0	1	disable (OVF2=OVF1= "L")	
6	1	1	0		
7	1	1	1		

(default)

Table 15. Overflow detect control (OVFE bit = "1")

■ Zero Detection

The AK4611 has two pins for zero detect flag outputs. Zero detect function is enabled when the OVFE bit is set to "0". Channel grouping can be selected by the DZFM3-0 bits. (Table 16) The DZF1 pin corresponds to the group 1 channels and the DZF2 pin corresponds to the group 2 channels. DZF1 is AND operation of all eight channels and DZF2 is disabled ("L") at mode 0, "H" at mode 1-3. When the input data of all channels in the group 1(group 2) are continuously zeros for 8192 LRCK cycles, the DZF1 (DZF2) pin goes to "H". The DZF1 (DZF2) pin immediately returns to "L" if input data of any channels in the group 1(group 2) is not zero.

Mode	DZFM				AOUT							
	3	2	1	0	L1	R1	L2	R2	L3	R3	L4	R4
0	0	0	0	0	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1
1	0	0	0	1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1
2	0	0	1	0	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1
3	0	0	1	1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1
4	0	1	0	0	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1
5	0	1	0	1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF2
6	0	1	1	0	DZF1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF2	DZF2
7	0	1	1	1	DZF1	DZF1	DZF1	DZF1	DZF1	DZF2	DZF2	DZF2
8	1	0	0	0	DZF1	DZF1	DZF1	DZF1	DZF2	DZF2	DZF2	DZF2
9	1	0	0	1	DZF1	DZF1	DZF1	DZF2	DZF2	DZF2	DZF2	DZF2
10	1	0	1	0	DZF1	DZF1	DZF2	DZF2	DZF2	DZF2	DZF2	DZF2
11	1	0	1	1	DZF1	DZF2	DZF2	DZF2	DZF2	DZF2	DZF2	DZF2
12	1	1	0	0	DZF2	DZF2	DZF2	DZF2	DZF2	DZF2	DZF2	DZF2
13	1	1	0	1	disable (DZF1=DZF2= "L")							
14	1	1	1	0								
15	1	1	1	1								

(default)

Table 16. Zero detect control (OVFE bit = "0")

■ Digital Attenuator

AK4611 has a channel-independent digital attenuator (256 levels, 0.5dB steps). Attenuation level of each channel can be set by each the ATT7-0 bits (Table 17).

ATT7-0	Attenuation Level	
00H	0dB	(default)
01H	-0.5dB	
02H	-1.0dB	
:	:	
7DH	-62.5dB	
7EH	-63.0dB	
7FH	-63.5dB	
	:	
FEH	-127.0dB	
FFH	MUTE (-∞)	

Table 17. Attenuation level of digital attenuator

Transition time between set values of ATT7-0 bits can be selected by the ATS1-0 bits (Table 18). Transition between set values is the soft transition in Mode1/2/3 eliminating switching noise in the transition.

Mode	ATS1	ATS0	ATT speed	
0	0	0	4096/fs	(default)
1	0	1	2048/fs	
2	1	0	512/fs	
3	1	1	256/fs	

Table 18. Transition time between set values of ATT7-0 bits

The transition between set values is a soft transition of 4096 levels in mode 0. It takes 4096/fs (85.3ms@fs=48kHz) from 00H(0dB) to FFH(MUTE). If the PDN pin goes to "L", the ATTs are initialized to 00H. The ATTs also become 00H when RSTN bit = "0", and fade to their current value when RSTN bit returns to "1".

* A power-down release command must be write again (dummy write) after 5 LRCK cycles or later form the first command when releasing power-down mode by PMVR, PMDAC, RSTN, PMDA1, PMDA2, PMDA3 or PMDA4 bit in I2C mode. If this dummy write is not executed, DATT output will keep the initial value (0dB) until the next write is executed.

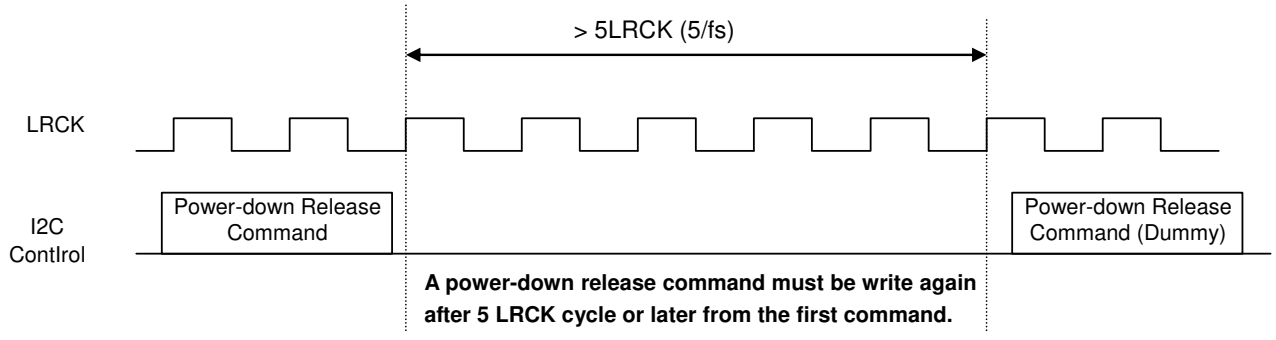
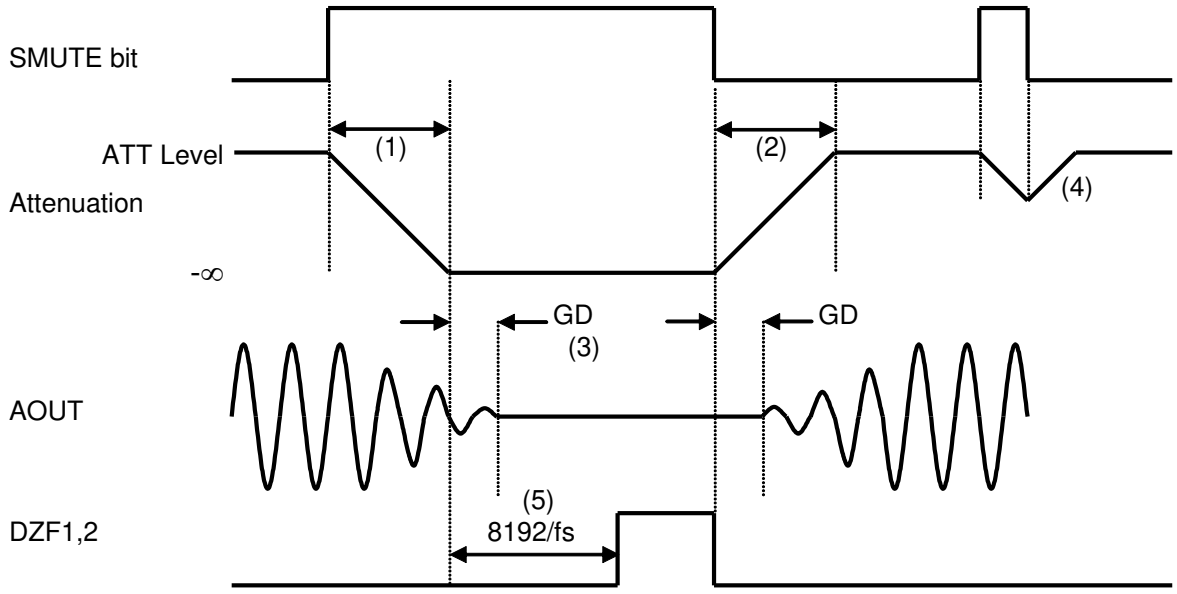


Figure 43. Power-up Sequence Example

■ Soft Mute Operation

Soft mute operation is performed in the digital domain. When the SMUTE bit becomes "1", the output signal is attenuated to -∞ in the cycle set by ATS bits (Table 18) from the current ATT level. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level in the cycle set by ATS bits. If the soft mute is cancelled before attenuating to -∞ after starting the operation, attenuation is discontinued and it is returned to ATT level by the same cycle. Soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) The time for input data attenuation to -∞ (Table 18). For example, in Normal Speed Mode, this time is 4096LRCK cycles (4096/fs) at ATT_DATA=00H. ATT transition of the soft-mute is from 00H to FFH

(2) The time for input data recovery to ATT level (Table 18). For example, in Normal Speed Mode, this time is 4096LRCK cycles (4096/fs) at ATT-DATA=FFH. ATT transition of soft-mute is from FFH to 00H.

(3) The analog output corresponding to the digital input has group delay, GD.

(4) If the soft mute is cancelled before attenuating to -∞, the attenuation is discontinued and returned to ATT level by the same cycle.

(5) When the input data at all the channels of the group are continuously zeros for 8192 LRCK cycles, DZF1, 2 pins of each channel goes to "H". DZF1/2 pins immediately returns to "L" if the input data of either channel of the group are not zero after going "H".

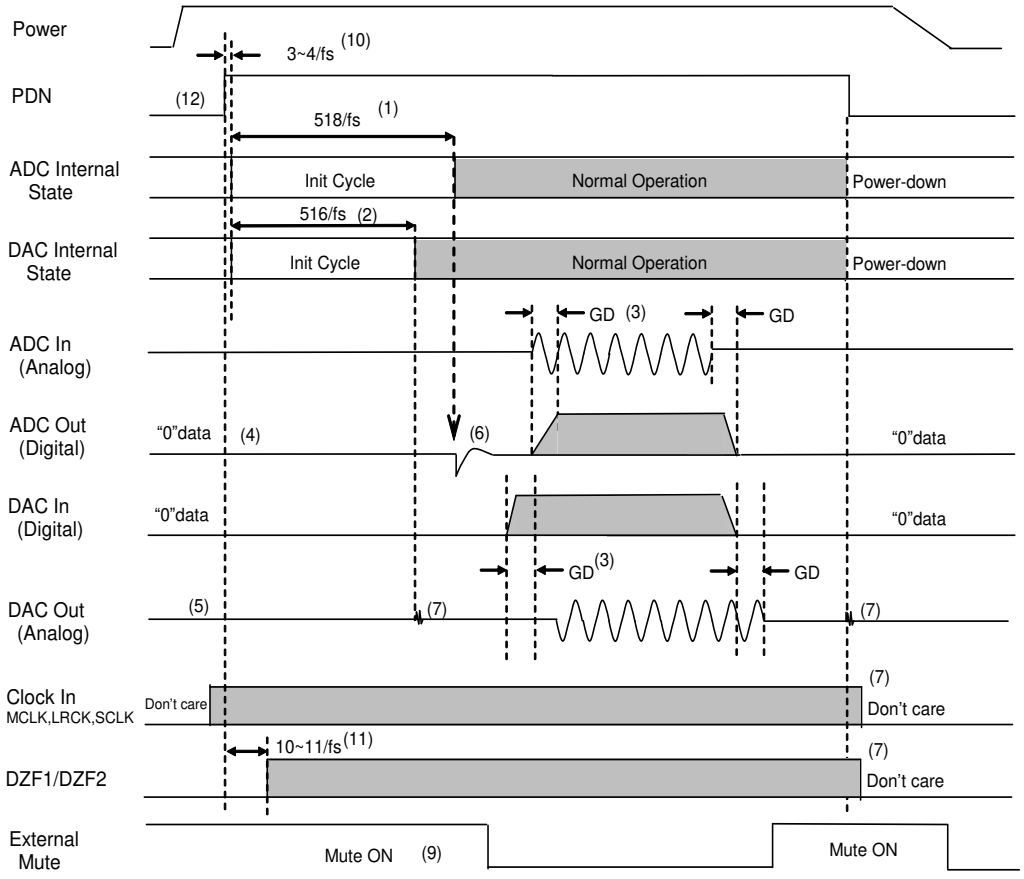
Figure 44. Soft mute and zero detection

■ System Reset

The AK4611 should be reset once by bringing the PDN pin = "L" upon power-up. The AK4611 is powered up and the internal timing starts clocking by LRCK "↑" after exiting the power down state of reference voltage (such as VCOM) by MCLK. The AK4611 is in power-down mode until MCLK and LRCK are input.

■ Power-Down

All ADCs and DACs of the AK4611 are placed in power-down mode by bringing the PDN pin "L" which resets both digital filters at the same time. The PDN pin "L" also resets the control registers to their default values. In power-down mode, when the DVMPD pin "L", the analog outputs go to VCOM voltage, when the DVMPD pin ="H", the analog outputs go to Hi-Z. The SDTO1-2, DZF1-2 pins go to "L" in the power-dwon mode. This reset should always be executed after power-up. For the ADC, an analog initialization cycle (518/fs) starts 3~4/fs after exiting power-down mode. The output data, SDTO1-2, is available after 521~522 cycles of the LRCK clock. For the DAC, an analog initialization cycle (516/fs) starts 3~4/fs after exiting power-down mode. The analog outputs are VCOM voltage when the DVMPD =pin "L", and the analog outputs go to Hi-Z when the DVMPD pin ="H" during the initialization. Figure 45 shows the power-down and power-up sequences.

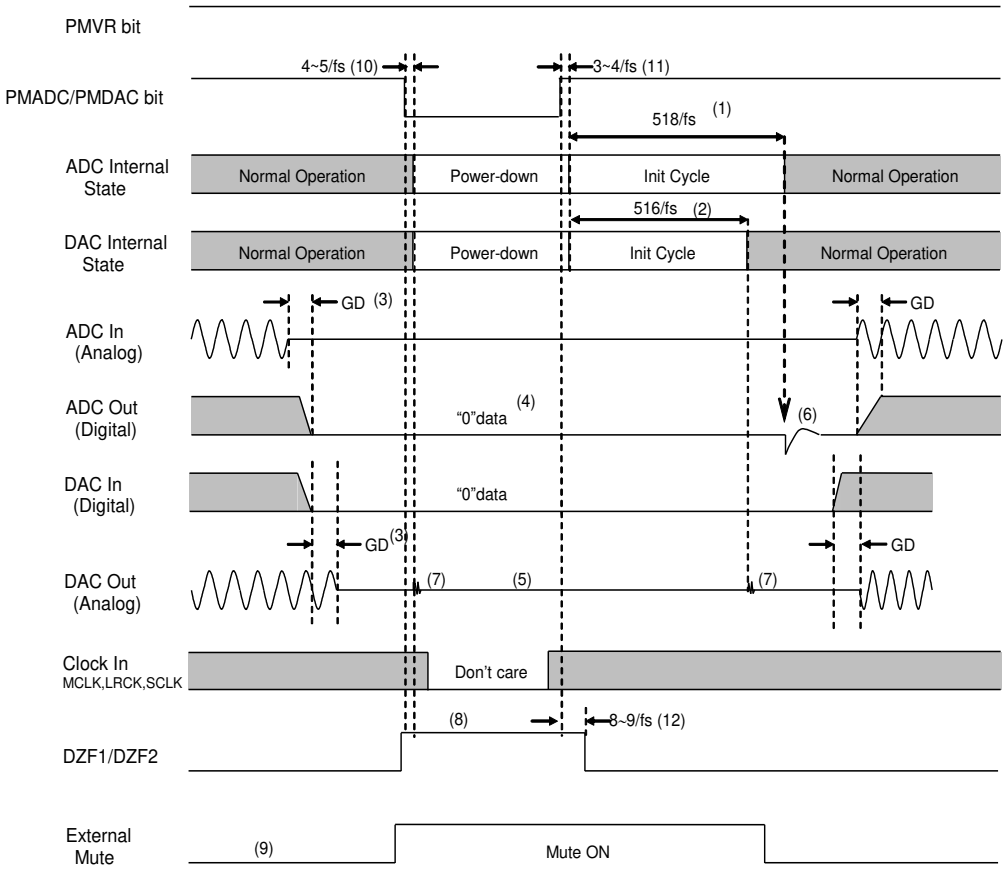


Notes:

(1) The analog part of ADC is initialized after exiting power-down state.
(2) The analog part of DAC is initialized after exiting power-down state.
(3) Digital output corresponds to analog input and analog output corresponds to digital input have group delay (GD).
(4) ADC output is "0" data at power-down state.
(5) The analog outputs are VCOM voltage when the DVMPD pin "L", and the analog outputs go to Hi-Z when the DVMPD pin "H" in power-down mode.
(6) Click noise occurs at the end of initialization of the analog part. Mute the digital output externally if the click noise influences system applications.
(7) Click noise occurs at the falling edge of PDN and at 519~520/fs after the rising edge of the PDN pin.
(8) DZF1-2 pins are "L" in power-down mode (PDN pin = "L").
(9) Please mute the analog output externally if the click noise (7) influences system applications.
(10) There is a delay, 3~4/fs from PDN pin "H" to the start of initial cycle.
(11) DZF pin= "L" for 10~11/fs after PDN pin = "↑".
(12) The PDN pin must be "L" when power up the AK4611 and set to "H" after all poweres are supplied.

Figure 45. Pin power-down/Pin power-up sequence example

All ADCs and all DACs can be powered-down individually through the PMADC bits and PMDAC bits, when the PMVR bit "1". ADC1-2 can be power-down individually through the PMAD2-1 bits. DAC1-4 can be power-down individually by PMDA4-1 bits. In this case, the internal register values are not initialized. When PMADC bit = "0", SDTO1-2 goes to "L". When PMDAC bit = "0", the analog outputs go to VCOM voltage when the DVMPD pin is "L", and the analog outputs go to Hi-Z when the DVMPD pin "H". When PMDAC bit = "0", DZF1-2 pins go to "H". As some click noise occurs, the analog output should be muted externally if the click noise influences system applications. Figure 46 shows the power-down and power-up sequences.



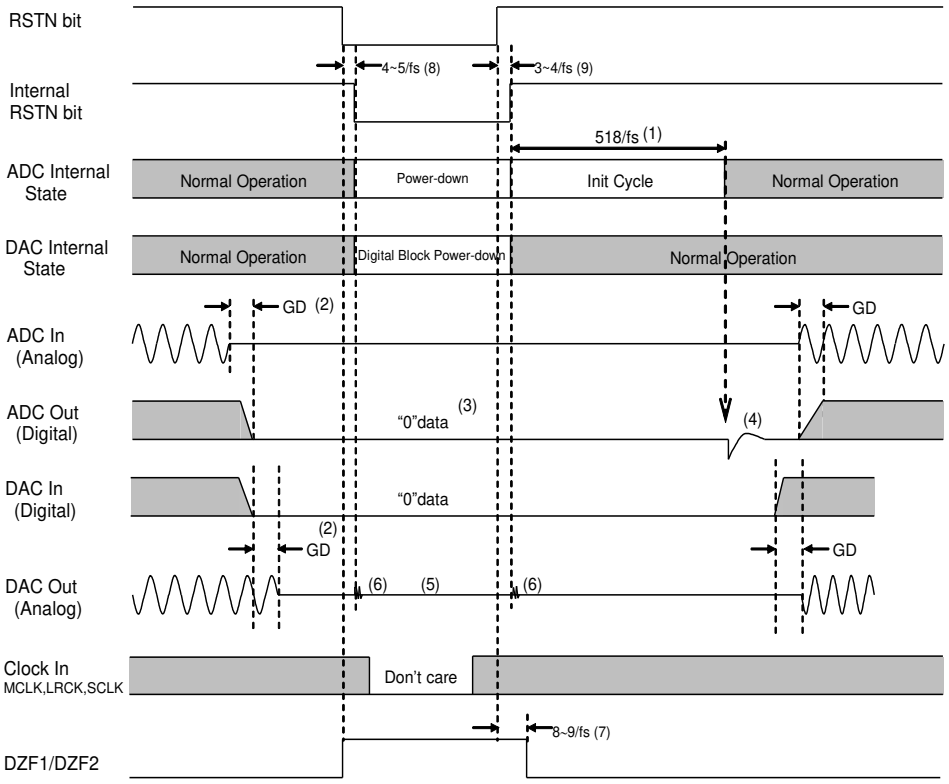
Notes:

(1) The analog section of ADC is initialized after exiting power-down state.
(2) The analog section of DAC is initialized after exiting power-down state.
(3) Digital output corresponding to the analog inputs and analog outputs corresponding to the digital inputs have group delay (GD).
(4) ADC output is "0" data at power-down state.
(5) The analog outputs are VCOM voltage when the DVMPD pin "L", and the analog outputs go to Hi-Z when the DVMPD pin "H" in power-down mode.
(6) Click noise occurs at the end of initialization of the analog part. Mute the digital output externally if the click noise influences system application.
(7) Click noise occurs at 4~5/fs after PMDAC bit becomes "0", and occurs at 519~520/fs after PMDAC bit becomes "1".
(8) DZF1-2 pins are "H" in power-down mode (PMDAC bit = "0").
(9) Mute the analog output externally if the click noise (7) influences system application.
(10) There is a delay, 4~5/fs from PMDAC bit becomes "0" to the applicable ADC power-down.
There is a delay, 4~5/fs from PMDAC bit becomes "0" to the applicable DAC power-down.
(11) There is a delay, 3~4/fs from PMADC and PMDAC bits become "1" to the start of initial cycle.
(12) DZF pin= "L" for 8~9/fs after PMDAC bit becomes "1".

Figure 46. Bit power-down/Bit power-up sequence example

■ Reset Function

When RSTN bit= "0", the analog and digital part of ADC and the digital part of DACs are powered-down, but the internal register are not initialized. The analog outputs go to VCOM voltage regardless of the DVMPD pin setting, then DZF1-2 pins go to "H" and SDTO1-2 pins go to "L". As some click noise occurs, the analog output should be muted externally if the click noise influences system application. Figure 47 shows the power-up sequence.



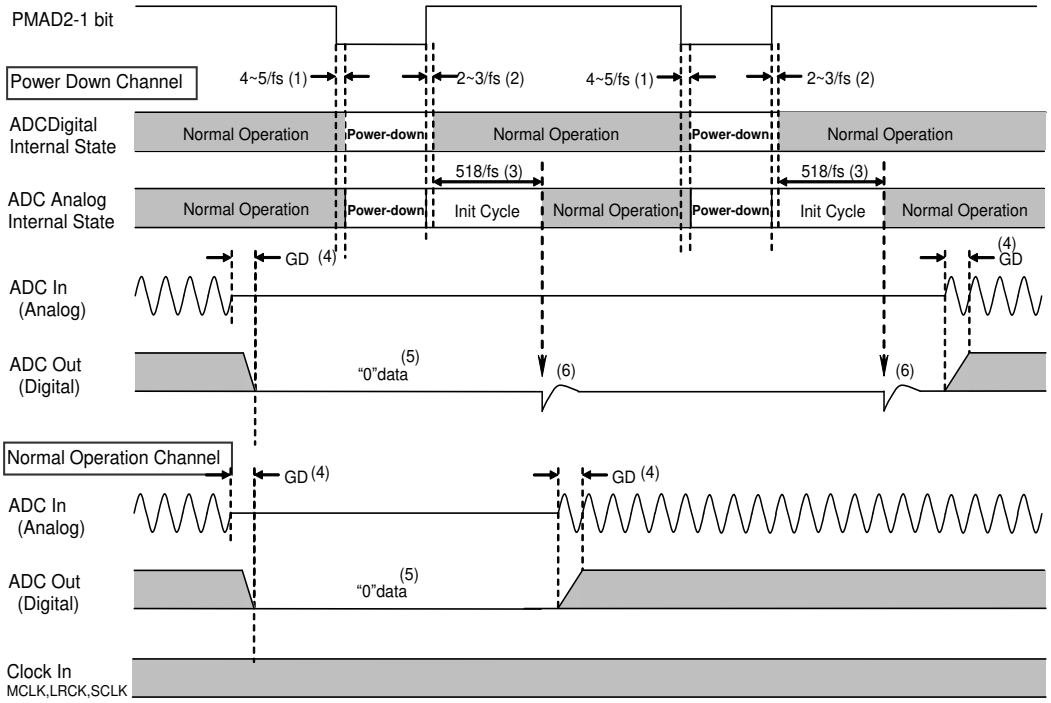
Notes:

(1) The analog section of the ADC is initialized after exiting reset state.
(2) Digital output corresponding to the analog inputs, and analog outputs corresponding to the digital inputs have group delay (GD).
(3) ADC output is "0" data at power-down state.
(4) Click noise occurs when the internal RSTN bit becomes "1". Mute the digital output externally if the click noise influences system application.
(5) The analog outputs go to VCOM voltage regardless of the DVMPD pin setting when RSTN bit becomes "0".
(6) Click noise occurs at 4~5/fs after RSTN bit becomes "0", and occurs at 3~4/fs after RSTN bit becomes "1".
(7) DZF pins go to "H" when the RSTN bit becomes "0", and go to "L" at 8~9/fs after RSTN bit becomes "1".
(8) There is a delay, 4~5/fs from RSTN bit "0" to the internal RSTN bit "0".
(9) There is a delay, 3~4/fs from RSTN bit "1" to the start of initial cycle.

Figure 47. Reset sequence example

■ ADC partial Power-Down Function

All of the ADCs can be powered-down individually by PMAD2-1 bits. The analog section and the digital section of the ADC are in power-down mode when the PMAD2-1 bits = "0". The analog section of ADCs are initialized after exiting the power-down state. Digital output corresponding to analog input have group delay (GD). ADC output is "0" data at the power-down state. Click noise occurs when the internal RSTN bit becomes "1". Mute the digital output externally if the click noise influences system applications. Figure 48 shows the power-down and power-up sequences by PMAD2-1 bits.



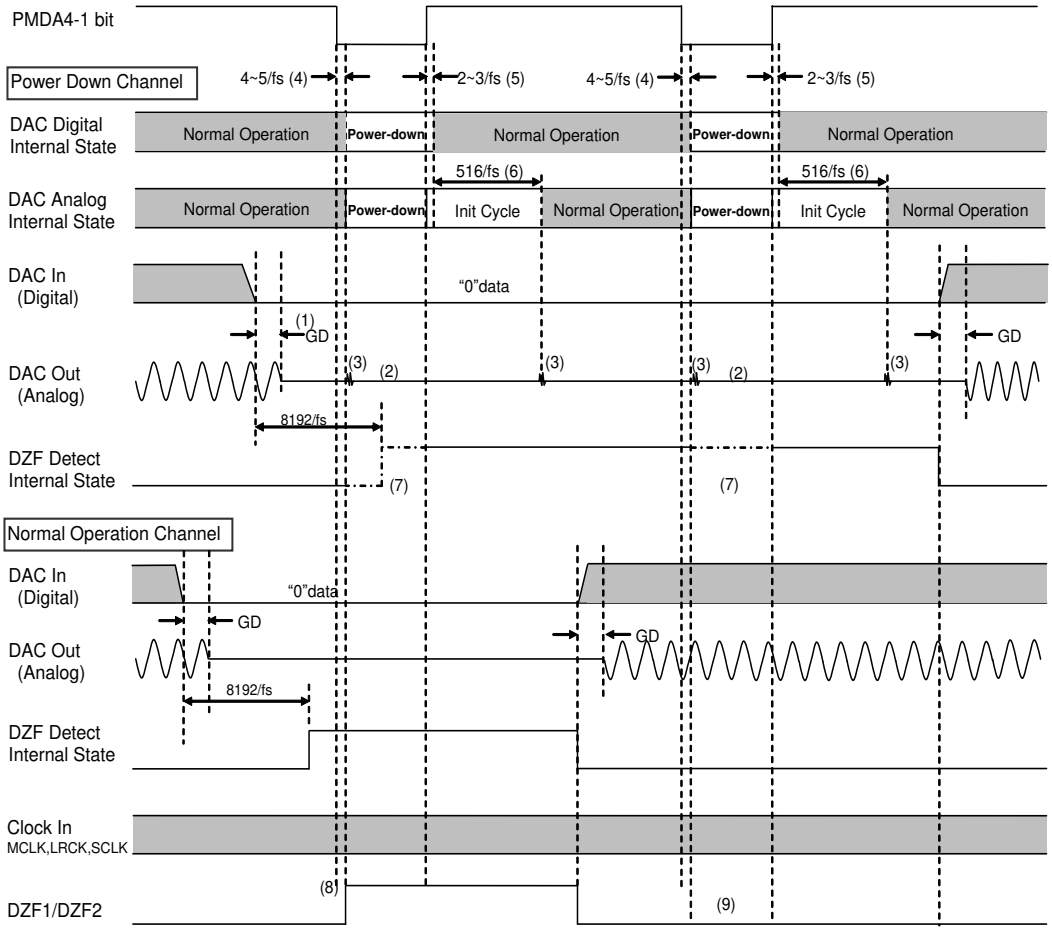
Notes.

(1) There is a delay, 4~5/fs from PMAD2-1 bits become "0" to the applicable ADC power-down.
(2) There is a delay, 2~3/fs from PMAD2-1 bits "1" to the start of initial cycle.
(3) The analog section of the ADC is initialized after exiting reset state.
(4) Analog output corresponding to the digital inputs have group delay (GD).
(5) ADC output is "0" data at power-down state.
(6) Click noise occurs when the internal RSTN bit becomes "1". Mute the digital output externally if the click noise influences system application.

Figure 48. ADC partial power-down example

■ DAC partial Power-Down Function

All of the DACs can be powered-down individually by PMDA4-1 bits. The analog section and the digital section of the DAC are placed in power-down mode when the PMDA4-1 bits = "0". The analog output of the powered-down channels, which is by PMDA4-1 bits, go to the voltage of VCOM when the DVMPD pin is "L", and go to Hi-Z when the DVMPD pin "H". Although DZF detection is in operation, the AK4611 stops reflecting the result of DZF detection to DZF1-2 pins. Some click noise occurs in both set-up and release of power-down. Mute the analog output externally or set PMDA4-1 bits when PMDAC bit = "0" or RSTN bit = "0", if click noise aversely affects system performance. Figure 49 shows the sequence of the power-down and the power-up by PMDA4-1 bits.



Notes:

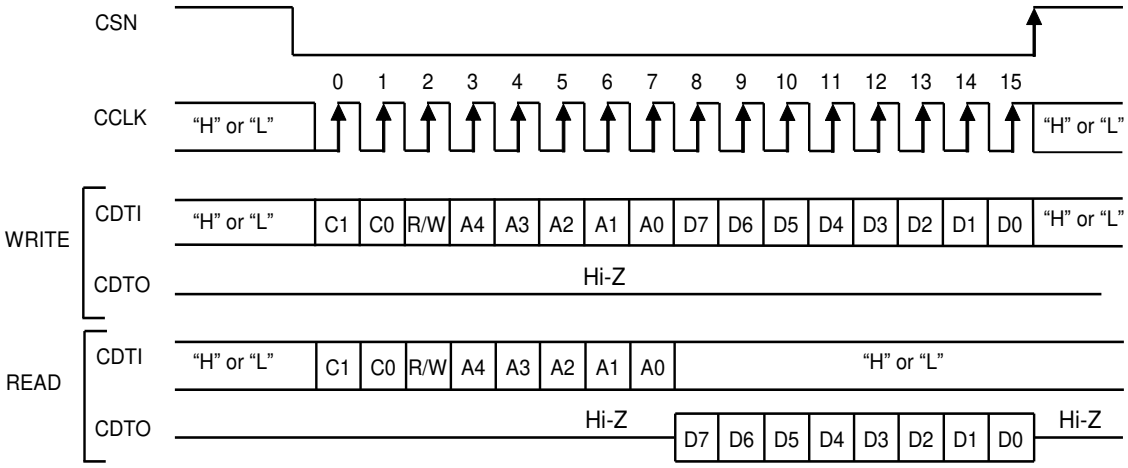
(1) Digital output corresponding to the analog inputs, and analog outputs corresponding to the digital inputs have group delay (GD).
(2) Analog output of the DAC powered down by PMDA4-1 = "0" and goes to VCOM voltage when the DVMPD pin ="L", and the analog outputs go to Hi-Z when the DVMPD pin ="H".
(3) Click noise occurs at 4~5/fs after RSTN bit becomes "0", and occurs at 3~4/fs after RSTN bit becomes "1". after PMDA4-1 bits are changed, some click noise occurs immediately at output of the channel changed by the own PD bits.
(4) The DACs will be powered-down 4~5fs after PMDA4-1 bits = "0"
(5) The initiation stars 2~3fs after PMDA4-1 bits are set to "1".
(6) The analog parts of DACs are initilised after exiting power down mode.
(7) Although DZF detection is active at a certain channel set up though PMDA4-1 = "0", the AK4611 stops reflecting the result of DZF detection to DZF1-2 pins.
(8) DZF detection of the DAC which is set up by the power-down setting is ignored, and DZF1-2 pins go to "H".
(9) When signal is input to a DAC, even if the partical power down is applied, DZF1-2 pins will not become "H".

Figure 49. DAC partial power-down example

■ Serial Control Interface

The AK4611's functions are controlled through registers. The registers may be written by two types of control modes. The chip address is determined by the state of the CAD0 and CAD1 inputs. The PDN pin = "L" initializes the registers to their default values. Writing "0" to the RSTN bit can initialize the internal timing circuit, but the register data will not be initialized.

(1) 4-wire Serial Control Mode (I2C pin = "L")
The internal registers may be written through the 4-wire µP interface pins (CSN, CCLK, CDTI and CDTO). The data on this interface consists of a 2-bit Chip address, Read/Write, Register address (MSB first, 5bits) and Control data (MSB first, 8bits). The chip address high bit is fixed to "1" and the lower bit is set by the CAD0 pin. Address and data are clocked in on the rising edge of CCLK and data is clocked out on the falling edge. After a low-to-high transition of CSN, data is latched for write operations and CDTO bit outputs Hi-Z. The clock speed of CCLK is 5MHz (max). The value of internal registers is initialized when the PDN pin = "L".



C1 – C0: Chip Address (C1=CAD1, C0=CA0)
R/W: READ / WRITE ("1": WRITE, "0": READ)
A4 - A0: Register Address
D7 – D0: Control Data

Figure 50. Serial Control I/F Timing

(2) I²C-bus Control Mode (I2C pin = "H")
The AK4611 supports the fast-mode I²C-bus (max: 400kHz).

(2)-1. WRITE Operations
Figure 51 shows the data transfer sequence of the I²C-bus mode. All commands are preceded by START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates START condition (Figure 57). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "00100". The next bits are CAD1 and CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pins (CAD1/0 pins) set these device address bits (Figure 52). If the slave address matches that of the AK4611, the AK4611 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 58). R/W bit = "1" indicates that the read operation is to be executed. "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4611. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 53). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 54). The AK4611 generates an acknowledge after each byte is received. Data transfer is always terminated by STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 57).

The AK4611 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4611 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 59) except for the START and STOP conditions.

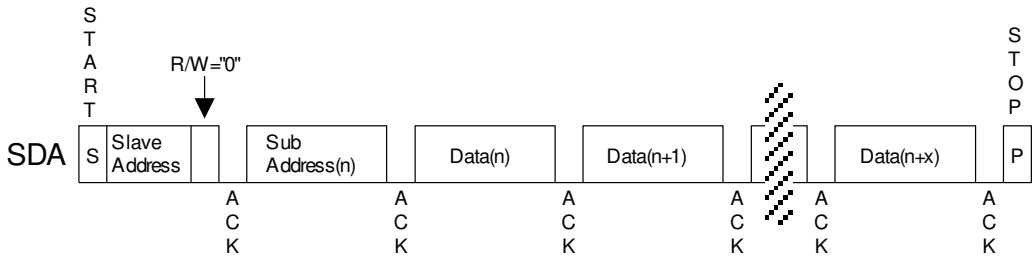


Figure 51. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	CAD1	CAD0	R/W

(Those CAD1/0 should match with CAD1/0 pins)
Figure 52. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 53. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 54. Byte Structure after the second byte

(2)-2. READ Operations
Set the R/W bit = "1" for the READ operation of the AK4611. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address.

The AK4611 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(2)-2-1. CURRENT ADDRESS READ
The AK4611 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4611 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4611 ceases transmission.

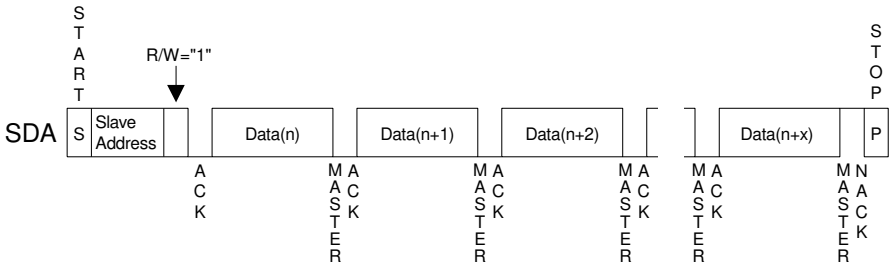


Figure 55. CURRENT ADDRESS READ

(2)-2-2. RANDOM ADDRESS READ
The random read operation allows the master to access any memory location at random. Prior to issuing a slave address with the R/W bit ="1", the master must execute a "dummy" write operation first. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit ="1". The AK4611 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4611 ceases transmission.

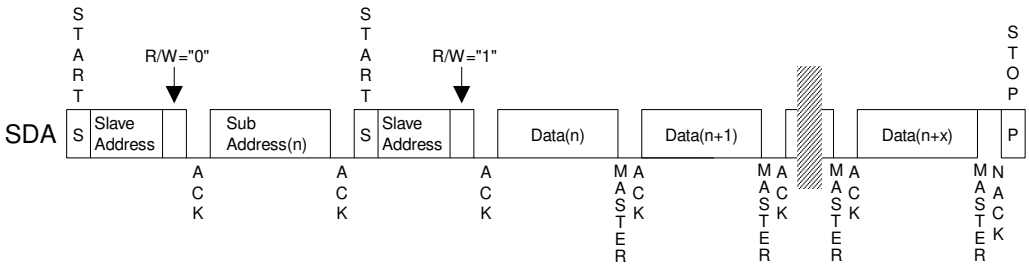


Figure 56. RANDOM ADDRESS READ

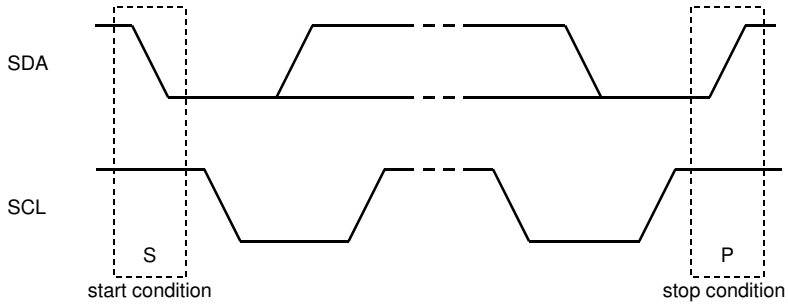


Figure 57. START and STOP Conditions

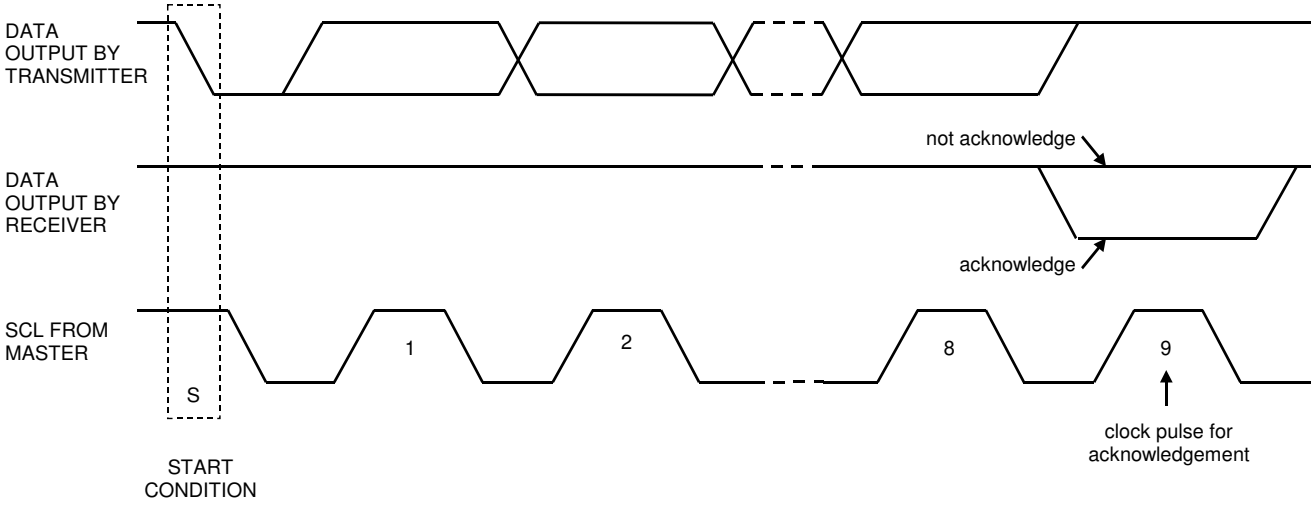


Figure 58. Acknowledge on the I^2C-Bus

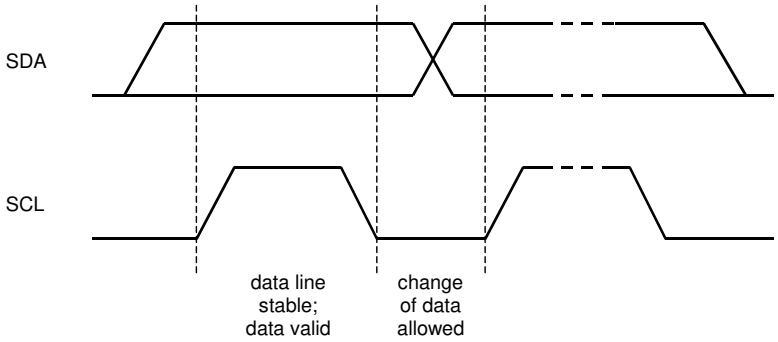


Figure 59. Bit Transfer on the I^2C-Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	0	0	0	PMVR	PMADC	PMDAC	RSTN
01H	Power Management 2	0	0	0	0	0	1	PMAD2	PMAD1
02H	Power Management 3	0	0	1	1	PMDA4	PMDA3	PMDA2	PMDA1
03H	Control 1	TDM1	TDM0	DIF2	DIF1	DIF0	ATS1	ATS0	SMUTE
04H	Control 2	0	MCKO	CKS1	CKS0	DFS1	DFS0	ACKS	DIV
05H	De-emphasis1	DEM41	DEM40	DEM31	DEM30	DEM21	DEM20	DEM11	DEM10
06H	Reserved	0	0	0	0	0	1	0	1
07H	Overflow Detect	0	0	0	0	OVFE	OVFM2	OVFM1	OVFM0
08H	Zero Detect	LOOP1	LOOP0	0	0	DZFM3	DZFM2	DZFM1	DZFM0
09H	Input Control	0	0	0	0	0	1	DIE2	DIE1
0AH	Output Control	0	0	1	1	DOE4	DOE3	DOE2	DOE1
0BH	LOUT1 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0CH	ROUT1 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0DH	LOUT2 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0EH	ROUT2 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0FH	LOUT3 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
10H	ROUT3 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
11H	LOUT4 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
12H	ROUT4 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

Note: For addresses from 13H to 1FH, data is not written.
When the PDN pin goes to “L”, the registers are initialized to their default values.
When RSTN bit goes to “0”, the internal timing is reset and the DZF1-2 pins go to “H”, but registers are not initialized to their default values.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	0	0	0	0	PMVR	PMADC	PMDAC	RSTN
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	1	1

RSTN: Internal timing reset
0: Reset. DZF1-2 pins go to "H", but registers are not initialized.
1: Normal operation

PMDAC: Power management of DAC1-4
0: Power-down
1: Normal operation

PMADC: Power management of ADC1-2
0: Power-down
1: Normal operation

PWVR: Power management of reference voltage
0: Power-down
1: Normal operation
When any blocks are powered-up, the PMVR bit must be set to "1". PMVR bit can be set to "0" only when PMADAL=PMADAR= bits = "0".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 2	0	0	0	0	0	1	PMAD2	PMAD1
R/W		RD	RD	RD	RD	RD	RD	R/W	R/W
Default		0	0	0	0	0	1	1	1

PMAD2-1: Power management of ADC1-2 (0: Power-down, 1: Normal operation)
PMAD1: Power management control of ADC1
PMAD2: Power management control of ADC2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Power Management 3	0	0	1	1	PMDA4	PMDA3	PMDA2	PMDA1
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	1	1	1	1	1	1

PMDA4-1: Power management of DAC1-4 (0: Power-down, 1: Normal operation)
PMDA1: Power management control of DAC1
PMDA2: Power management control of DAC2
PMDA3: Power management control of DAC3
PMDA4: Power management control of DAC4

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Control 1	TDM1	TDM0	DIF2	DIF1	DIF0	ATS1	ATS0	SMUTE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	0	0	0	0

SMUTE: Soft Mute Enable
0: Normal operation
1: All DAC outputs soft-muted

ATS1-0: Digital attenuator transition time setting (Table 18)
Initial: "00", mode 0

DIF2-0: Audio Data Interface Modes (Table 11, Table 12, Table 13, Table 14)
Initial: "100", mode 4
TDM1-0: TDM Format Select (Table 11, Table 12, Table 13, Table 14)

Mode	TDM1	TDM0	SDTI	Sampling Speed
0	0	0	1-6	Stereo mode (Normal, Double, Quad Speed Mode)
1	0	1	1	TDM512 mode (Normal Speed Mode)
2	1	0	1-2	TDM256 mode (Double Speed Mode)
3	1	1	1-3	TDM128 mode (Quad Speed Mode)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Control 2	0	MCKO	CKS1	CKS0	DFS1	DFS0	ACKS	DIV
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	0	0	0	0	0

DIV: Output of Master clock frequency
0: x 1
1: x 1/2

ACKS: Master Clock Frequency Auto Setting Mode Enable
0: Disable, Manual Setting Mode
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically at ACKS bit "1". In this case, the setting of DFS are ignored. When this bit is "0", DFS0, 1 set the sampling speed mode.

DFS1-0: Sampling speed mode (Table 1)
The setting of DFS is ignored at ACKS bit ="1".

CKS1-0: Master Clock Input Frequency Select (Table 2)

MCKO: Master clock output enable
0: Output "L"
1: Output "MCKO"

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	De-emphasis1	DEM41	DEM40	DEM31	DEM30	DEM21	DEM20	DEM11	DEM10
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	0	1	0	1

DEMA11-10: De-emphasis response control for DAC1 data on SDTI1 (Table 8)
Initial: "01", OFF

DEMA21-20: De-emphasis response control for DAC2 data on SDTI1 (Table 8)
Initial: "01", OFF

DEMA31-30: De-emphasis response control for DAC3 data on SDTI1 (Table 8)
Initial: "01", OFF

DEMA41-40: De-emphasis response control for DAC4 data on SDTI1 (Table 8)
Initial: "01", OFF

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Overflow Detect	0	0	0	0	OVFE	OVFM2	OVFM1	OVFM0
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	1	1

OVFM2-0: Overflow detect mode select (Table 15)
Initial: "111", disable

OVFE: Overflow detection enable (Table 15)
0: Disable, pin#33 becomes DZF2 pin.
1: Enable, pin#33 becomes OVF pin.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Zero Detect	LOOP1	LOOP0	0	0	DZFM3	DZFM2	DZFM1	DZFM0
R/W		R/W	R/W	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	1	1

DZFM3-0: Zero detect mode select (Table 16)
Initial: "1111", disable

LOOP1-0: Loopback mode enable
00: Normal (No loop back)
01: LIN1 → LOUT1, LOUT2
RIN1 → ROUT1, ROUT2
LIN2 → LOUT3, LOUT4
RIN2 → ROUT3, ROUT4

The digital ADC output is connected to the digital DAC input. In this mode, the input DAC data to SDTI1-4 are ignored. The audio format of SDTO at loopback mode becomes mode 3 at mode 0 or 1, and mode 5 at mode 2, respectively.

10: SDTI1(L) → SDTI2(L), SDTI3(L), SDTI4(L)
SDTI1(R) → SDTI2(R), SDTI3(R), SDTI4(R)
In this mode, the input DAC data to SDTI2-4 are ignored.

11: Not Available

LOOP1-0 should be set to "00" at TDM mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Output Control	0	0	0	0	0	1	DIE2	DIE1
R/W		RD	RD	RD	RD	RD	RD	R/W	R/W
Default		0	0	0	0	0	1	1	1

DIE2-1: ADC1-2 Differential Input Enable (0: Single-End Input, 1: Differential Input)

DIE1: ADC1 Differential Input Enable
DIE2: ADC2 Differential Input Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Output Control	0	0	1	1	DOE4	DOE3	DOE2	DOE1
R/W		RD	RD	RD	RD	R/W	R/W	R/W	R/W
Default		0	0	1	1	1	1	1	1

DOE4-1: DAC1-4 Differential Output Enable (0: Single-End Input, 1: Differential Input)
DOE1: DAC1 Differential Output Enable
DOE2: DAC2 Differential Output Enable
DOE3: DAC3 Differential Output Enable
DOE4: DAC4 Differential Output Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0BH	LOUT1 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0CH	ROUT1 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0DH	LOUT2 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0EH	ROUT2 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0FH	LOUT3 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
10H	ROUT3 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
11H	LOUT4 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
12H	ROUT4 Volume Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ATT7-0: Attenuation Level (Table 17)

* A power-down release command must be write again (dummy write) after 5 LRCK cycles or later form the first command when releasing power-down mode by PMVR, PMDAC, RSTN, PMDA1, PMDA2, PMDA3 or PMDA4 bit in I2C mode. If this dummy write is not executed, DATT output will keep the initial value (0dB) until the next write is executed. (Figure 43)

SYSTEM DESIGN

Condition: Differential Input (DIE2-1 bit = "11"), Differential Output (DOE4-1 bit = "1111")
4-wire Serial Control Interface (I2C pin = "L")
Master mode (M/S pin = "H")
The AK4611 has the analog Anti-Alias Filter for Differential Input.
The AK4611 does not have the analog Smoothing Filter for Differential Output.

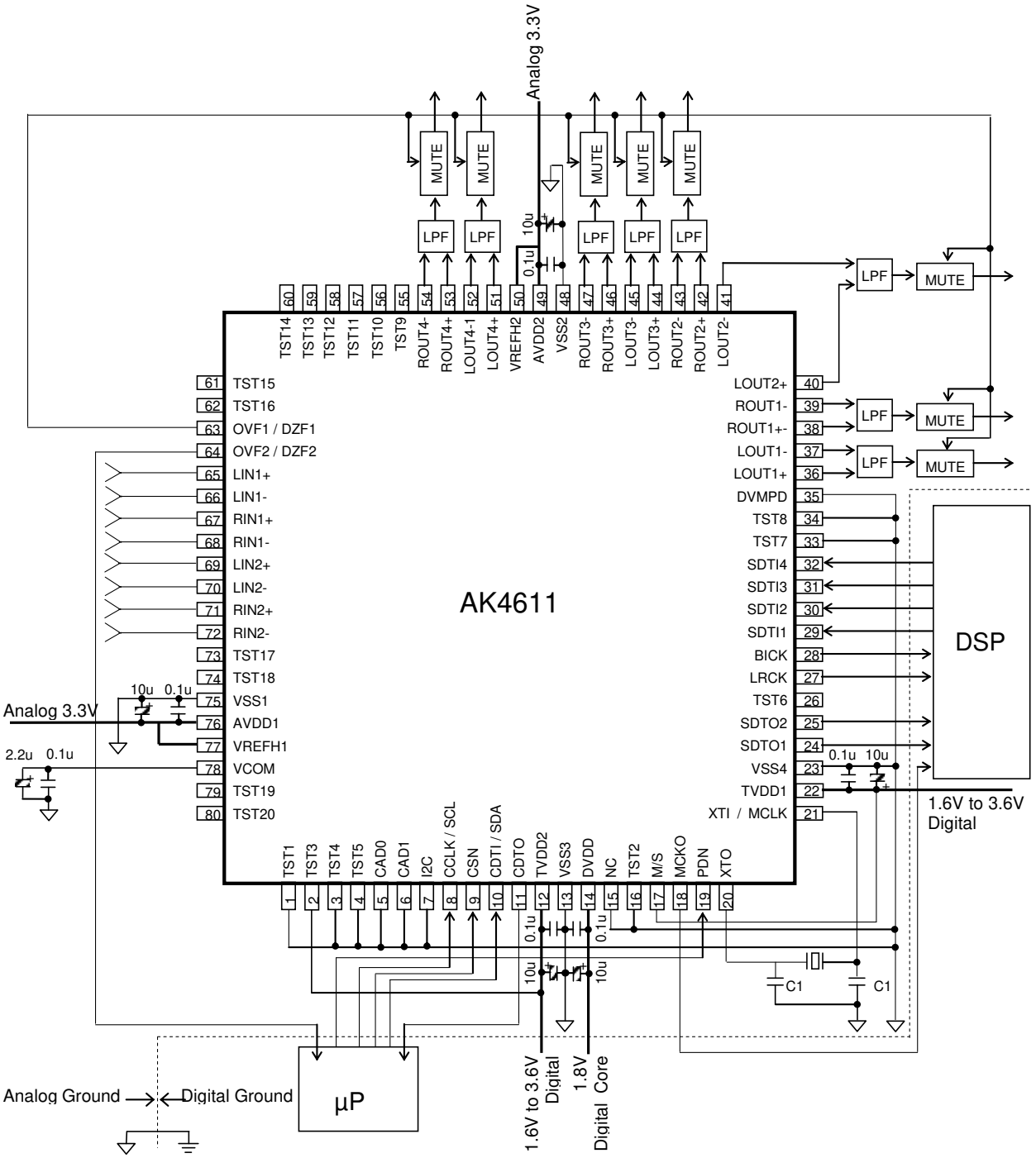


Figure 60. Typical Connection Diagram1

Condition: Single-end Input (DIE2-1 bit = "00"), Single-end Output (DOE4-1 bit = "0000")
I²C Bus Control Interface (I2C pin = "H")
Slave mode (M/S pin = "L")
The AK4611 has the analog Anti-Alias Filter for Single-Ended Input.
The AK4611 has the analog Smoothing Filter for Single-Ended Output.

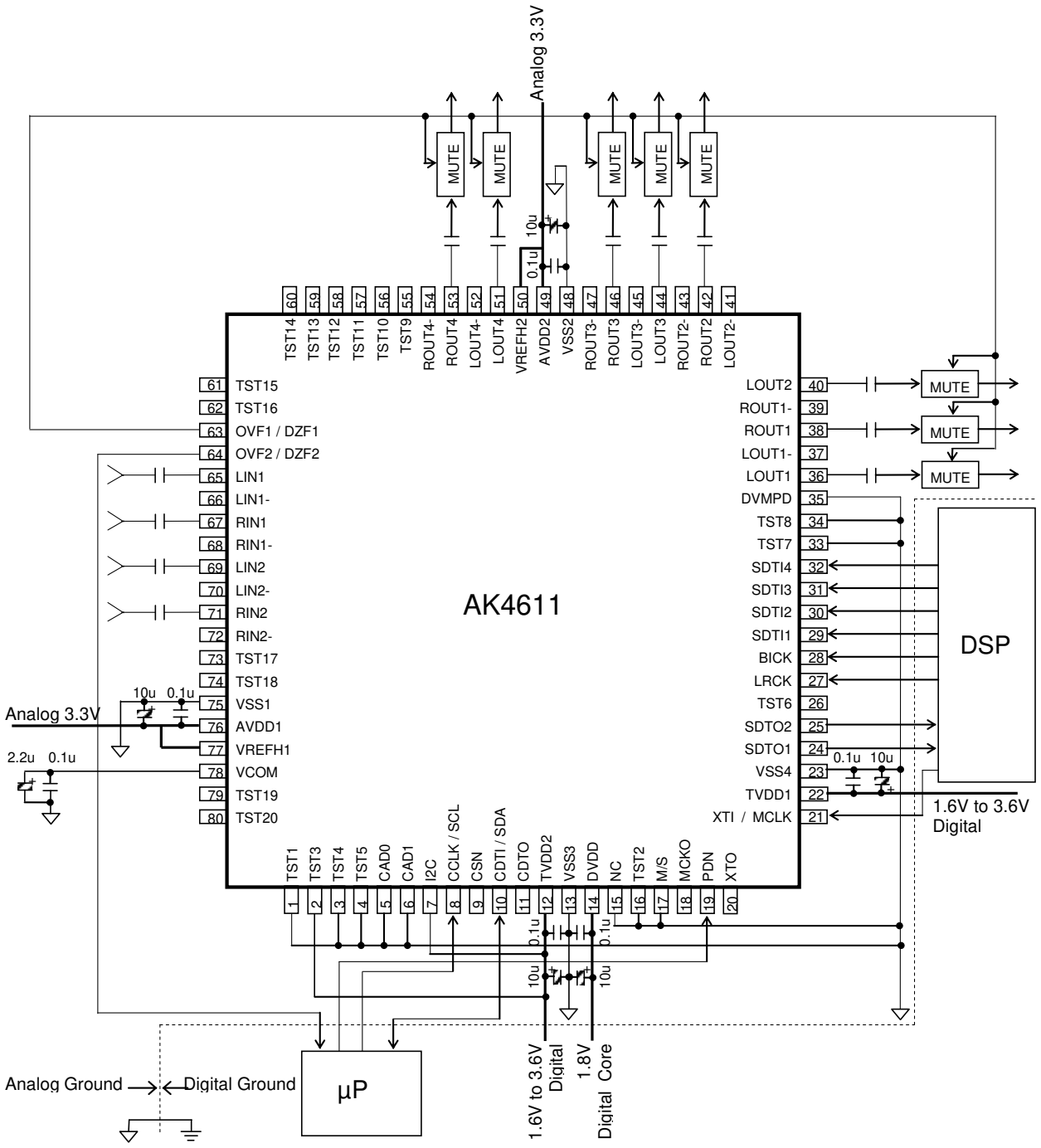


Figure 61. Typical Connection Diagram2

1. Grounding and Power Supply Decoupling

The AK4611 requires careful attention to power supply and grounding arrangements. AVDD1, AVDD2, TVDD1 and TVDD2 are usually supplied from analog supply in system. Alternatively if AVDD1, AVDD2, TVDD1 and TVDD2 are supplied separately, the power up sequence is not critical. **VSS1, VSS2, VSS3 and VSS4 of the AK4611 must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4611 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference Inputs

The voltage of VREFH1, VREFH2 set the analog input/output range. The VREFH1 pin is normally connected to AVDD1 with a 0.1μF ceramic capacitor. The VREFH2 pin is normally connected to AVDD2 with a 0.1μF ceramic capacitor. VCOM is a signal ground of this chip and output the voltage AVDD1x1/2. An electrolytic capacitor 2.2μF parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. Ceramic capacitors should be as near to the pin as possible. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VREFH1, VREFH2 and VCOM pins in order to avoid unwanted coupling into the AK4611.

3. Analog Inputs

The ADC inputs correspond to single-ended and differential are able to select by DIE2-1 bits. When the inputs are single-ended, internally biased to the common voltage (AVDD1x1/2) with 9kΩ(typ) resistance. The input signal range scales with the supply voltage and nominally 0.65xVREFH1 Vpp (typ) @fs=48kHz. When the inputs are differential, internally biased to the common voltage (AVDD2x1/2) with 13kΩ(typ) resistance. The input signal range between LIN(RIN)+ and LIN(RIN)− scales with the supply voltage and nominally ±0.65xVREFH1 Vpp (typ) @fs=48kHz The ADC output data format is 2's complement. The internal HPF removes the DC offset.

The AK4611 samples the analog inputs at 128fs (@ fs=48kHz). The digital filter rejects noise above the stop band except for multiples of the sampling frequency of analog inputs. The AK4611 includes an anti-aliasing filter (RC filter) to attenuate a noise around the sampling frequency of analog inputs.

4. Analog Outputs

The DAC outputs correspond to single-ended and differential are able to select by DOE4-1 bits. When the outputs are single-ended, the output signal range is centered around the VCOM voltage and nominally 0.63 x VREFH2 Vpp. When the outputs are differential, the output signal ranges are ±0.63 x VREFH2 Vpp (typ) centered around the VCOM voltage. The differential outputs are summed externally, V_{AOUT} = [L(R)OUT+]-[L(R)OUT-] between L(R)OUT+ and L(R)OUT-. If the summing gain is 1, the output range is 4.16Vpp (typ@AVDD2=3.3V). The bias voltage of the external summing circuit is supplied externally. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal output is VCOM voltage for 000000H(@24bit). The internal analog filters remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband, when the single-end input mode. The differential output mode does not have the internal analog filters, therefore this noise should be remove by the external analog filters.

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV.

5. External Analog Inputs Circuit

Figure 62 shows the input buffer circuit example 1. The input level of this circuit is 4.3Vpp (AK4611: typ. ±2.15Vpp).

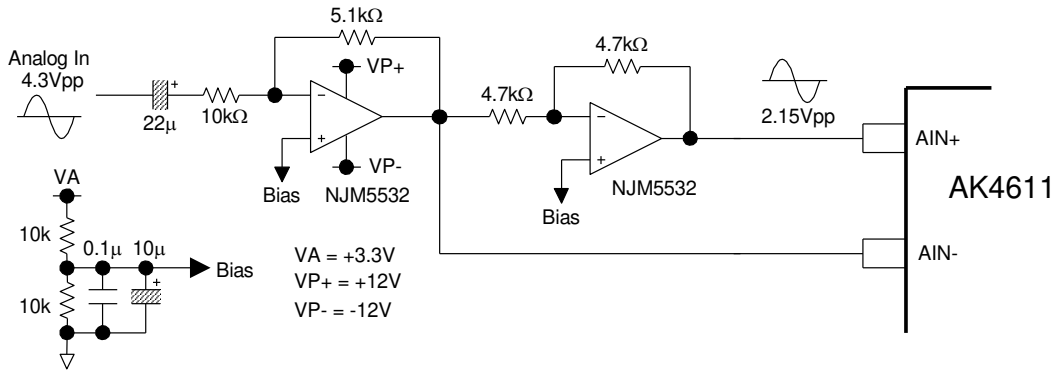


Figure 62. Input buffer circuit example 1 (DC coupled single-end input)

Figure 63 shows the input buffer circuit example 2. The input level of this circuit is 4.3Vpp (AK4611: typ. ±2.15Vpp).

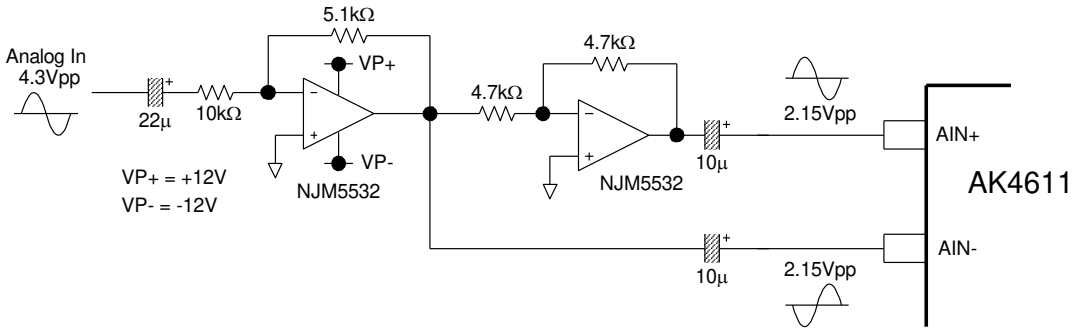


Figure 63. Input buffer circuit example 2 (AC coupled single-end input)

Figure 64 shows the input buffer circuit example 3. The input level of this circuit is ±2.15Vpp (AK4611: typ. ±2.15Vpp).

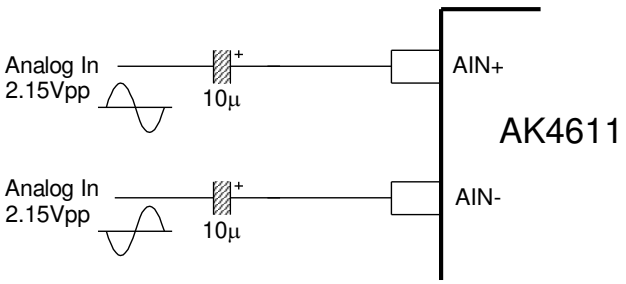


Figure 64. Input buffer circuit example 3 (AC coupled differential input)

Figure 65 shows the input buffer circuit example 4. The input level of this circuit is ±2.15Vpp (AK4611: typ. ±2.15Vpp).

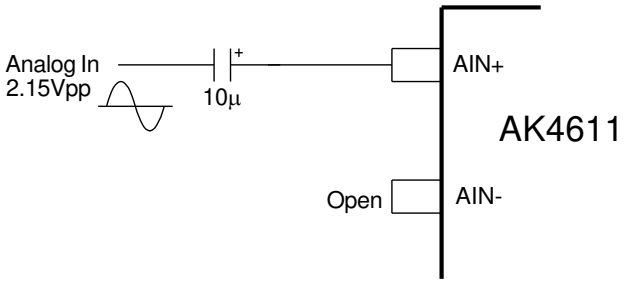


Figure 65. Input buffer circuit example 4 (AC coupled single-end input)

6. External Analog Outputs Circuit

Figure 66 shows the output buffer circuit example 1. The output level of this circuit is 4.16Vpp (AK4611: typ. ±2.08Vpp).

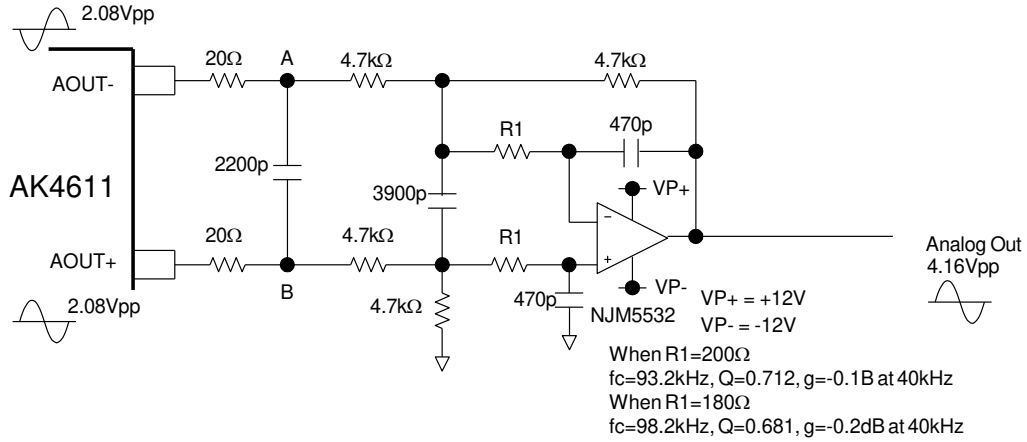


Figure 66. Output buffer circuit example 1 (DC coupled differential output)

Figure 67 shows the output buffer circuit example 2. The output level of this circuit is 4.16Vpp (AK4611: typ. ±2.08Vpp).

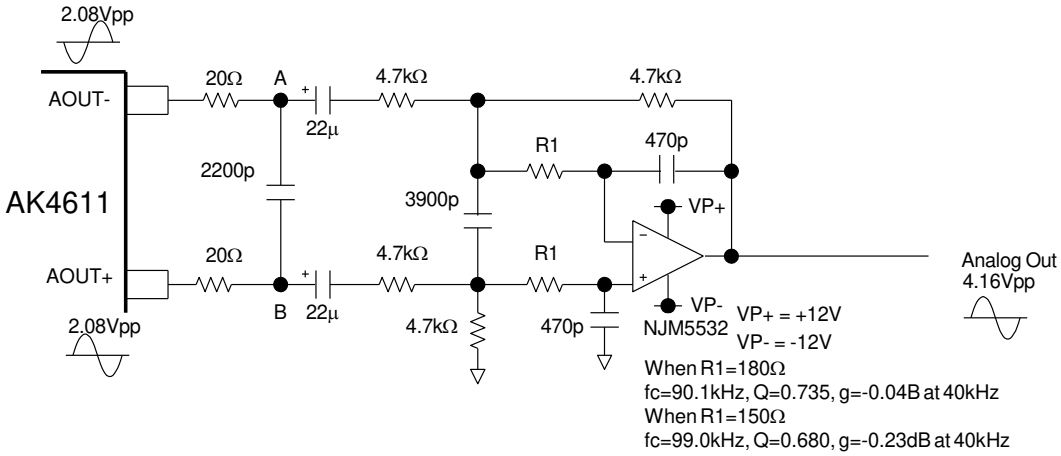


Figure 67. Output buffer circuit example 2 (AC coupled differential output)

Figure 68 shows the output buffer circuit example 3. The output level of this circuit is 4.16Vpp (AK4611: typ. 2.08Vpp).

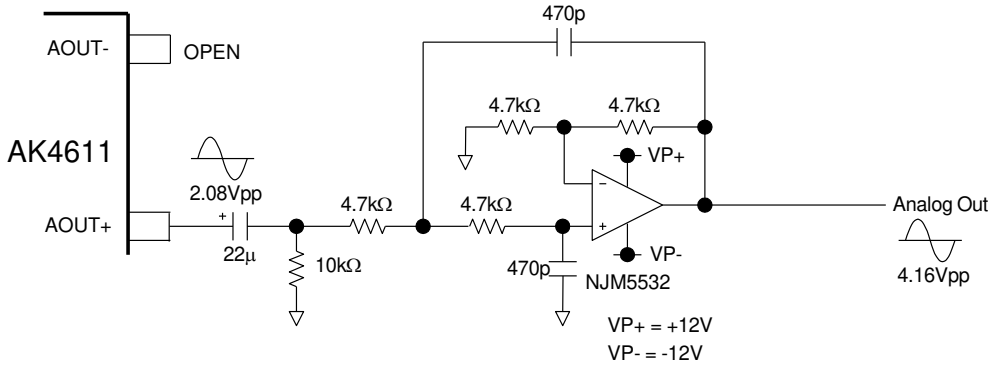


Figure 68. Output buffer circuit example 3 (AC coupled single-end output)

Figure 69 shows the output buffer circuit example 4. The output level of this circuit is 2.08Vpp (AK4611: typ. 2.08Vpp).

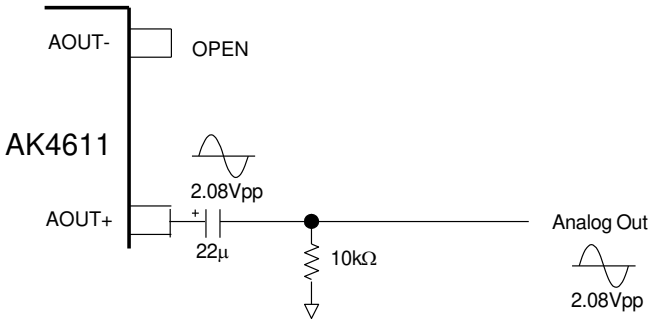
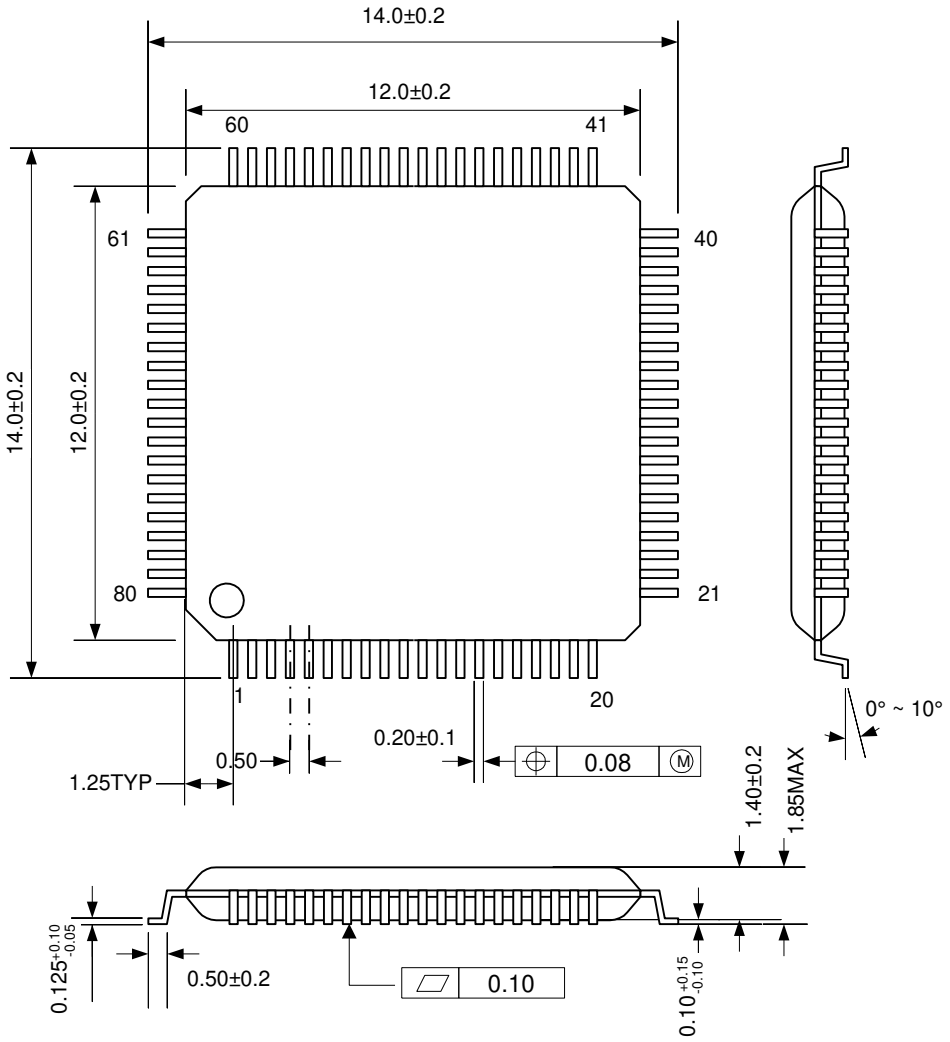


Figure 69. Output buffer circuit example 4 (AC coupled single-end output)

PACKAGE

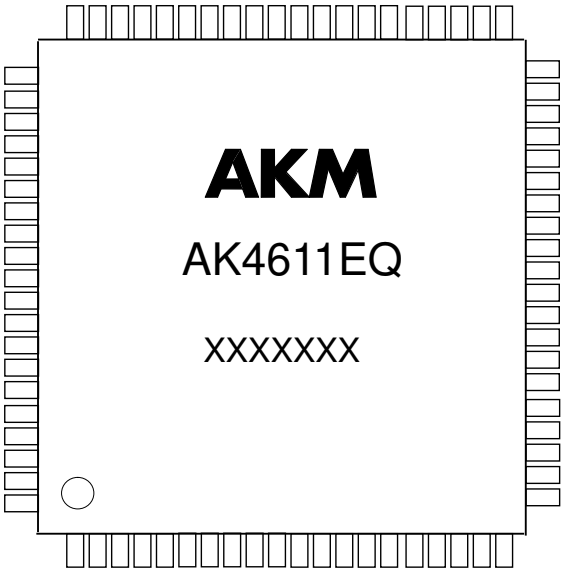
- 80-pin LQFP (Unit: mm)



■ Package & Lead frame material

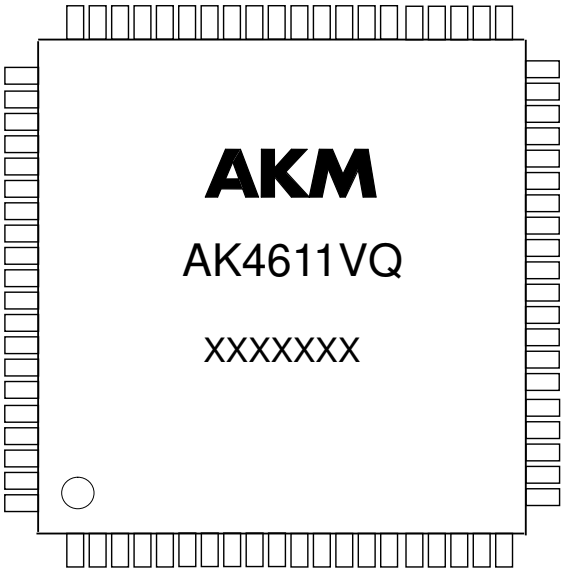
Package molding compound:	Epoxy resin, Halogen (bromine and chlorine) free
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING (AK4611EQ)



1) Pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK4611EQ
4) Asahi Kasei Logo

MARKING (AK4611VQ)



1) Pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK4611VQ
4) Asahi Kasei Logo

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
09/02/06	00	First Edition		
09/06/05	01	Specification Change	10	ANALOG CHARACTERISTICS ADC Analog Input Characteristics (differential) S/(N+D) fs=48kHz, -1dBFS: 89 → 88 (min)
10/06/14	02	Description Addition		AK4611EQ was added.
13/07/03	03	Description Addition	43	■ Digital Attenuator A description was added. Figure 43 was added.
			59	■ Register Definitions A description was added.
14/09/29	04	Error Correction	30	■ Differential / Single-End Input selection "L/RIN1-2 pins" → "L/RIN1-/2- pins"
15/06/11	05	Error Correction	15-18	SWITCHING CHARACTERISTICS TDM512 mode: TDM0 bit = "0", TDM1 bit = "1" →TDM1 bit = "0", TDM0 bit = "1" TDM256 mode: TDM0 bit = "1", TDM1 bit = "0" →TDM1 bit = "1", TDM0 bit = "0"
			33	■ Audio Serial Interface Format (2) TDM Mode TDM256 mode (fs = 48kHz) → (fs= 96kHz)
			56	■ Register Definitions Table for TDM1-0 bits is corrected. Mode 2: TDM1 "1", TDM0 "1" → TDM1 "1", TDM0 "0" Mode 3: TDM1 "1", TDM0 "0" → TDM1 "1", TDM0 "1"

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