

SN54BCT543, SN74BCT543 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS026C – NOVEMBER 1988 – REVISED APRIL 1994

- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- 3-State True Outputs
- Back-to-Back Registers for Storage
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include Plastic Small-Outline Packages (DW), Ceramic Chip Carriers (FK) and Flatpacks (W), and Plastic and Ceramic 300-mil DIPs (JT, NT)

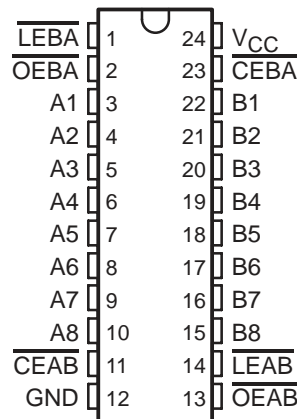
description

The 'BCT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (\overline{LEAB} or \overline{LEBA}) and output-enable (\overline{OEAB} or \overline{OEBA}) inputs are provided for each register to permit independent control in either direction of data flow.

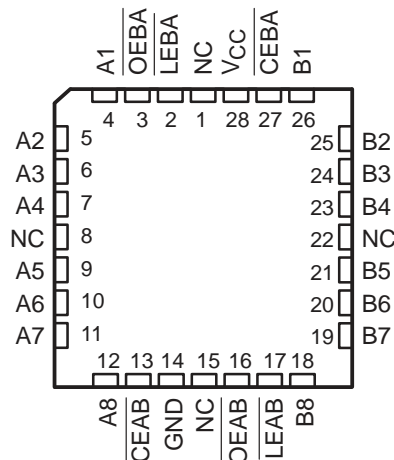
The A-to-B enable (\overline{CEAB}) input must be low in order to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs.

The SN54BCT543 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74BCT543 is characterized for operation from 0°C to 70°C .

SN54BCT543 . . . JT OR W PACKAGE
SN74BCT543 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54BCT543 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE†

INPUTS				OUTPUT
\overline{CEAB}	\overline{LEAB}	\overline{OEAB}	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0^{\ddagger}
L	L	L	L	L
L	L	L	H	H

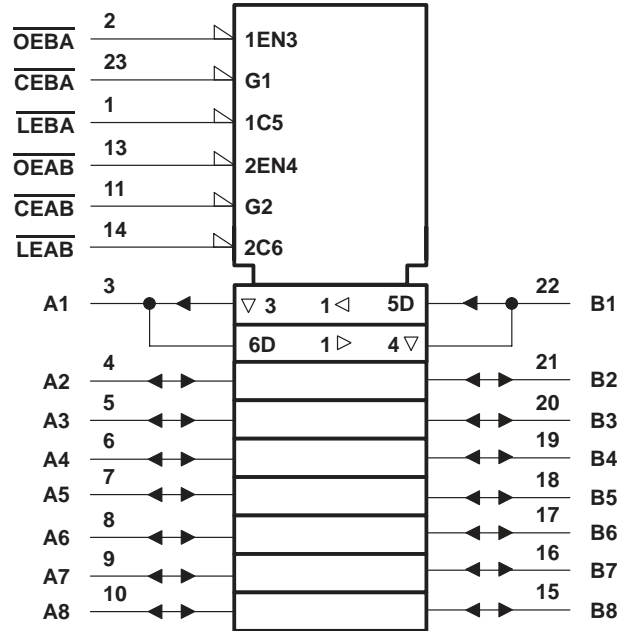
† A-to-B data flow is shown; B-to-A flow control is the same except that it uses \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .

‡ Output level before the indicated steady-state input conditions were established.

SN54BCT543, SN74BCT543 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

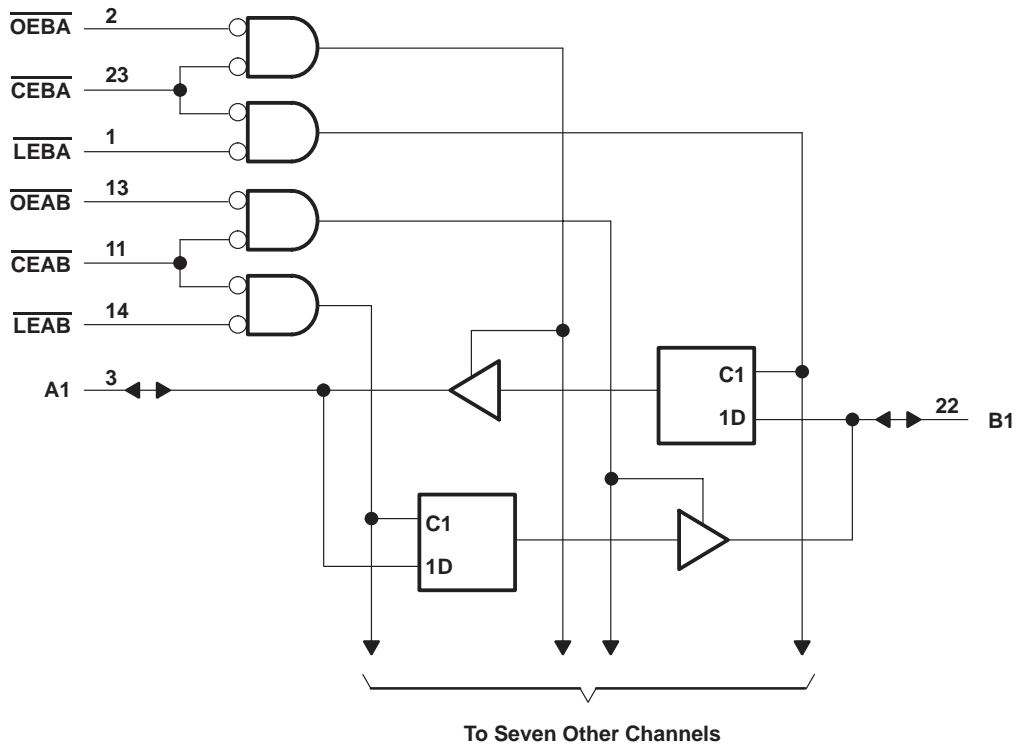
SCBS026C – NOVEMBER 1988 – REVISED APRIL 1994

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, NT, and W packages.

SN54BCT543, SN74BCT543 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS026C – NOVEMBER 1988 – REVISED APRIL 1994

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	– 0.5 V to 7 V
Input voltage range: Control inputs (see Note 1)	– 0.5 V to 7 V
I/O ports (see Note 1)	– 0.5 V to 5.5 V
Voltage range applied to any output in the disabled or power-off state, V_O	– 0.5 V to 7 V
Voltage range applied to any output in the high state, V_O	– 0.5 V to V_{CC}
Input clamp current, I_{IK}	–30 mA
Current into any output in the low state: SN54BCT543	96 mA
SN74BCT543	128 mA
Operating free-air temperature range: SN54BCT543	– 55°C to 125°C
SN74BCT543	0°C to 70°C
Storage temperature range	– 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		SN54BCT543			SN74BCT543			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			–18			–18	mA
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	–55		125	0		70	°C



SN54BCT543, SN74BCT543 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS026C – NOVEMBER 1988 – REVISED APRIL 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT543		SN74BCT543		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$				-1.2		V	
V_{OH}	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.3	2.4	3.3	V	
		$I_{OH} = -12\text{ mA}$	2	3.2				
		$I_{OH} = -15\text{ mA}$			2	3.1		
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$	0.38 0.55				V	
		$I_{OL} = 64\text{ mA}$			0.42	0.55		
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$				0.4		mA	
I_{IH}^\ddagger	A or B port	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$			70		μA	
	Control input				20			
I_{IL}^\ddagger	A or B port	$V_{CC} = 5.5\text{ V}$, $V_I = 0.5\text{ V}$			-0.65		mA	
	Control input				-0.6			
I_{OS}^\S	$V_{CC} = 5.5\text{ V}$, $V_O = 0$		-100	-225	-100	-225	mA	
I_{CCL}	A or B port	$V_{CC} = 5.5\text{ V}$		45	71	45	71	mA
I_{CCH}	A or B port	$V_{CC} = 5.5\text{ V}$		5	8	5	8	mA
I_{CCZ}	A or B port	$V_{CC} = 5.5\text{ V}$		9	15	9	15	mA
C_i	Control input	$V_{CC} = 5\text{ V}$, $V_I = 2.5\text{ V}$ or 0.5 V		6		6		pF
C_{io}	A or B port	$V_{CC} = 5\text{ V}$, $V_O = 2.5\text{ V}$ or 0.5 V		16		16		pF

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		SN54BCT543		SN74BCT543		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, \overline{LEAB} or \overline{LEBA} low	7		8		7		ns
t_{su}	Setup time, data before \overline{LEAB} or $\overline{LEBA}\uparrow$	4.5		5.5		4.5		ns
t_h	Hold time, data after \overline{LEAB} or $\overline{LEBA}\uparrow$	1.5		1.5		1.5		ns

SN54BCT543, SN74BCT543 OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS026C – NOVEMBER 1988 – REVISED APRIL 1994

switching characteristics (see Note 2)

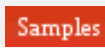

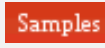

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†				UNIT
			'BCT543			SN54BCT543		SN74BCT543		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	B or A	2	5.7	7.5	2	9.9	2	8.8	ns
t _{PHL}			2	6.3	8.2	2	9.7	2	9.6	
t _{PLH}	\overline{LE}	A or B	2	8.2	10.3	2	13.9	2	12.9	ns
t _{PHL}			2	8.5	10.6	2	13.2	2	12.7	
t _{PZH}	\overline{OE}	A or B	1	6.8	8.6	1	11.4	1	10.7	ns
t _{PZL}			1	8.7	10.8	1	12.8	1	12.3	
t _{PHZ}	\overline{OE}	A or B	1	5.5	7.2	1	8.8	1	8.1	ns
t _{PLZ}			1	4.7	6.4	1	8.1	1	7.2	
t _{PZH}	\overline{CE}	A or B	1	7.6	9.8	1	12.8	1	12	ns
t _{PZL}			1	9.5	11.6	1	13.8	1	13.5	
t _{PHZ}	\overline{CE}	A or B	1	5.8	7.5	1	9.3	1	8.5	ns
t _{PLZ}			1	4.8	6.7	1	8.4	1	7.6	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9087001M3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9087001M3A SNJ54BCT 543FK	
SN74BCT543DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT543	
SNJ54BCT543FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9087001M3A SNJ54BCT 543FK	
SNJ54BCT543JT	ACTIVE	CDIP	JT	24	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9087001ML A SNJ54BCT543JT	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54BCT543, SN74BCT543 :

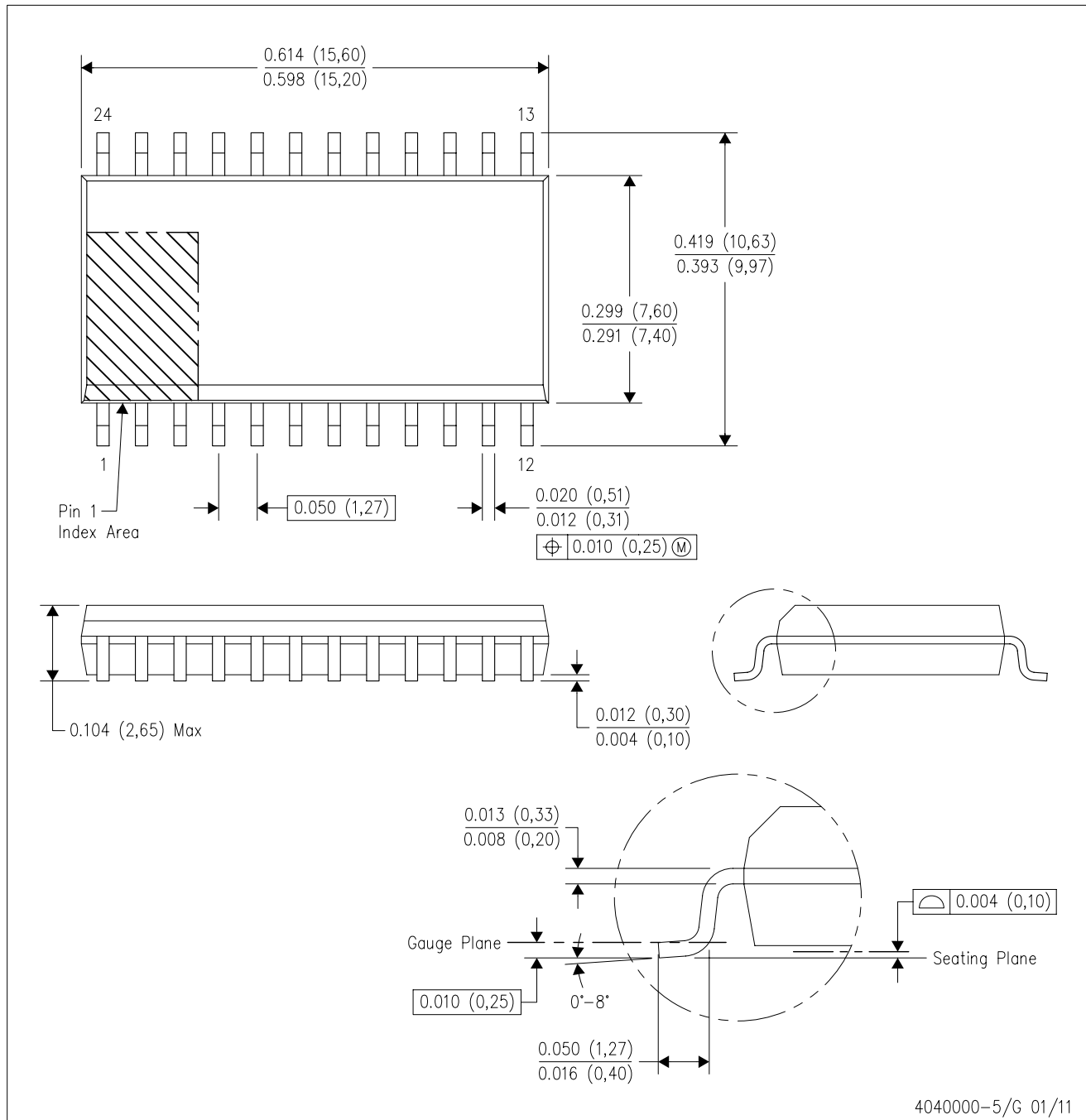
- Catalog: [SN74BCT543](#)
- Military: [SN54BCT543](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

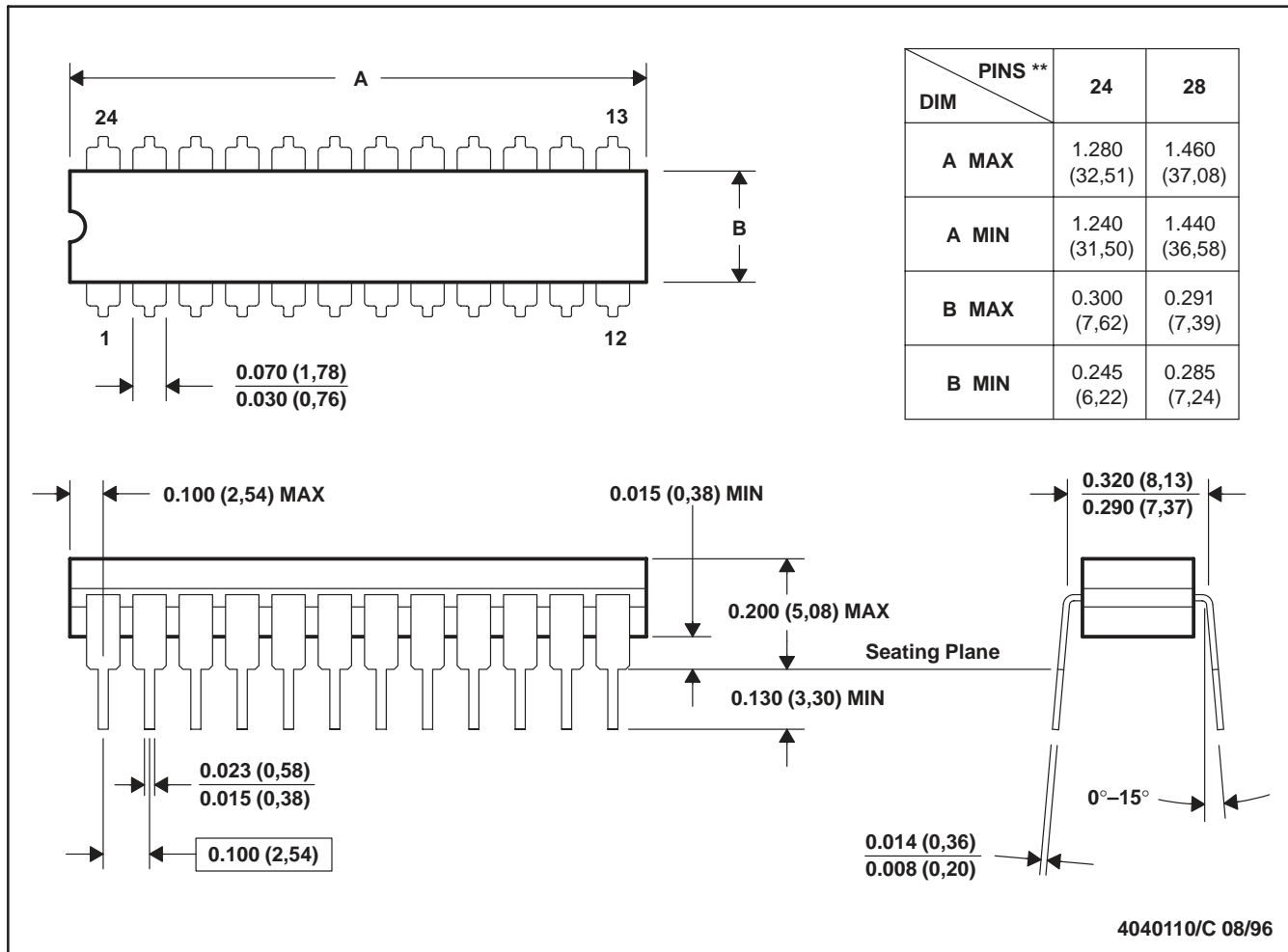


- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated