

# Linear Single Cell Li-Ion Battery Charger IC

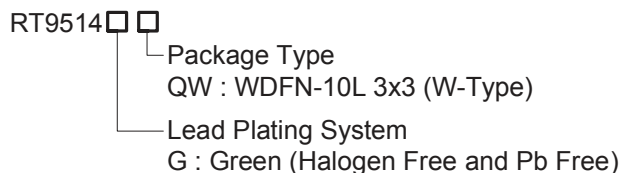
## General Description

The RT9514 is a fully integrated low cost single-cell Li-Ion battery charger IC ideal for portable applications. The RT9514 is capable of being powered up from AC adapter. The RT9514 enters sleep mode when AC adapter is removed.

The RT9514 optimizes the charging task by using a control algorithm including preconditioning mode, fast charge mode and constant voltage mode. The charging task is terminated as the charge current drops below the preset threshold. The AC adapter charge current can be programmed up to 1A with an external resistor. The internal thermal feedback circuitry regulates the die temperature to optimize the charge rate for all ambient temperatures.

The RT9514 features 18V maximum rating voltages for AC adapter. The other features are under voltage protection, over voltage protection for AC adapter supply.

## Ordering Information



Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

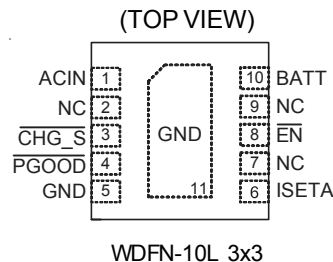
## Features

- 18V Maximum Rating for AC Adapter
- Internal Integrate P-MOSFETs
- AC Adapter Power Good Status Indicator
- Charge Status Indicator
- Under Voltage Protection
- Over Voltage Protection
- Automatic Recharge Feature
- Small 10-Lead WDFN Package
- Thermal Feedback Optimizing Charge Rate
- RoHS Compliant and Halogen Free

## Applications

- Digital Cameras
- Cellular Phones
- Personal Data Assistants (PDAs)
- MP3 Players
- Handheld PCs

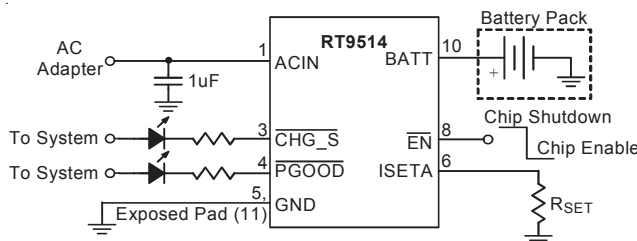
## Pin Configurations



## Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

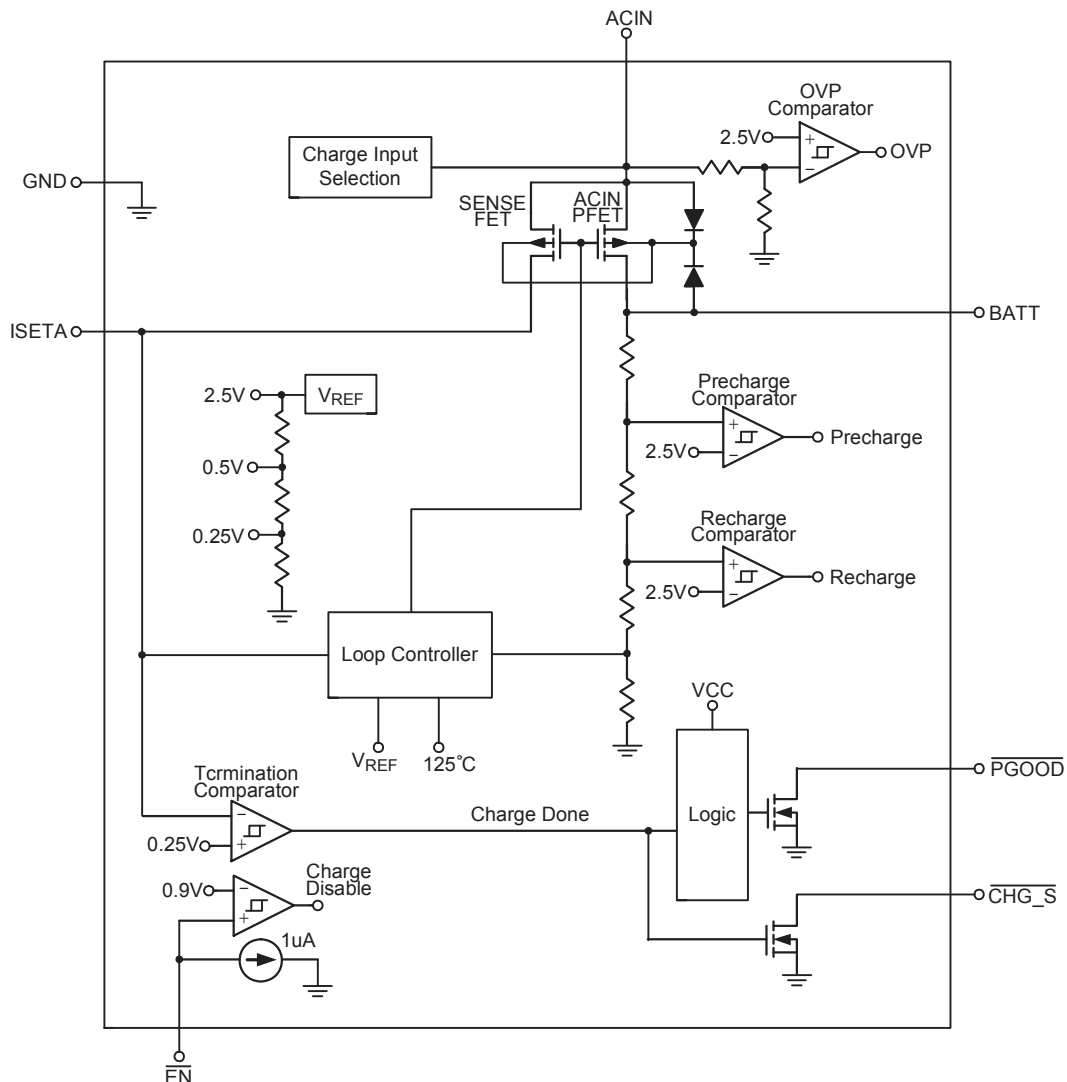
## Typical Application Circuit

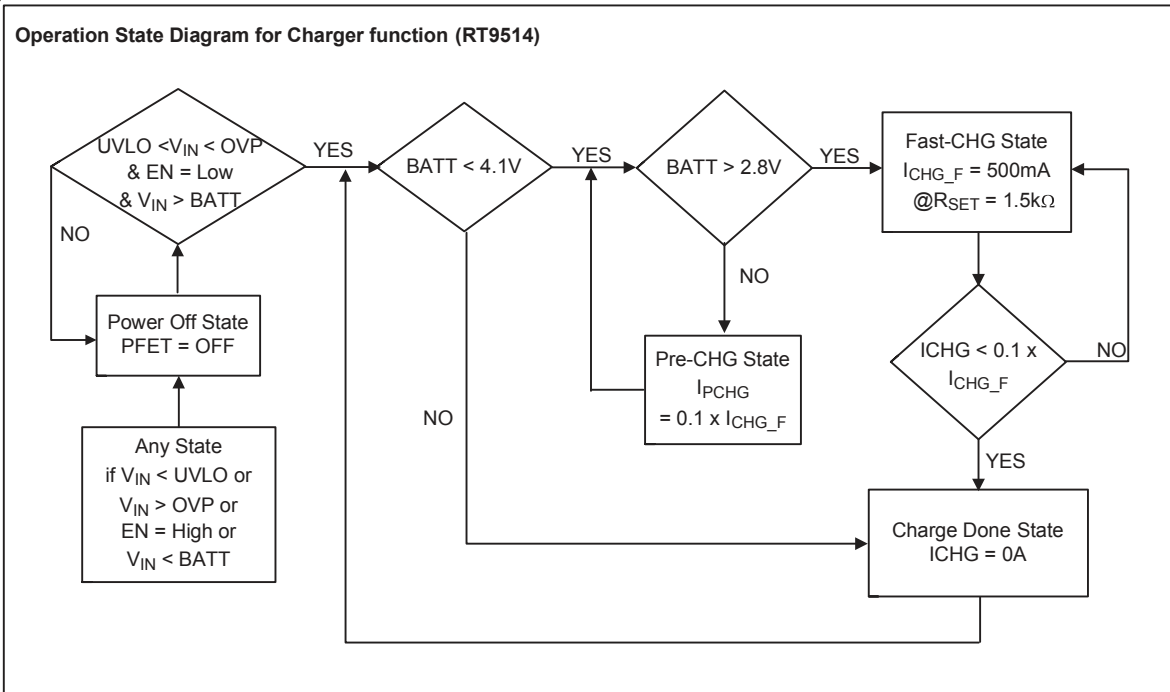


Functional Pin Description

Pin No.	Pin Name	Pin Function
1	ACIN	Wall Adaptor Charge Input Supply.
2, 7, 9	NC	No Internal Connection.
3	CHG_S	Charge Status Indicator Output (open drain).
4	PGOOD	Power Good Indicator Output (open drain).
5	GND	Ground.
6	ISETA	Wall Adaptor Supply Charge Current Set Point.
8	EN	Charge Enable Input (active low).
10	BATT	Battery Charge Current Output.
11 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram





## Absolute Maximum Ratings (Note 1)

- AC Input Voltage ----- -0.3V to 18V
- $\overline{\text{EN}}$  Input Voltage ----- -0.3V to 6V
- Output Current ----- 1.2A
- Power Dissipation,  $P_D$  @  $T_A = 25^\circ\text{C}$   
 WDFN-10L 3x3 ----- 1.667W
- Package Thermal Resistance (Note 2)  
 WDFN-10L 3x3,  $\theta_{JA}$  -----  $60^\circ\text{C/W}$   
 WDFN-10L 3x3,  $\theta_{JC}$  -----  $8.2^\circ\text{C/W}$
- Lead Temperature (Soldering, 10 sec.) -----  $260^\circ\text{C}$
- Junction Temperature -----  $150^\circ\text{C}$
- Storage Temperature Range -----  $-65^\circ\text{C}$  to  $150^\circ\text{C}$
- ESD Susceptibility (Note 3)  
 HBM (Human Body Mode) ----- 2kV  
 MM (Machine Mode) ----- 200V

## Recommended Operating Conditions (Note 4)

- ACIN Input Voltage Range ----- 4.5V to 6V
- Junction Temperature Range -----  $-40^\circ\text{C}$  to  $125^\circ\text{C}$
- Ambient Temperature Range -----  $-40^\circ\text{C}$  to  $85^\circ\text{C}$

## Electrical Characteristics

(ACIN = 5V,  $T_A = 25^\circ\text{C}$ , Unless Otherwise specification)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>Supply Input</b>						
ACIN UVLO Threshold Voltage	$V_{UVLO}$	Rising	--	3	3.5	V
ACIN UVLO Hysteresis	$V_{UVLO\_Hys}$		50	80	120	mV
ACIN Standby Current	$I_{STBY}$	$V_{BATT} = 4.5V$	--	300	500	$\mu\text{A}$
ACIN Shutdown Current	$I_{SHDN}$	$V_{\overline{\text{EN}}} = \text{High}$	--	50	100	$\mu\text{A}$
ACIN Quiescent Current	$I_Q$	$V_{ACIN} = 4V, V_{BATT} = 3V$	--	150	250	$\mu\text{A}$
BATT Sleep Leakage Current	$I_{SLEEP}$	$V_{ACIN} = 4V, V_{BATT} = 4.5V$	--	--	10	$\mu\text{A}$
<b>Voltage Regulation</b>						
BATT Regulation Voltage	$V_{REG}$	$I_{BATT} = 60\text{mA}$	4.168	4.21	4.252	V
Regulation Voltage Accuracy			-1	--	+1	%
ACIN MOSFET	$R_{DS(ON)\_ACIN}$	$I_{BATT} = 500\text{mA}$	--	600	--	$\text{m}\Omega$
<b>Current Regulation</b>						
ISETA Set Voltage (Fast Charge Phase)	$V_{ISETA}$	$V_{BATT} = 3.5V$	2.45	2.5	2.55	V
Full Charge Setting Range	$I_{CHG\_F}$		100	--	1200	mA
AC Charge Current accuracy	$I_{CHG\_F}$	$V_{BATT} = 3.8V, R_{ISET} = 1.5\text{k}\Omega$	--	500	--	mA

*To be continued*

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>Precharge</b>						
BATT Pre-Charge Rising Threshold	V <sub>PRECH</sub>		2.6	2.8	3	V
BATT Pre-Charge Threshold Hysteresis	ΔV <sub>PRECH</sub>		50	100	200	mV
Pre-Charge Current	I <sub>PCHG</sub>	V <sub>BATT</sub> = 2V	8	10	12	%
<b>Recharge Threshold</b>						
BATT Re-Charge Falling Threshold Hysteresis	ΔV <sub>RECH_L</sub>	V <sub>REG</sub> - V <sub>BATT</sub>	60	100	170	mV
<b>Charge Termination Detection</b>						
Termination Current Ratio (default)	I <sub>TERM</sub>	V <sub>BATT</sub> = 4.2V	--	10	--	%
<b>Logic Input/Output</b>						
CHG_S Pull Down Voltage	V <sub>CHG_S</sub>	TBD, I <sub>CHG_S</sub> = 5mA	--	65	--	mV
PGOOD Pull Down Voltage	V <sub>PGOOD</sub>	TBD, I <sub>PGOOD</sub> = 5mA	--	220	--	mV
EN Threshold	Logic-High Voltage	V <sub>IH</sub>	1.5	--	--	V
	Logic-Low Voltage	V <sub>IL</sub>	--	--	0.4	V
EN Pin Input Current	I <sub>EN</sub>	V <sub>EN</sub> = 2V	--	--	2	uA
<b>Protection</b>						
Thermal Regulation			--	125	--	°C
OVP SET		Internal Default	--	6.5	--	V

**Note 1.** Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

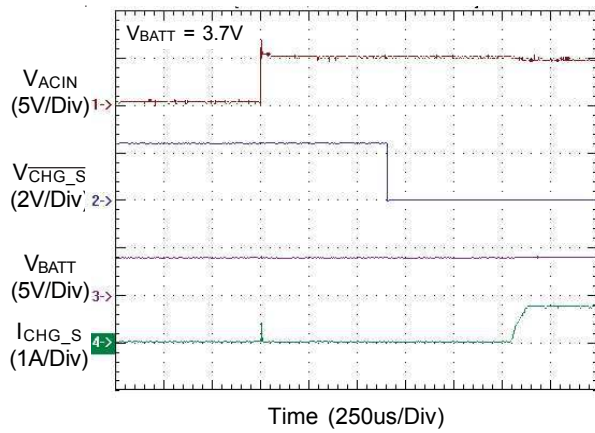
**Note 2.** θ<sub>JA</sub> is measured in the natural convection at T<sub>A</sub> = 25°C on a high effective thermal conductivity test board (4 layers, 2S2P) of JEDEC 51-7 thermal measurement standard. The case point of θ<sub>JC</sub> is on the expose pad for the package.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

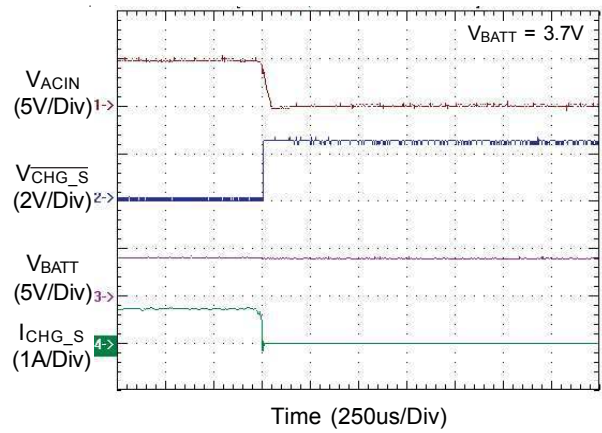
**Note 4.** The device is not guaranteed to function outside its operating conditions.

## Typical Operating Characteristics

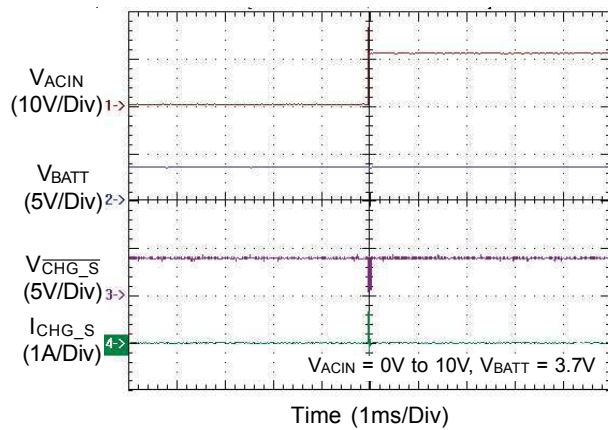
### ACIN Power On



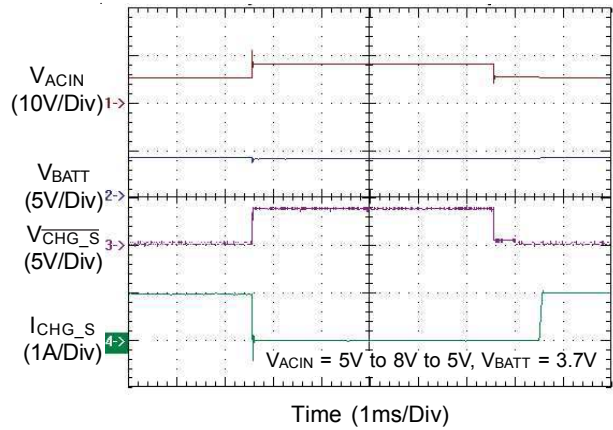
### ACIN Power Off



### ACIN OVP



### ACIN OVP



## Application Information

### Automatically Power Source Selection

The RT9514 is a battery charger IC which is designed for Li-ion Battery with 4.21V rated voltage.

AC Mode : When the AC input voltage (ACIN) is higher than the UVP voltage level and lower than the OVP protection (3V), the RT9514 will enter AC Mode. In the AC Mode, ACIN P-MOSFET is turned on.

Sleep Mode : The RT9514 will enter Sleep Mode when AC input voltage are removed. This feature provides low leakage current from the battery during the absence of input supply.

### ACIN Over Voltage Protection

The AC input voltage is monitored by an internal OVP comparator. The comparator has an accurate reference of 2.5V from the band-gap reference. The OVP threshold is set by the internal resistive. The protection threshold is set to 6.5V. When the input voltage exceeds the threshold, the comparator outputs a logic signal to turn off the power P-MOSFET to prevent the high input voltage from damaging the electronics in the handheld system. When the input over oltage condition is removed (ACIN < 6V), the comparator re-enables the output by running through the soft-start.

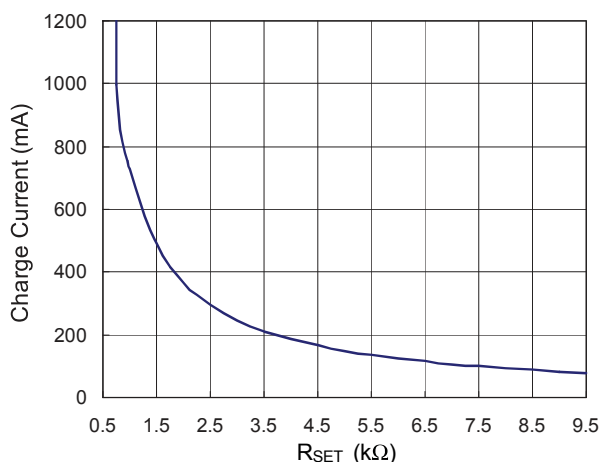


Figure 1. Charge Current Setting

### Fast-Charge Current Setting

The RT9514 offers ISETA pin to determine the charge current from 100mA to 1.2A. The charge current can be calculated as following equation.

$$I_{CHG\_F} = K \frac{V_{ISETA}}{R_{SET}}$$

The parameter K = 300 ; V<sub>ISETA</sub> = 2.5V (typ.). R<sub>SET</sub> is the resistor connected between the ISETA and GND.

### Pre- Charge Current Setting

During a charge cycle if the battery voltage is below the VPRECH threshold, the RT9514 applies a pre-charge mode to the battery. This feature revives deeply discharged cells and protects battery life. The RT9514 internally determines the pre-charge rate as 10% of the fast-charge current.

### Battery Voltage Regulation

The RT9514 monitors the battery voltage through the BATT pin. Once the battery voltage level closes to the VREG threshold, the RT9514 voltage enters constant phase and the charging current begins to taper down. When battery voltage is over the VREG threshold, the RT9514 will stop charge and keep to monitor the battery voltage. However, when the battery voltage decreases 100mV below the V<sub>REG</sub>, it will be recharged to keep the battery voltage.

### Charge Status Outputs

The open-drain  $\overline{CHG\_S}$  and  $\overline{PGOOD}$  outputs indicate various charger operations as shown in the following table.

These status pins can be used to drive LEDs or communicate to the host processor. Note that ON indicates the open-drain transistor is turned on and LED is bright.

Charge State		$\overline{CHG\_S}$	$\overline{PGOOD}$
ACIN	Charge	ON	ON
	Charge done	OFF	ON

### Temperature Regulation

In order to maximize the charge rate, the RT9514 features a junction temperature regulation loop. If the power dissipation of the IC results in a junction temperature greater than the thermal regulation threshold (125°C), the RT9514 throttles back on the charge current in order to maintain a junction temperature around the thermal regulation threshold (125°C). The RT9514 monitors the junction temperature,  $T_J$ , of the die and disconnects the battery from the input if  $T_J$  exceeds 125°C. This operation continues until junction temperature falls below thermal regulation threshold (125°C) by the hysteresis level. This feature prevents the chip from damaging.

### Selecting the Input and Output Capacitors

In most applications, the most important is the high-frequency decoupling capacitor on the input of the RT9514. A 1uF ceramic capacitor, placed in close proximity to input pin and GND pin is recommended. In some applications depending on the power supply characteristics and cable length, it may be necessary to add an additional 10uF ceramic capacitor to the input. The RT9514 requires a small output capacitor for loop stability. A 1uF ceramic capacitor placed between the BATT pin and GND is typically sufficient.

### Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where  $T_{J(MAX)}$  is the maximum operation junction temperature 125°C,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance.

For recommended operating conditions specification, where  $T_{J(MAX)}$  is the maximum junction temperature of the die (125°C) and  $T_A$  is the ambient temperature. The junction to ambient thermal resistance  $\theta_{JA}$  is layout dependent. For WDFN-10L 3x3 packages, the thermal resistance  $\theta_{JA}$  is 60°C/W on the standard JEDEC 51-7 four layers thermal

test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (60^\circ\text{C/W}) = 1.667\text{W for WDFN-10L 3x3 packages}$$

The maximum power dissipation depends on operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal resistance  $\theta_{JA}$ . For WDFN-10L 3x3 package, the Figure 2 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

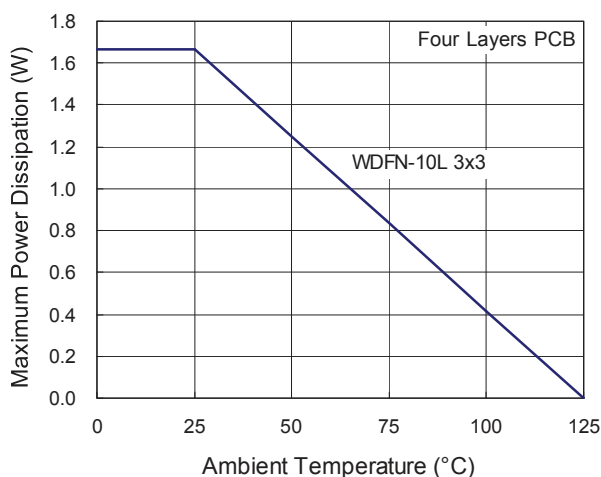


Figure 2. Derating Curves for RT9514 Package

### Layout Considerations

For the best performance of the RT9514, the following PCB layout guidelines must be strictly followed.

- ▶ Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- ▶ Keep the main power traces as wide and short as possible.
- ▶ The connection of  $R_{SETA}$  should be isolated from other noisy traces. The short wire is recommended to prevent EMI and noise coupling.
- ▶ Connect the GND and Exposed Pad to a strong ground plane for maximum thermal dissipation and noise protection.



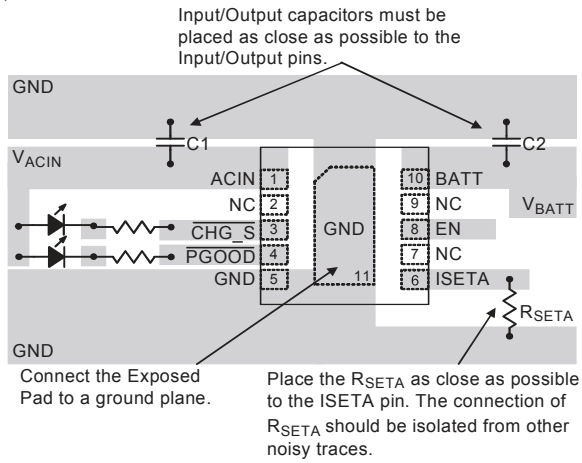
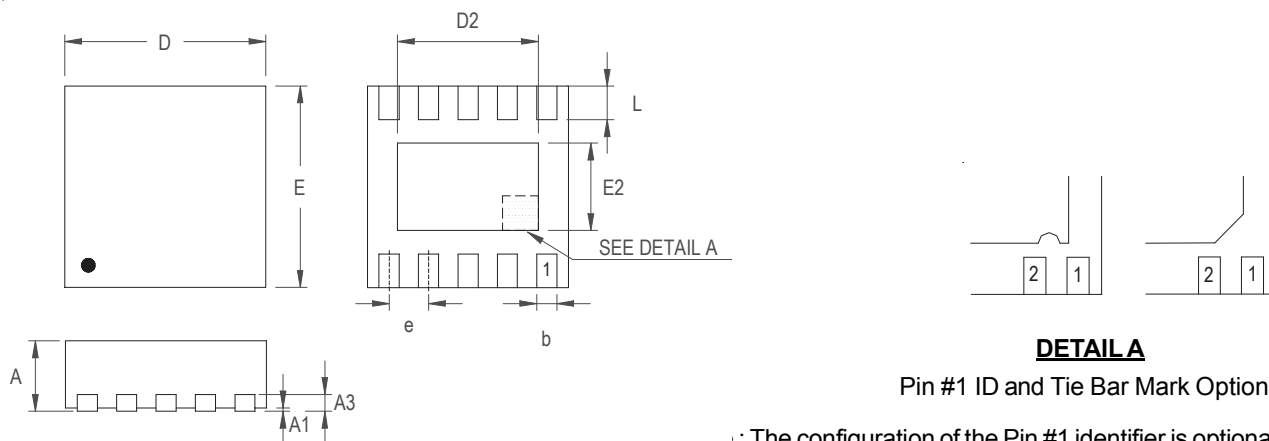


Figure 3. PCB Layout Guide

## Outline Dimension



### DETAIL A

Pin #1 ID and Tie Bar Mark Options

The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

### Richtek Technology Corporation

Headquarter

5F, No. 20, Taiyuen Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789 Fax: (8863)5526611

### Richtek Technology Corporation

Taipei Office (Marketing)

5F, No. 95, Minchiuan Road, Hsintien City

Taipei County, Taiwan, R.O.C.

Tel: (8862)86672399 Fax: (8862)86672377

Email: [marketing@richtek.com](mailto:marketing@richtek.com)

Information that is provided by Richtek Technology Corporation is believed to be accurate and reliable. Richtek reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. No third party intellectual property infringement of the applications should be guaranteed by users when integrating Richtek products into any application. No legal responsibility for any said applications is assumed by Richtek.