

November 2021

### GENERAL DESCRIPTION

The HI-485x devices are slew-rated controlled TIA-485/TIA-422-B and ISO 8482:1993 compliant transceivers with extended power-supply, temperature and receiver common-mode range for avionic and industrial control applications. The devices can operate over an extended supply (3.0V to 5.5V) and temperature (-55°C to 125°C) range. The receiver input common-mode range of [-15, 20]V, and  $\pm 24V$  for the half and full duplex configurations respectively is valid over the full supply and temperature specification. The HI-4850 has a half-duplex configuration, and the HI-4851 and HI-4852 are full-duplex. Slew rates are optimized for data rates below 5 Mbps. The drivers slew-rate control and pre-emphasis reduces high-frequency components in the output signal transitions and also compensates for impedance mismatch. These features provide optimum EMI and jitter performance, essential in EMI sensitive environments and high-integrity data link applications such as in aerospace and industrial controls.

The devices deliver at least  $\pm 1.50V$  (VDD=3.0V), and  $\pm 2.45V$  (VDD= 4.5V) output levels at an extended temperature range of -55°C to +125°C into a differential load of 54 $\Omega$  and 50pF.

The receiver offers true Fail-Safe operation, providing a guaranteed logic high on RO when the bus is open-circuit, short-circuit, or idle (terminated but not driven). The receiver's worst case minimum input resistance is at least 90K $\Omega$ , supporting up to 224 nodes

### APPLICATIONS

- Extended Temperature Range RS-485/422 Networks
- Process Control and Factory Automation
- EMI Emission Sensitive Avionics
- Industrial Field Bus Networks
- Networks requiring extended common-mode range

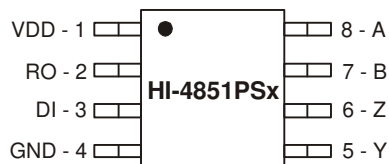
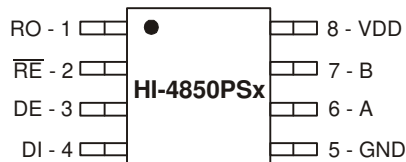
Device Selection Table			
Part Number	Half/Full Duplex	Data Rate (Mbps)*	Package
HI-4850	Half	$\leq 5.0$	8-pin SOIC
HI-4851	Full	$\leq 5.0$	8-pin SOIC
HI-4852	Full	$\leq 5.0$	14-pin SOIC 16-pin QFN

\* For RS-485 Transceivers optimized for data rates up to 20Mbps please refer to the HI-4853 data sheet.

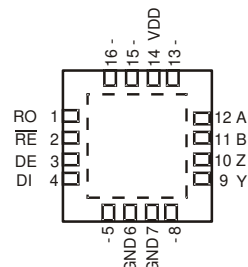
### FEATURES

- Slew Rate Control and Pre-Emphasis for superior EMI
- Extended Power Supply Operating Range 3.0V to 5.5V
- Extended Receiver Common-Mode Range:
  - **-15.0V to 20.0V Half-Duplex**
  - **$\pm 24V$  Full-Duplex**
- ESD Protection
  - 16KV HBM (Bus Pins)
  - 8KV HBM (Logic Pins)
- 5 Mbps Data Rate up to 100 ft. CAT-5 UTP
- 2 Mbps Data Rate up to 1000 ft. CAT-5 UTP
- Current Limiting Protection
- Extended Temperature Range -55°C to 125°C
- Industry Standard 75176 Pin-out

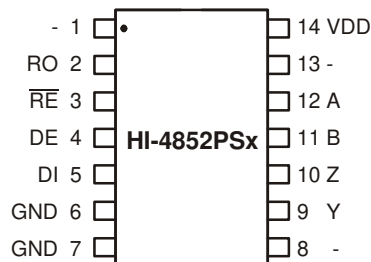
### PIN CONFIGURATIONS (Top Views)



8-Pin Plastic SOIC package (Narrow Body)



HI-4852PCx  
16-pin 4mm x 4mm QFN



14-Pin Plastic SOIC package (Narrow Body)

# PIN DESCRIPTIONS

SIGNAL	FUNCTION	DESCRIPTION
RO	OUTPUT	Receiver Output. If $V_{ID} \geq -50\text{mV}$ , then RO is high. If $V_{ID} < -150\text{mV}$ then RO is low. If the bus is shorted, open or terminated but not driven by another terminal, RO will be high.
$\overline{\text{RE}}$	INPUT	Receiver Enable. $\overline{\text{RE}} = \text{Low}$ enables the receiver. $\overline{\text{RE}} = \text{High}$ forces the receiver output (RO) into a high impedance state. Internal 450K $\Omega$ pull-down resistor
DE	INPUT	Driver Enable. DE = high enables the driver. DE = low will force the driver output into a high impedance state and the device will function as a line receiver if $\overline{\text{RE}}$ is also low. Internal 450K $\Omega$ pull-up resistor
DI	INPUT	Driver Input. Forces the logic state of the Driver's output, if Driver is enabled. Internal 450K $\Omega$ pull-up resistor
GND	POWER	Chip ground, 0V Supply
A, Y	ANALOG I/O	Non-inverting Receiver Input / Driver Output.
B, Z	ANALOG I/O	Inverting Receiver Input / Driver Output.
VDD	POWER	Positive Supply: $3.0\text{V} \leq \text{VDD} \leq 5.5\text{V}$

## TX FUNCTION TABLE

TRANSMITTING					
INPUTS			LINE CONDITION	OUTPUTS	
$\overline{\text{RE}}$	DE	DI		B	A
X	1	1	Transmit logic high	0	1
X	1	0	Transmit logic low	1	0
0	0	X	Disable	Hi-Z	Hi-Z
1	0	X	Shutdown	Hi-Z	Hi-Z

## RX FUNCTION TABLE

RECEIVING				
INPUTS		BUS PINS $V_{ID} = V_A - V_B$	OUTPUT RO	OPERATION
$\overline{\text{RE}}$	DE			
0	0	$-150\text{mV} < V_{ID} < -50\text{mV}$	X	Undefined Input
0	X	$-50\text{mV} \leq V_{ID}$	1	Receiver logic high
0	X	$V_{ID} \leq -150\text{mV}$	0	Receiver logic low
0	0	Open or Shorted	1	Default
0	0	Idle and terminated	1	Default
1	1	X	Hi-Z	Disabled
1	0	X	Hi-Z	Shutdown

## Typical Operating Circuit

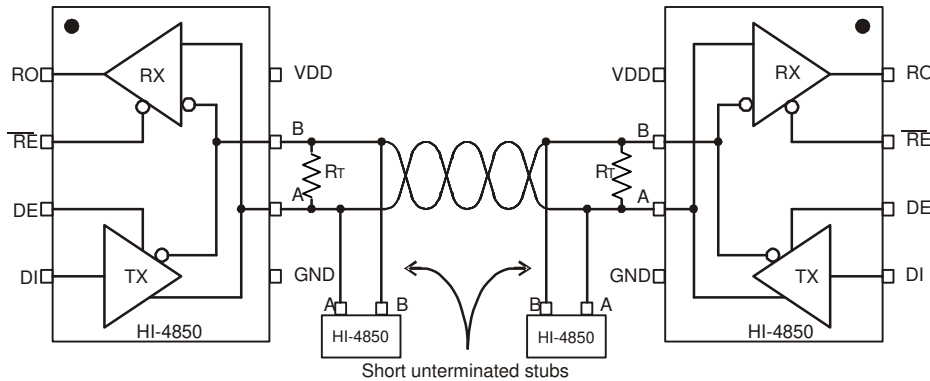


Figure 1 - Typical half-duplex configuration

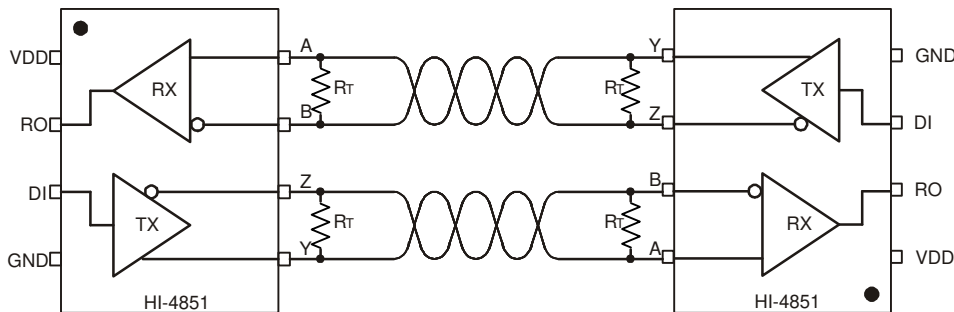


Figure 2 - Typical full-duplex 8-pin configuration

## ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND = 0V)

Supply Voltage, VDD:.....7 V	Operating Temperature Range:(Industrial).....-40°C to +85°C (Hi-Temp).....-55°C to +125°C
Control Input Currents: .....-100mA to 100mA	
Digital Input Voltages (DI, DE, RE):.....-0.5V to VDD + 0.5V	
Bus Voltage (AY, BZ):.....±25V	Internal Power Dissipation:.....900mW
Digital Output Voltage (RO):.....-0.5V to V + 0.5V	Storage Temperature Range: .....-65°C to +150°C
Short-Circuit Duration, Driver (V: ±15V).....∞	
ESD (Human Body Model): AY, BZ, VDD, GND pins:.....±16KV DI, DE, RE, RO pins:.....±8KV	Solder Temperature: (Reflow)..... +260°C

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## SPECIFIED OPERATING CONDITIONS

PARAMETERS	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Supply Voltage	V <sub>DD</sub>		3.0	3.3 / 5.0	5.5	V
Temperature	T		-55		125	°C
TX Common-Mode Bus Loading	V <sub>OCM</sub>	See Figure 4	-7		12	V
RX Input Common-Mode Voltage	V <sub>ICM</sub>	Half-Duplex	-16		20	V
Differential Load Resistance	R <sub>L</sub>		45	60	∞	Ω
Differential Load Capacitance	C <sub>L</sub>			100		pF
Digital Input High Voltage	V <sub>IH</sub>	DE, DI, RE	70			%V <sub>DD</sub>
Digital Input Low Voltage	V <sub>IL</sub>	DE, DI, RE			30	%V <sub>DD</sub>
Digital Input Current high	I <sub>IH</sub>	DE, DI, V <sub>IH</sub> = V <sub>DD</sub>			1	μA
Digital Input Pull-Down Current	I <sub>PD</sub>	RE, V <sub>IH</sub> = V <sub>DD</sub>	6		18	μA
Digital Input Current low	I <sub>IL</sub>	RE, V <sub>IH</sub> = 0	-1			μA
Digital Input Pull-Up Current	I <sub>PU</sub>	DE, DI, V <sub>IH</sub> = 0V	-18		-6	μA

## DRIVER DC ELECTRICAL CHARACTERISTICS

VDD = 3.0V to 3.6V or 4.5V to 5.5V; T = -55°C to 125°C; MIN and MAX values are at range boundaries

PARAMETER	SYMBOL	CONDITIONS	FIGURE	VDD = 3.3V ± 10%			VDD = 5.0V ± 10%			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Differential Output Voltage with no load	V <sub>OD1</sub>	R <sub>L</sub> = ∞	3	V <sub>DD</sub> - 0.1		V <sub>DD</sub>	V <sub>DD</sub> - 0.1		V <sub>DD</sub>	V
Differential Output Voltage into load with no common-mode voltage	V <sub>OD2</sub>	R <sub>L</sub> = 54Ω, C <sub>L</sub> = 50pF	3	1.5		3.0	2.45		4.0	V
Differential Output Voltage into load with applied common-mode voltage	V <sub>OD3</sub>	-7V ≤ V <sub>OCM</sub> ≤ 12V T <sub>A</sub> = 25°C	4	1.5		3.0	2.45		4.0	V
Differential Output Over/Under Shoot						5.5			3.2	%V <sub>OD</sub>
Change in Differential Output Voltage between logic states	ΔV <sub>OD</sub>	R <sub>L</sub> = 54Ω, C <sub>L</sub> = 50pF	3	-125		125	-125		125	mV
Output Common-Mode Voltage	V <sub>OCM</sub>	R <sub>L</sub> = 54Ω, C <sub>L</sub> = 50pF	4	1.40	1.60	2.0	2.15	2.45	3.0	V
Change in output Common-Mode Voltage between logic states	ΔV <sub>OCM</sub>	R <sub>L</sub> = 54Ω, C <sub>L</sub> = 50pF	4	-125		125	-150		150	mV
Bus Pin Leakage Current (High-Z Power On)	I <sub>OHZ1</sub>	DE=0, -15V ≤ V <sub>OCM</sub> ≤ 15V DE=0, -12V ≤ V <sub>OCM</sub> ≤ 15V		-200		200	-200		200	μA
Bus Pin Leakage Current (Power Off)	I <sub>OHZ2</sub>	V <sub>OCM</sub> = ±15V		-200		200	-200		200	μA
Peak Short Circuit Current	I <sub>SCP</sub>	DE = V <sub>DD</sub> , Bus Pin = ±15		-230		230	-250		250	mA
Steady State Short Circuit Current	I <sub>SC</sub>	DE = V <sub>DD</sub> , Bus Pin = ±15		0		50	0		50	μA
Differential Output Capacitance	C <sub>OD</sub>	DE = 0				16			16	pF
Static Supply Current	I <sub>DD</sub>	DE=V <sub>DD</sub> , RE=0, R <sub>L</sub> =∞			8	10		10	12	mA
Supply Current (Shutdown)	I <sub>DDQ</sub>	DE=0, RE=V <sub>DD</sub> , R <sub>L</sub> =∞			90	110		100	400	μA

## DRIVER SWITCHING CHARACTERISTICS

VDD = 3.0V - 3.6V or 4.5V - 5.5V as noted , Operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	FIGURE	VDD = 3.3V ± 10%			VDD = 5.0V ± 10%			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Low - to - High	t <sub>PDR</sub>	R <sub>L</sub> = 54Ω, C <sub>L</sub> =50pF	5 & 6	110	145	200	108	150	205	ns
Propagation Delay High - to - Low	t <sub>PDF</sub>	R <sub>L</sub> = 54Ω, C <sub>L</sub> =50pF	5 & 6	110	145	200	108	150	205	ns
Differential Rise Time	t <sub>r</sub>	R <sub>L</sub> = 54Ω, C <sub>L</sub> =50pF	5 & 6	90	105	120	115	135	155	ns
Differential Fall Time	t <sub>f</sub>	R <sub>L</sub> = 54Ω, C <sub>L</sub> =50pF	5 & 6	90	105	120	115	135	125	ns
Output Pulse Skew	t <sub>MSK</sub>	R <sub>L</sub> = 54Ω, C <sub>L</sub> =50pF	5 & 6		2	8		2	8	ns
Driver Enable to Output High	t <sub>ZH</sub>	R <sub>L</sub> = 500Ω, C <sub>L</sub> =50pF	7		95	120		90	117	ns
Driver Enable to output Low	t <sub>ZL</sub>	R <sub>L</sub> = 500Ω, C <sub>L</sub> =50pF	7		95	120		90	117	ns
Driver Disable from Output High	t <sub>HZ</sub>	R <sub>L</sub> = 500Ω, C <sub>L</sub> =50pF	7		20	33		18	30	ns
Driver Disable from Output Low	t <sub>LZ</sub>	R <sub>L</sub> = 500Ω, C <sub>L</sub> =50pF	7		20	33		18	30	ns
Shutdown to Active Output Delay	t <sub>ON</sub>	R <sub>L</sub> = 500Ω, C <sub>L</sub> =50pF	7			10			10	μs
Shutdown Delay	t <sub>OFF</sub>					10			10	μs

## RECEIVER DC ELECTRICAL CHARACTERISTICS

VDD = 3.0V - 3.6V or 4.5V - 5.5V as noted , Operating temperature range.

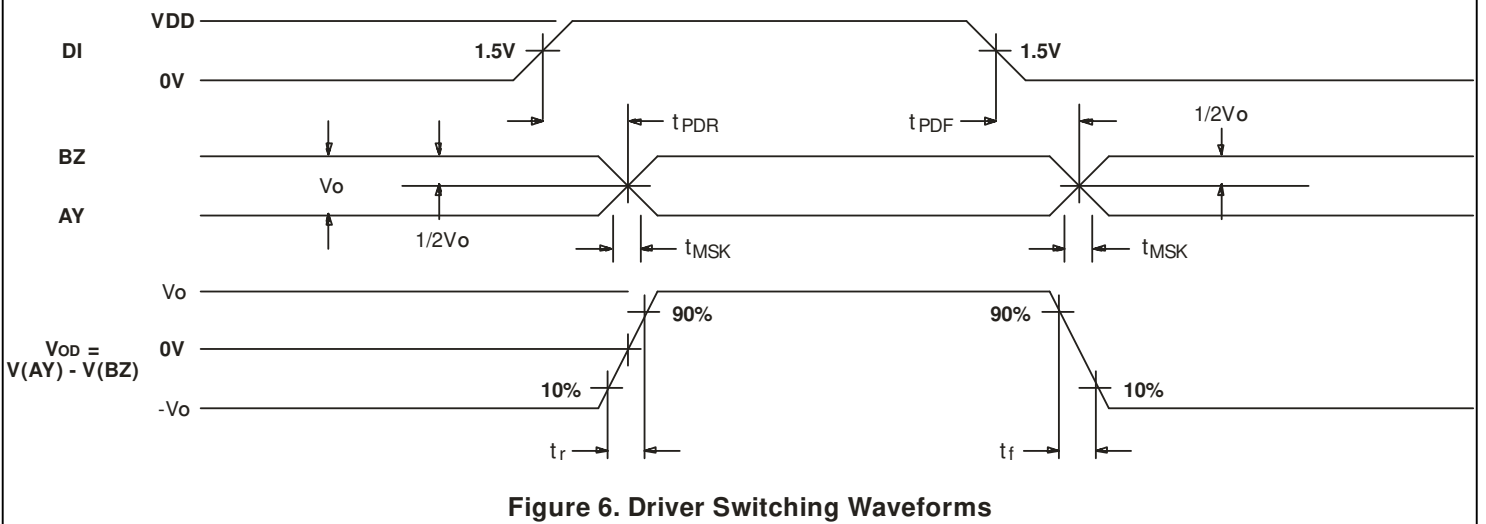
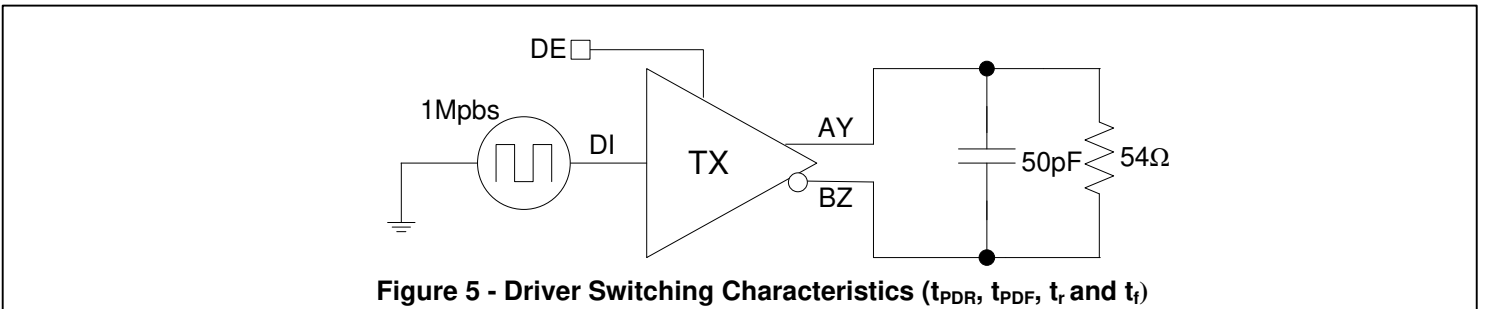
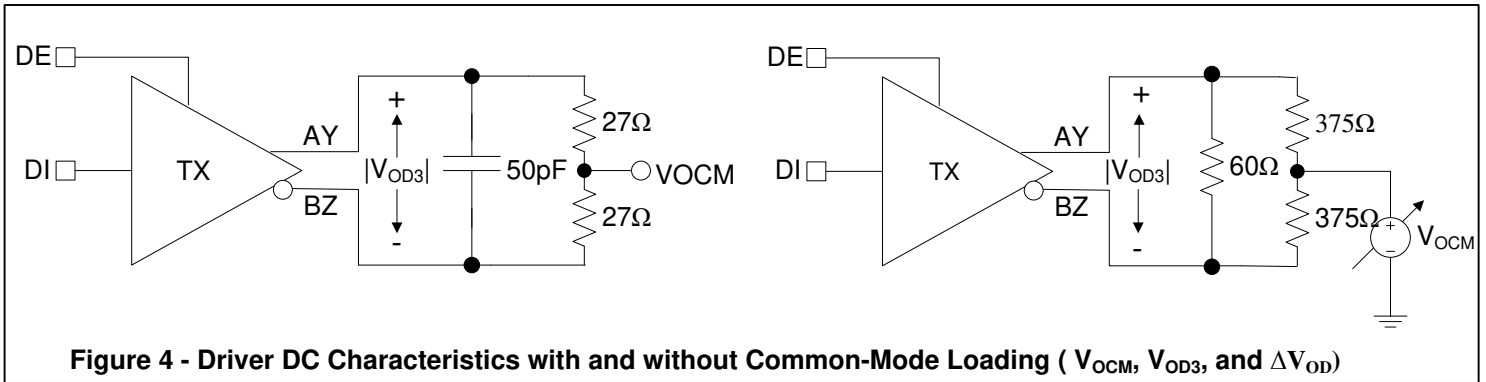
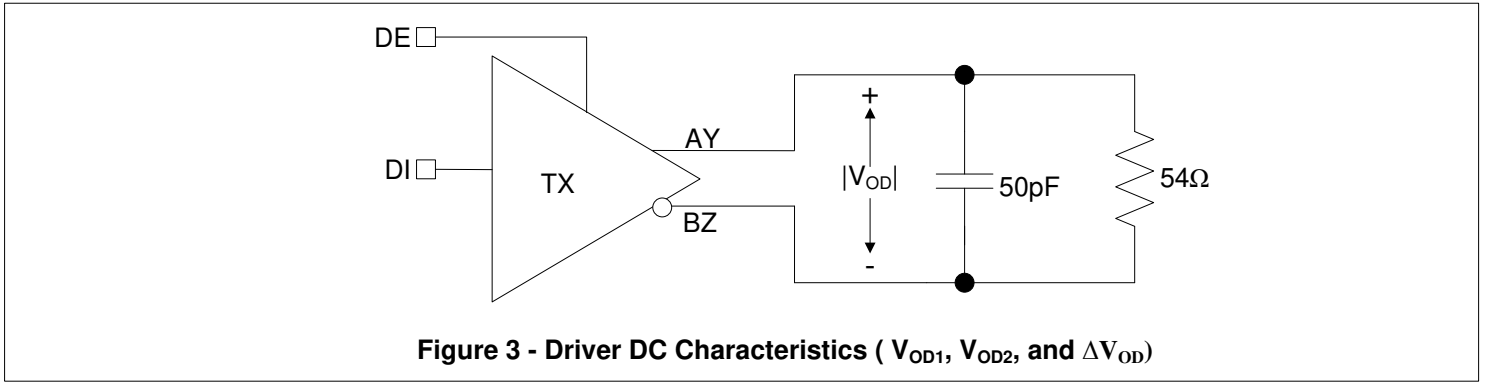
PARAMETER	SYMBOL	CONDITIONS	FIGURE	VDD = 3.3V ± 10%			VDD = 5.0V ± 10%			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input Threshold Voltage	V <sub>TH</sub>	-15 ≤ V <sub>ICM</sub> ≤ +20		-200	-100	-50	-200	-100	-50	mV mV
Input Hysteresis	V <sub>HYS</sub>	V <sub>ICM</sub> = 0V		17	28	33	17	28	33	mV
Input Resistance	R <sub>IN</sub>	-15 ≤ V <sub>ICM</sub> ≤ +20		80	92		80	92		KΩ KΩ
RO Output High Level	V <sub>OH</sub>	V <sub>ICM</sub> = +200mV I <sub>OUT</sub> = -3.0mA		90%			90%			V <sub>DD</sub>
RO Output Low Level	V <sub>OL</sub>	V <sub>ICM</sub> = -200mV I <sub>OUT</sub> = +3.0mA				10%			10%	V <sub>DD</sub>
RO Output Hi-Z Leakage Current	I <sub>OZH</sub>	0V ≤ V <sub>RO</sub> ≤ V <sub>DD</sub>		-1		1	-1		1	μA

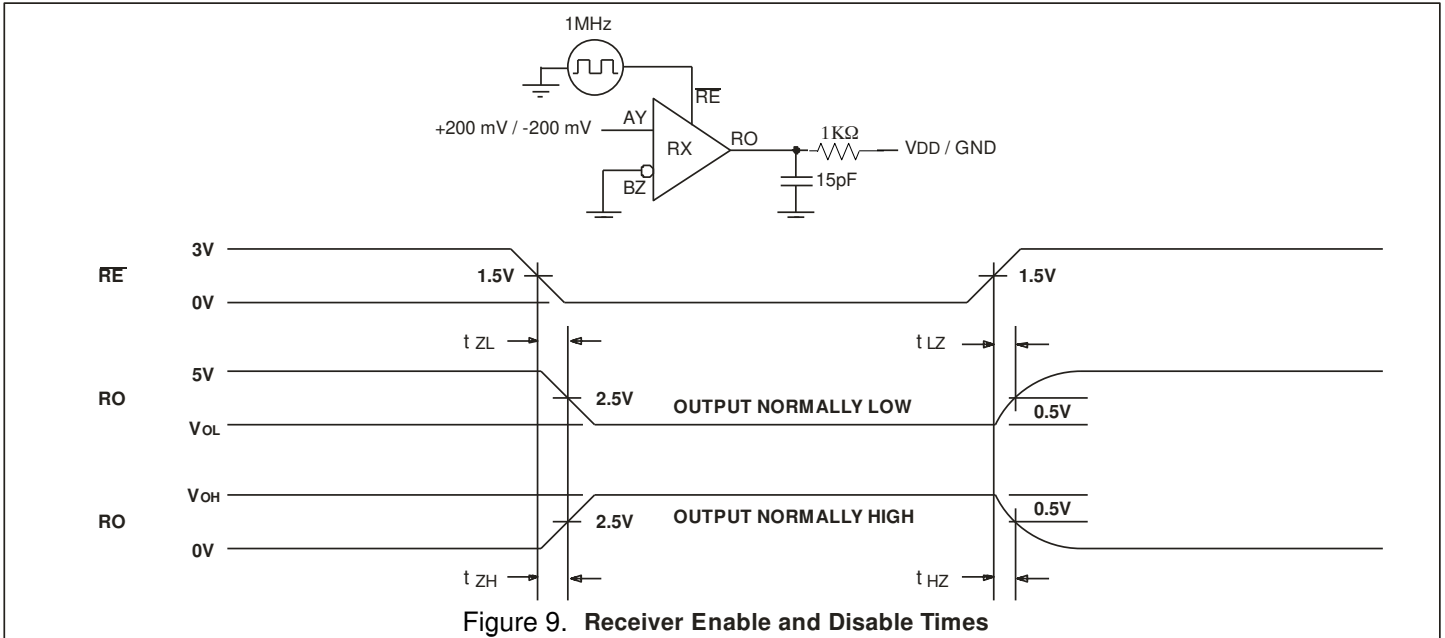
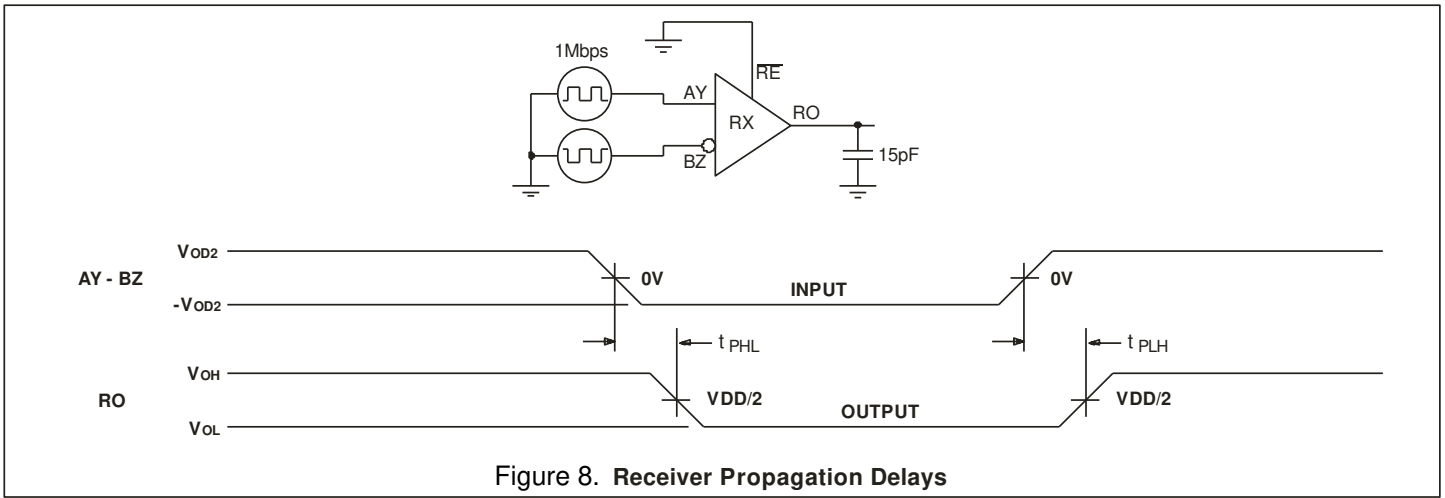
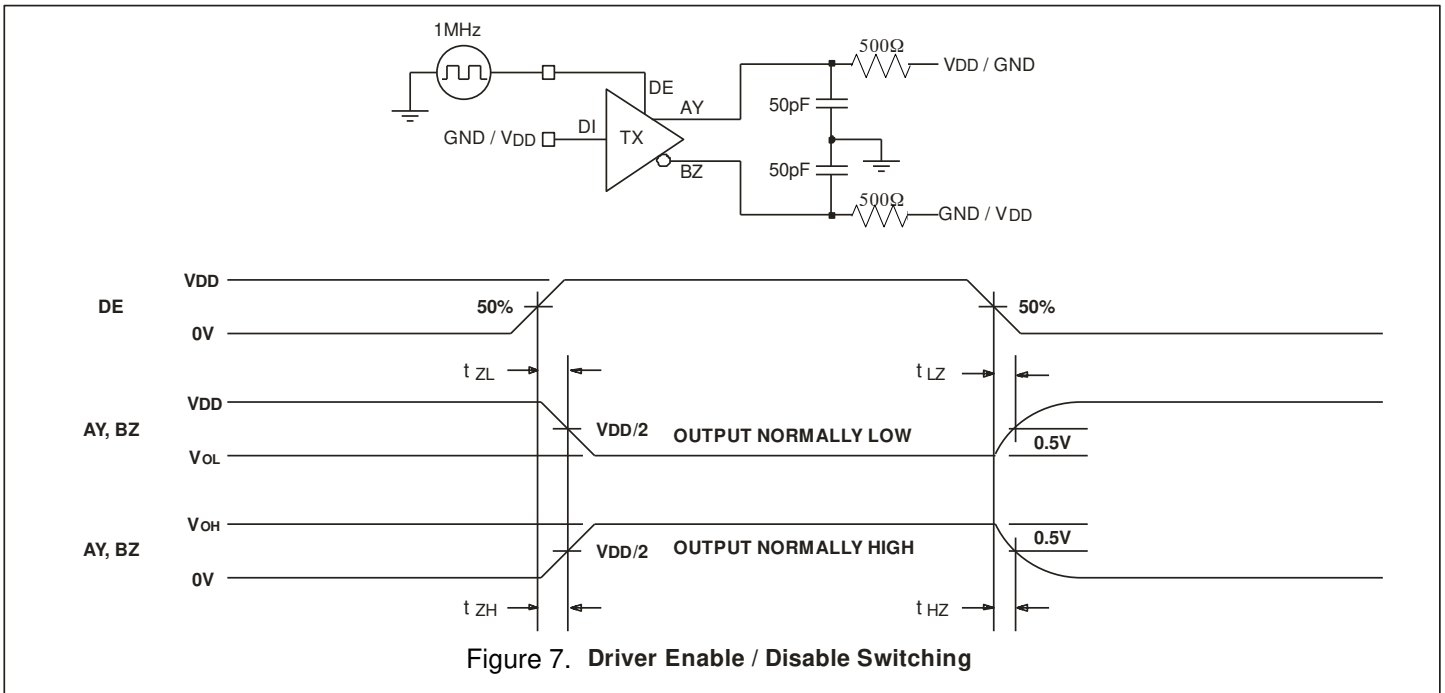
## RECEIVER SWITCHING CHARACTERISTICS

VDD = 3.0V - 3.6V or 4.5V - 5.5V as noted , Operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	FIGURE	VDD = 3.3V ± 10%			VDD = 5.0V ± 10%			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Low - to - High	t <sub>RPDR</sub>	V <sub>ID</sub> = +1.5V, C <sub>L</sub> =15pF	8	20	26	32	20	26	32	ns
Propagation Delay High - to - Low	t <sub>RPDF</sub>	V <sub>ID</sub> = -1.5V, C <sub>L</sub> =15pF	8	20	26	32	20	26	32	ns
RO Output Rise Time	t <sub>Rr</sub>	V <sub>ID</sub> = +1.5V, C <sub>L</sub> =15pF	8	1.1	1.9	3.3	1.1	1.9	3.3	ns
RO Output Fall Time	t <sub>Rf</sub>	V <sub>ID</sub> = -1.5V, C <sub>L</sub> =15pF	8	1.1	1.9	3.3	1.1	1.9	3.3	ns
Output Pulse Skew	t <sub>RMSK</sub>	V <sub>ID</sub> = +1.5V, C <sub>L</sub> =15pF	8		0.8	1.6		0.8	1.6	ns
Receiver Enable to RO Output High	t <sub>RZH</sub>	R <sub>L</sub> = 1KΩ, C <sub>L</sub> =15pF	9		12	16		12	16	ns
Receiver Enable to output Low	t <sub>RZL</sub>	R <sub>L</sub> = 1KΩ, C <sub>L</sub> =15pF	9		12	16		12	16	ns
Receiver Disable from Output High	t <sub>RHZ</sub>	R <sub>L</sub> = 1KΩ, C <sub>L</sub> =15pF	9		6	10		6	10	ns
Receiver Disable from Output Low	t <sub>RLZ</sub>	R <sub>L</sub> = 1KΩ, C <sub>L</sub> =15pF	9		6	10		6	10	ns
Shutdown to RO Active Output Delay	t <sub>RON</sub>	R <sub>L</sub> = 1KΩ, C <sub>L</sub> =15pF	9			5			5	μs
Shutdown Delay to RO HiZ	t <sub>ROFF</sub>	R <sub>L</sub> = 1KΩ, C <sub>L</sub> =15pF	9		60	100		60	100	ns

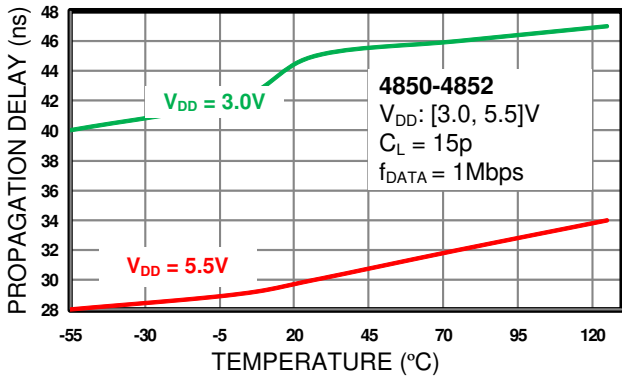
TEST CIRCUITS



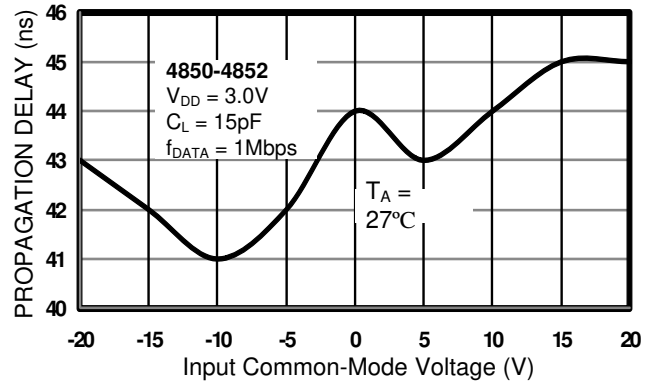


**PERFORMANCE CHARACTERISTICS OVER SUPPLY AND TEMPERATURE  
HI-4850/52**

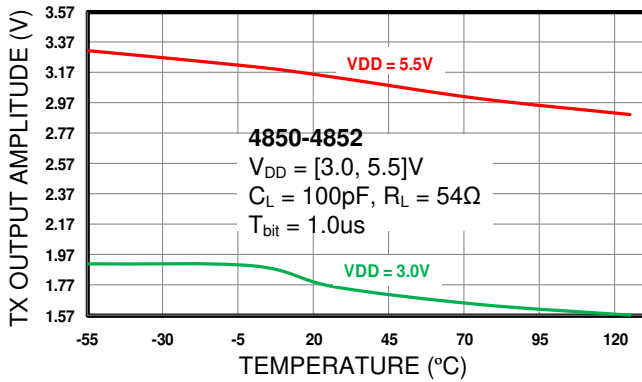
**RX PROPAGATION DELAY vs. TEMPERATURE**



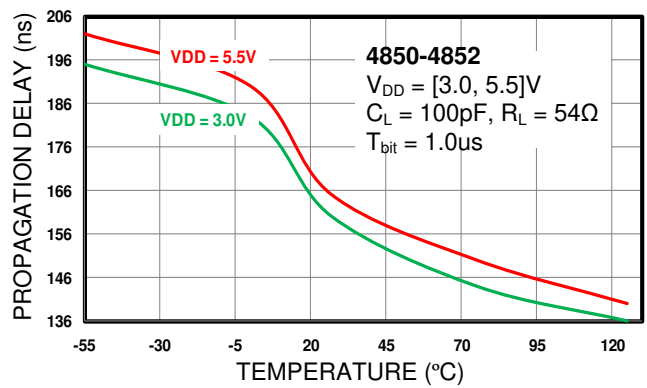
**RX PROP DELAY vs. INPUT COMMON-MODE**



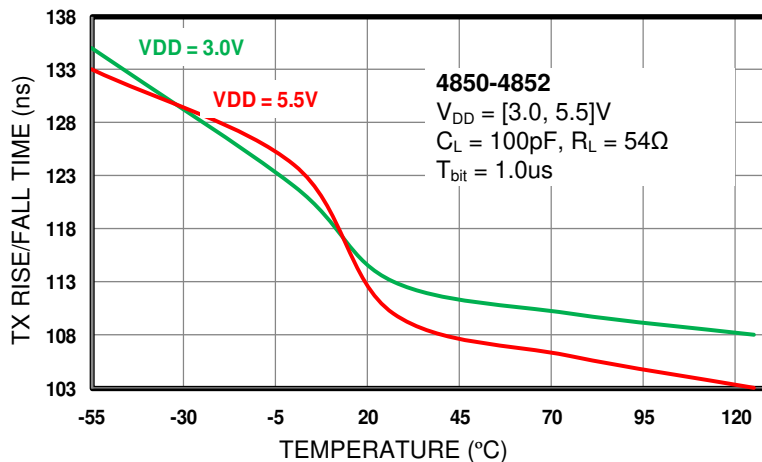
**TX DIFFERENTIAL ZERO TO PEAK AMPLITUDE vs. TEMPERATURE**



**TX PROPAGATION DELAY vs. TEMPERATURE**



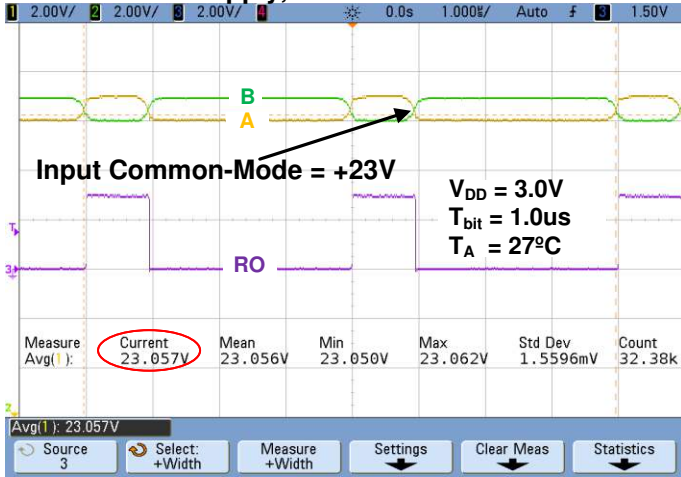
**TX Rise/Fall Time vs. TEMPERATURE**



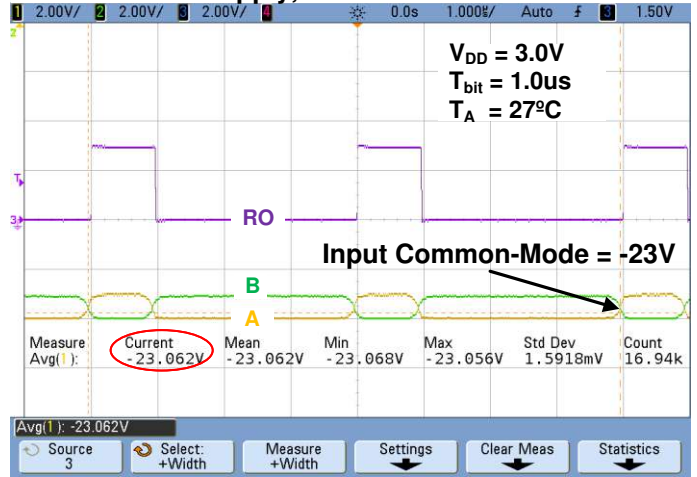


# Full Duplex Receiver Typical Performance Characteristics HI-4851/52

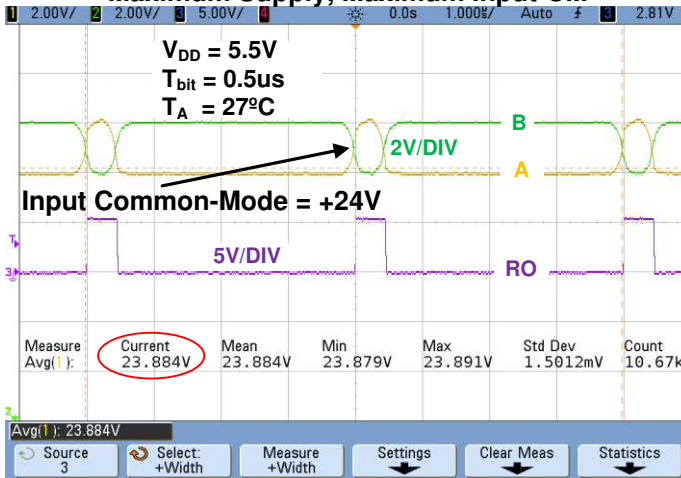
**RX Extended Common-Mode Range:  
Minimum Supply, Maximum Common-Mode**



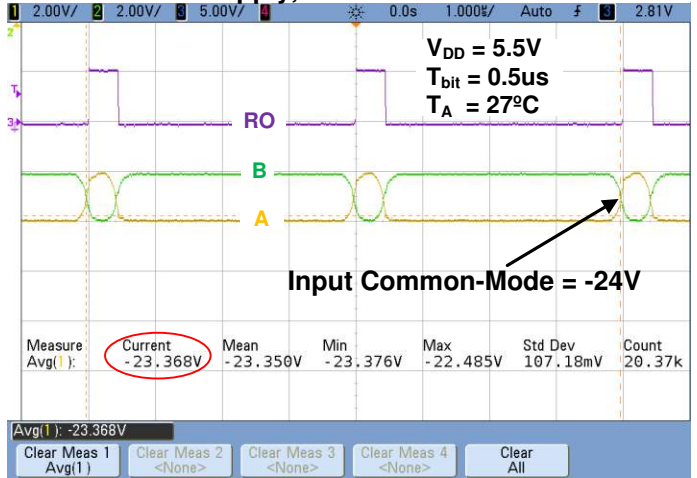
**RX Extended Common-Mode Range:  
Minimum Supply, Minimum Common-Mode**



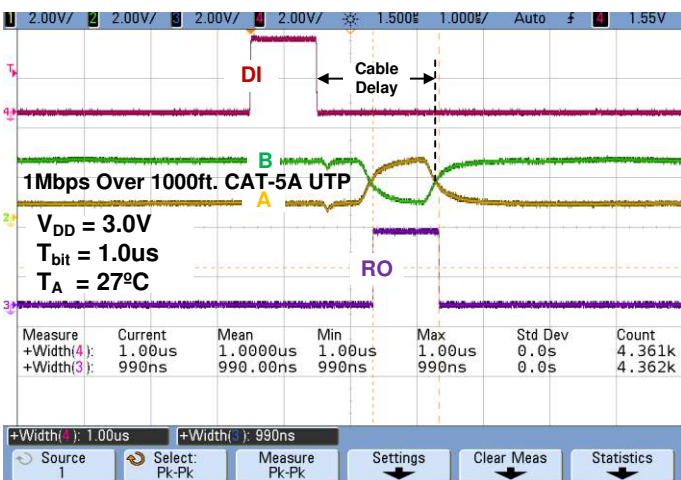
**RX Extended Common-Mode Range:  
Maximum Supply, Maximum Input-CM**



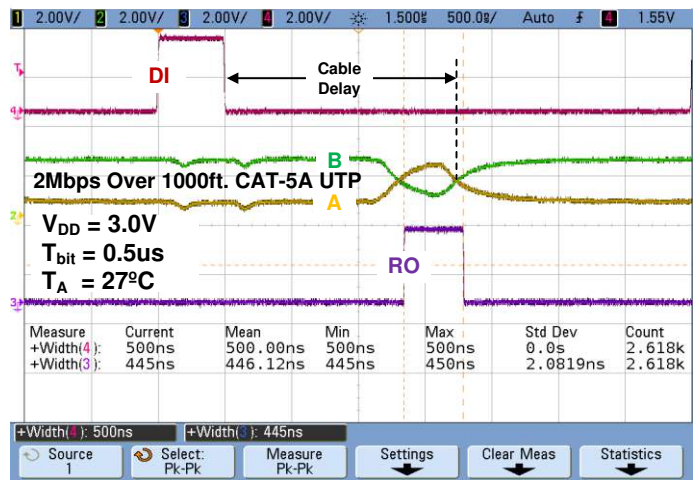
**RX Extended Common-Mode Range:  
Maximum Supply, Minimum Common-Mode**



**1Mbps Data Pulse Over 1000ft CAT-5 UTP**

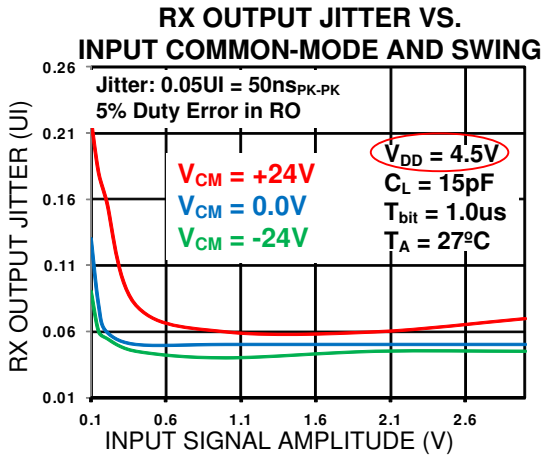


**2Mbps Data Pulse Over 1000ft CAT-5 UTP**

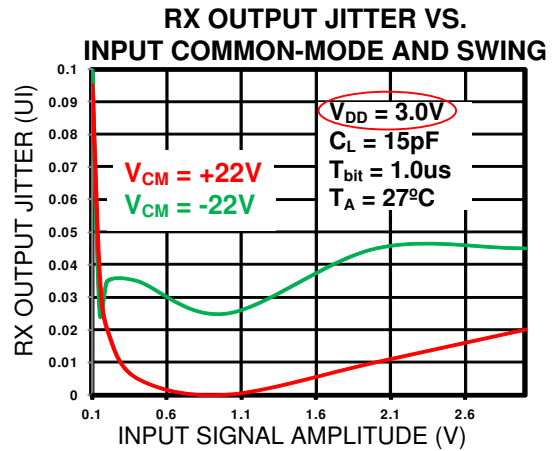




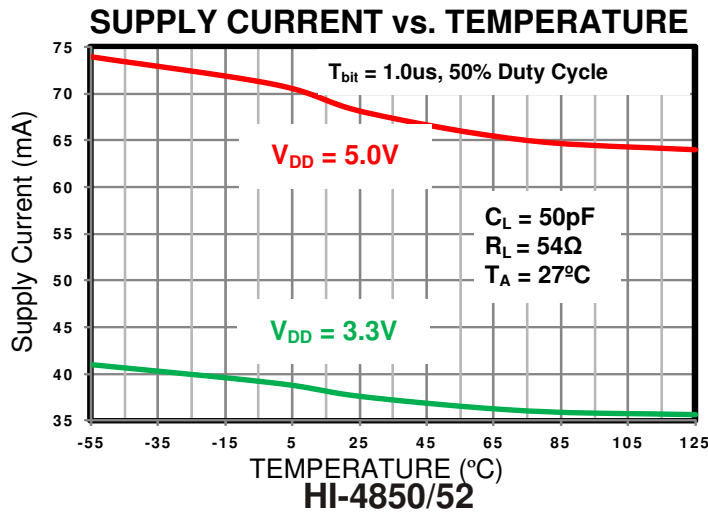
TYPICAL TRANCEIVER PERFORMANCE CHARACTERISTICS



HI-4851/52

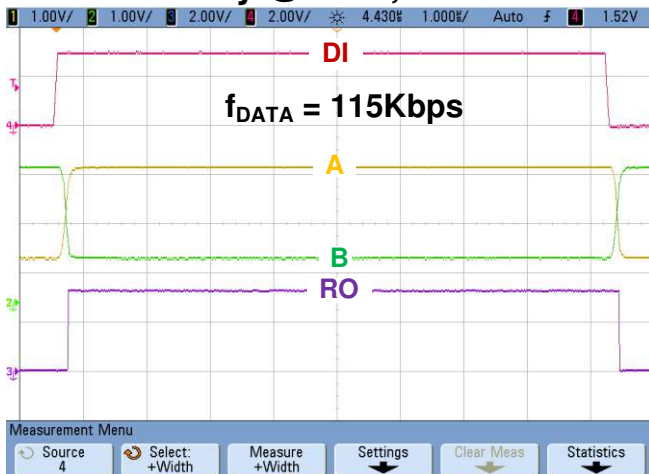


HI-4851/52



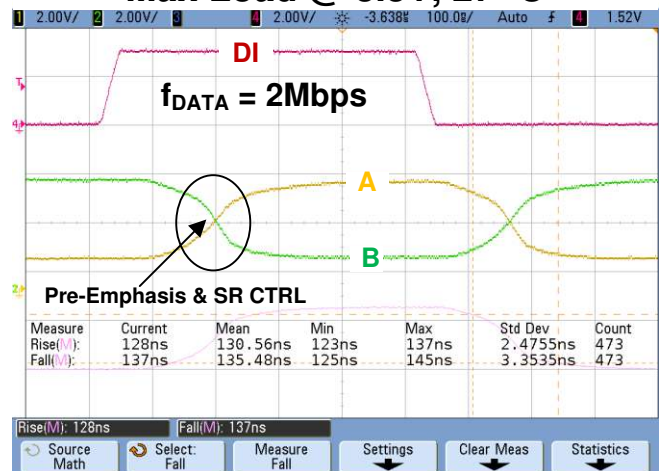
HI-4850/52

Typical TX/RX Propagation Delay @ 3.3V, 27 °C



HI-4850/52

Typical TX Rise/Fall Time Max Load @ 3.3V, 27 °C



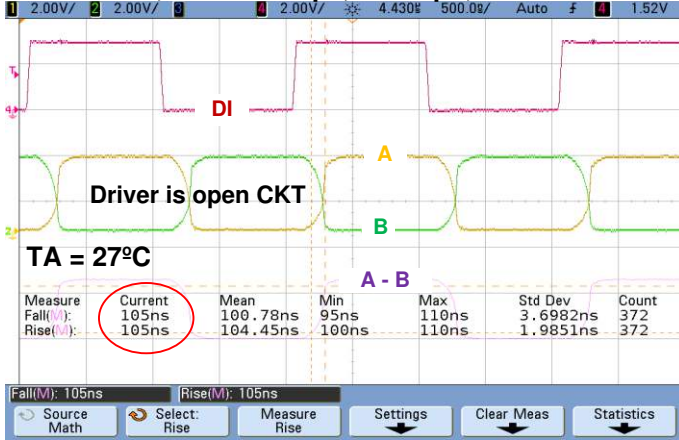
HI-4850/52

# TYPICAL PERFORMANCE CHARACTERISTICS

## HI-4850/52

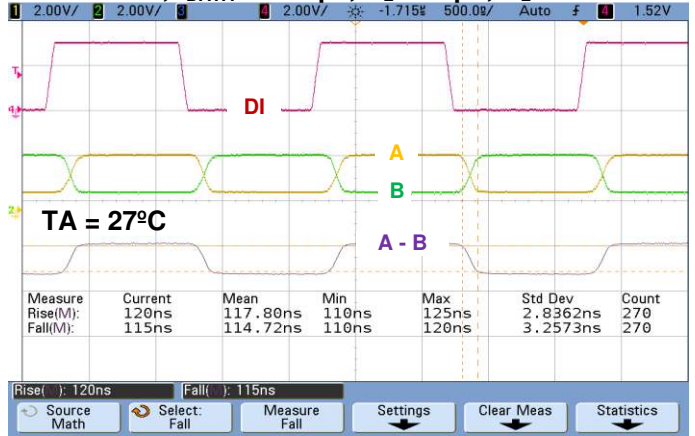
### TX Slew-Rate Controlled Output Characteristics:

VDD = 3.3V, f<sub>DATA</sub> = 1Mbps, C<sub>L</sub> < 1pF, R<sub>L</sub> = ∞



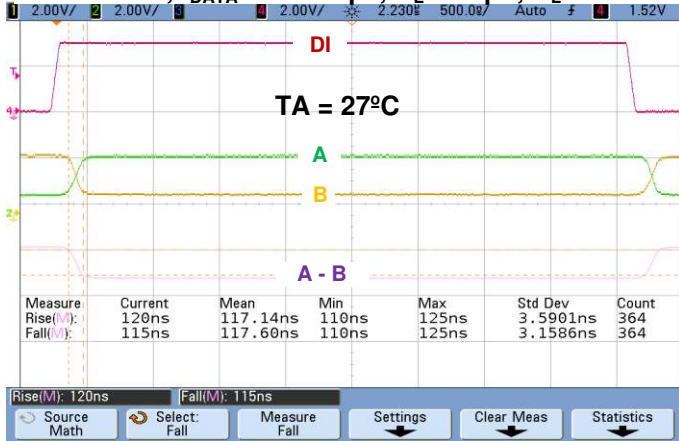
### TX Slew-Rate Controlled Output Characteristics:

VDD = 3.3V, f<sub>DATA</sub> = 1Mbps, C<sub>L</sub> = 50pF, R<sub>L</sub> = 54Ω



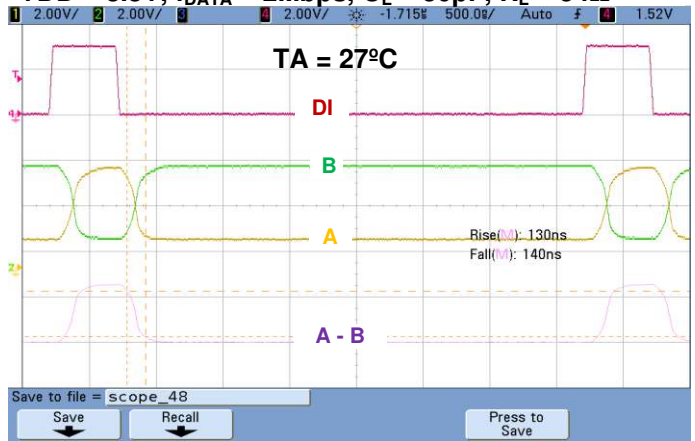
### TX Low Speed Output Characteristics:

VDD = 3.3V, f<sub>DATA</sub> = 115Kbps, C<sub>L</sub> = 50pF, R<sub>L</sub> = 54Ω



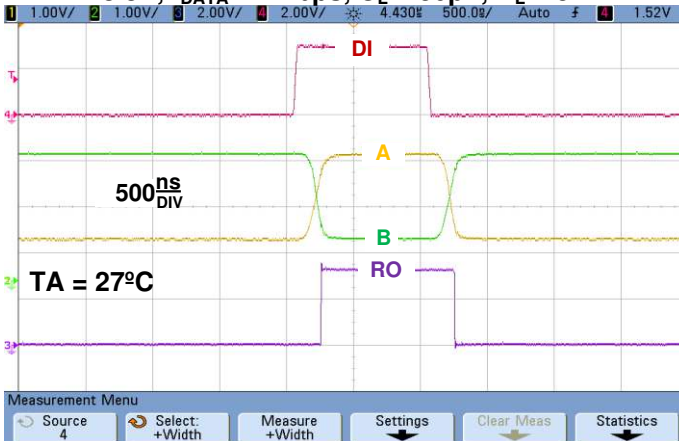
### TX High Speed Output Characteristics:

VDD = 3.3V, f<sub>DATA</sub> = 2Mbps, C<sub>L</sub> = 50pF, R<sub>L</sub> = 54Ω



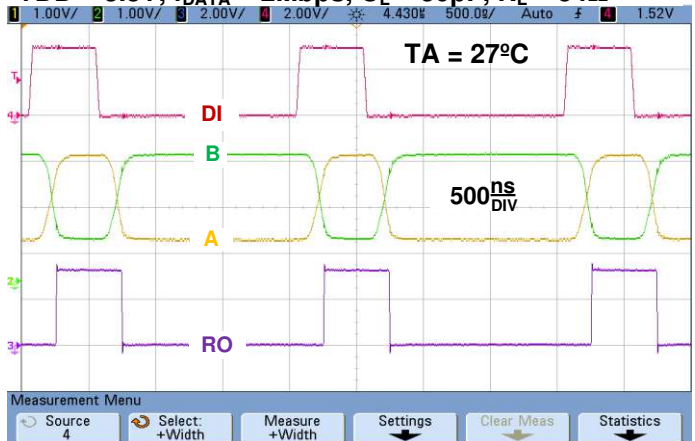
### TX / RX Propagation Delay:

VDD = 3.3V, f<sub>DATA</sub> = 1Mbps, C<sub>L</sub> = 50pF, R<sub>L</sub> = 54Ω



### TX / RX Propagation Delay:

VDD = 3.3V, f<sub>DATA</sub> = 2Mbps, C<sub>L</sub> = 50pF, R<sub>L</sub> = 54Ω



## ORDERING INFORMATION

HI-485x xx x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO
M	-55°C TO +125°C	M	YES

PART NUMBER	PACKAGE DESCRIPTION
PS	8 PIN PLASTIC NARROW BODY SOIC (8HN) (HI-4850, HI-4851)
PS	14 PIN PLASTIC NARROW BODY SOIC (14HN) (HI-4852 only)
CR	8 PIN CERDIP (8D) not available Pb-free (HI-4850, HI-4851)

PART NUMBER	FUNCTION
4850	HALF DUPLEX TRANSCEIVER
4851	FULL DUPLEX TRANSCEIVER ALWAYS ENABLED
4852	FULL DUPLEX TRANSCEIVER WITH ENABLE PINS

# ORDERING INFORMATION

HI-4852 xx x x

PART NUMBER	LEAD FINISH
Blank	NiPdAu
F	NiPdAu (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO

PART NUMBER	PACKAGE DESCRIPTION
PC	16 PIN PLASTIC 4 x 4 mm QFN (16PCS)

PART NUMBER	FUNCTION
4852	FULL DUPLEX TRANSCEIVER WITH ENABLE PINS

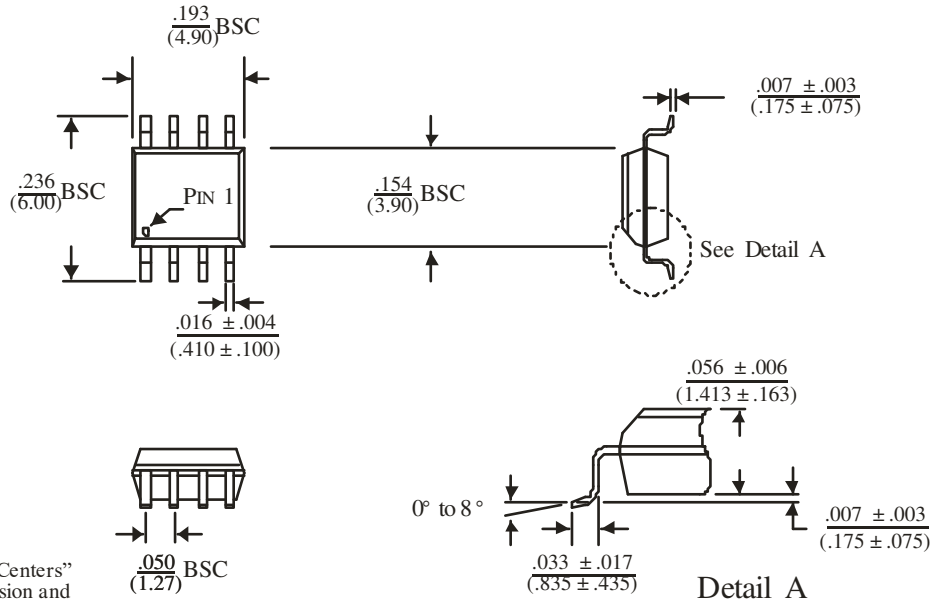
## REVISION HISTORY

Revision	Date	Description of Change
DS4850, Rev New	10/12/2011	Initial Release
Rev. A	3/15/2012	Added characterization data. Fixed errors in $V_{IL}$ and $V_{IH}$ values.
Rev. B	8/2/2012	Updated Rx Function Table rows 2 and 3 on p. 2 for DE = X. Updated package drawings for SOIC-8 (8HN), QFN-16 (16PCS) and SOIC-14 (14HN) packages.
Rev. C	03/13/2013	Correct typo on nRE pull-up resistor (should be pull-down). Update Digital Input pull-up/pull-down current. Update typo in Figure 4 resistors. Update solder temperature (reflow) in Max. Ratings
Rev. D	04/18/2017	Remove redundant Control Input Voltages from Absolute Maximum Ratings (same parameter as Digital Input Voltages).
Rev. E	04/24/2019	Correct typo in QFN package drawing. Update QFN Lead Finish to NiPdAu.
Rev. F	11/05/2021	Update minimum Differential Load Resistance from 54 Ohm to 45 Ohm in Specified Operating Conditions table.

**8-PIN PLASTIC SMALL OUTLINE (SOIC) - NB**  
(Narrow Body)

*inches (millimeters)*

Package Type: 8HN

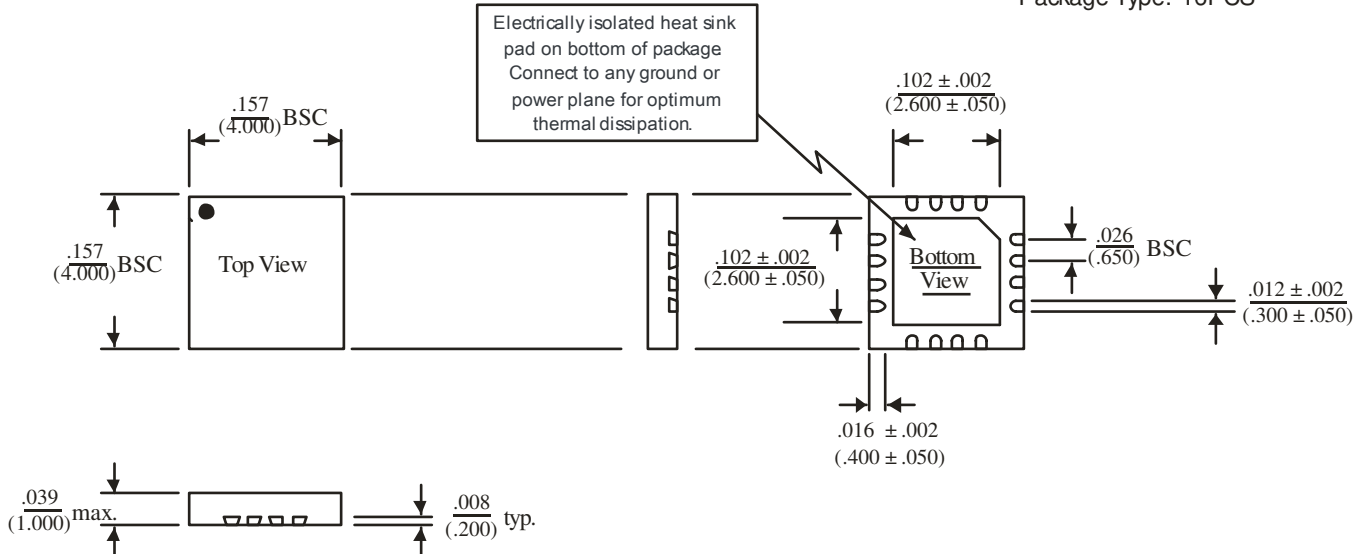


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (EDEC Standard 95)

**16-PIN PLASTIC CHIP-SCALE PACKAGE**

*inches (millimeters)*

Package Type: 16PCS



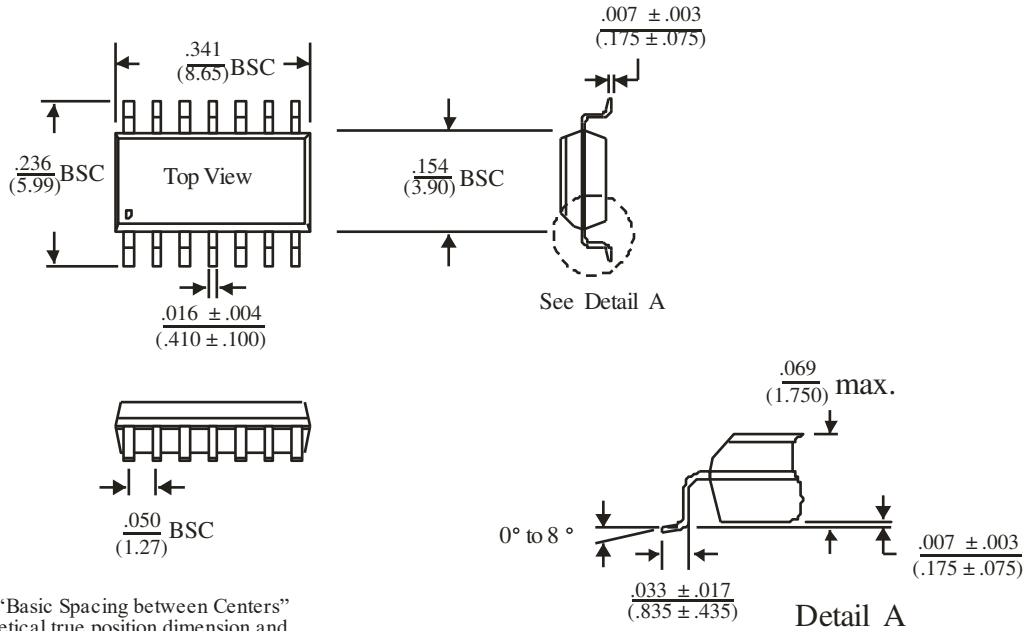
BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (EDEC Standard 95)



**14-PIN PLASTIC SMALL OUTLINE (SOIC) - NB**  
(Narrow Body)

*inches (millimeters)*

Package Type: 14HN

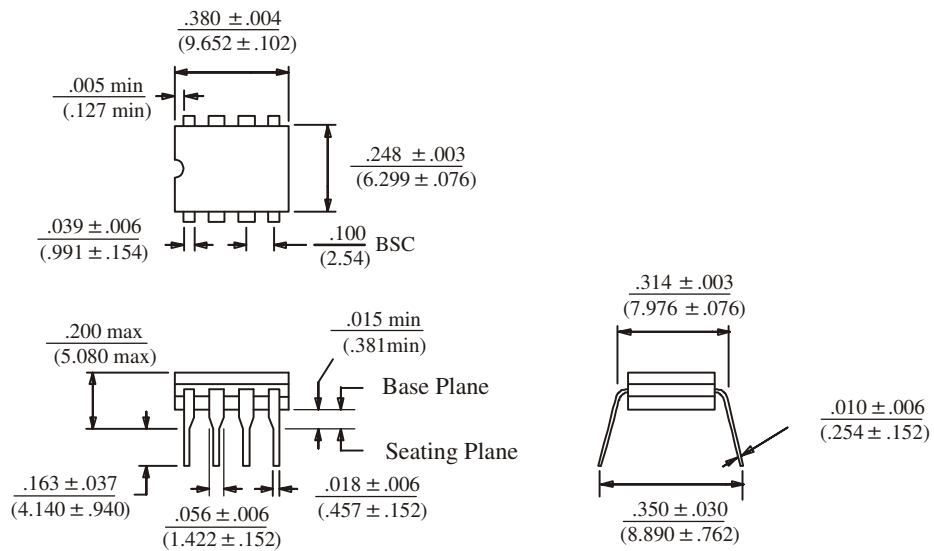


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

**8-PIN CERDIP**

*inches (millimeters)*

Package Type: 8D



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)