

UCC53x0xD Evaluation Module

The manual describes the UCC53x0xD evaluation module (EVM). The UCC53x0x EVM allows designers to evaluate device AC and DC performance of the complete UCC53x0 family of devices (split output, Miller clamp, UVLO) with a prepopulated capacitive load or user-installed IGBT in the standard TO-247 package.

WARNING

Although these devices provide galvanic isolation of up to 3000 V, the EVM cannot be used for isolation voltage testing. Voltage exceeding the EVM ratings ($V_{CC1} > 15\text{ V}$, $V_{CC2} - V_{EE2} > 33\text{ V}$, or IGBT collector-emitter voltage $V_{CE} > 50\text{ V}$) can damage the EVM resulting in personal injury.

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Trademarks

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1 Overview

The UCC53x0x family of devices is a 3-kV_{RMS} basic isolated, IGBT and MOSFET gate driver with split outputs (UCC53x0S), Miller clamp (UCC53x0M), and UVLO (UCC53x0E) features. These gate drivers are capable of sourcing and sinking 0.5 A to 10 A of peak current, depending on the device. The input side operates from a single 3-V to 15-V supply. The output side allows for a supply range from a minimum of 15 V to a maximum of 33 V. Two complementary CMOS inputs control the output state of the gate driver. The short propagation time ensures accurate control of the output stage.

When the IGBT is turned off during normal operation with bipolar output supply, the output is hard clamped to $V_{\text{EE}2}$ in a UVLO (UCC53x0E) device. The UCC53x0M devices, with a unipolar output supply, have an active Miller clamp, allowing Miller current to sink across a low-impedance path which prevents the IGBT from being dynamically turned on during high-voltage transient conditions. The UCC53x0S device, which has a split output, provides better control over the rise and fall time of the driver output.

2 Pin Configuration of the UCC53x0 Isolated IGBT Gate Drivers

Figure 1 shows the UCC53x0 pin configurations in an 8-pin SOIC (D) package.

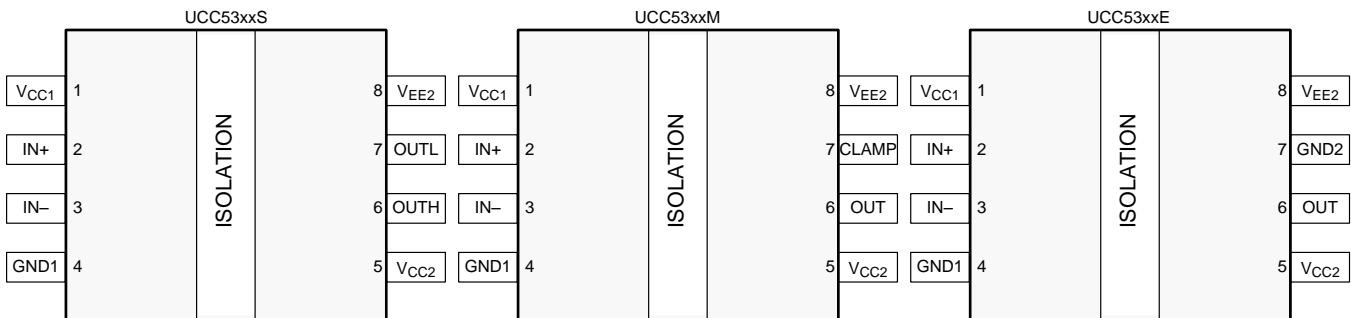


Figure 1. UCC53x0x Pin Configurations

3 EVM Setup and Precautions

3.1 Before You Begin

The following warnings and cautions are noted for the safety of anyone using or working close to the UCC53x0 EVM. Observe all safety precautions.

**Warning**

Warning Hot surface. Contact may cause burns. Do not touch.

**Danger High Voltage**

The UCC53x0 EVM does not have an isolation boundary. If you apply high voltage to this board, all terminals should be considered high voltage. Electric shock is possible when connecting the board to live wire. The board should be handled with care by a professional. For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

CAUTION

Do not leave EVM powered while unattended.

The IGBT device can be populated on board only for low current functionality testing. The IGBT device requiring heat sink (high load current) must be externally connected and is not recommended to be populated on EVM.

3.2 Power Supply Connections

Figure 2 shows the UCC53x0 EVM power supply schematic.

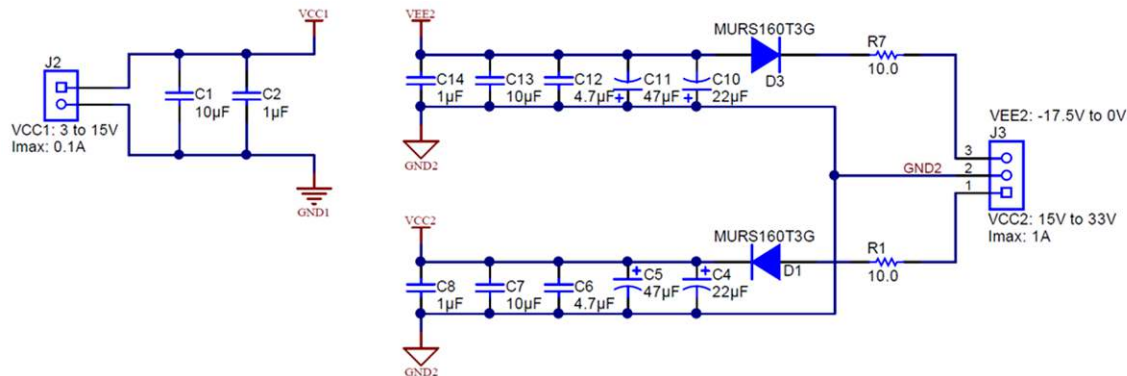


Figure 2. UCC53x0 EVM Power Supply Schematic

The input side of the UCC53x0x EVM (V_{CC1}) operates from a single 3-V to 15-V power supply and connected by J2. A test point (TP1) is available for monitoring the input power supply.

The UCC53x0 EVM provides connections for evaluating the output side (V_{CC2} , V_{EE2}) with either a bipolar or unipolar power supply, from a minimum 15 V to maximum 33 V. V_{CC2} and V_{EE2} can be supplied at J3. The D1 and D3 diodes and R1 and R7 resistors are provided for supply reverse polarity protection and to limit the supply current.

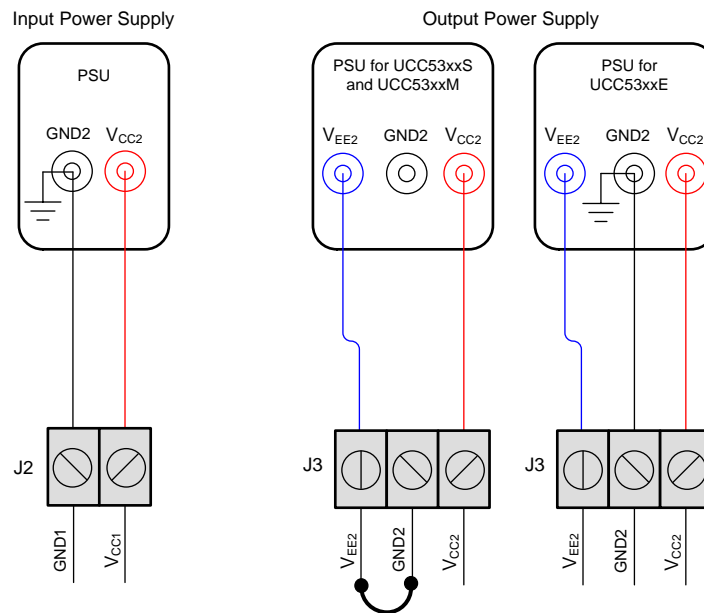


Figure 3. Input Power Supply (J2) and Output Power Supply (J3)

3.3 Signal Connections

The UCC53x0 EVM is a universal EVM designed to support the complete UCC53x0 family of devices. The same EVM can be used for a split output, Miller clamp, and UVLO device by configuring it according to Figure 4.

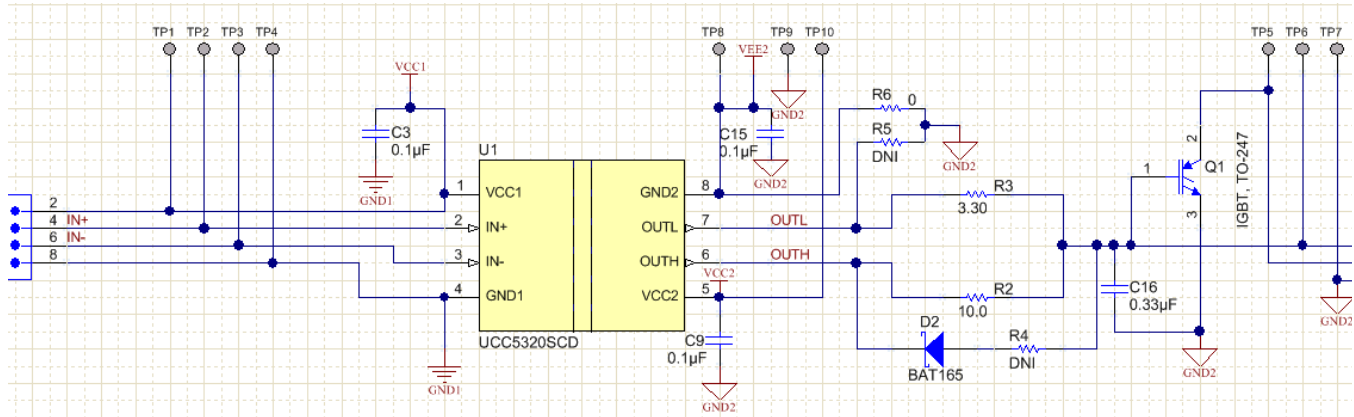


Figure 4. UCC53x0S EVM Signal Path Schematic

Table 1 lists the UCC53x0 configurations.

Table 1. UCC53x0 Configurations

UCC53x0 Configurations	Pin 7	R3	R4	R5	R6
UCC53x0Sx: Split	OUTL	3.3 Ω	DNI	DNI	0 Ω
UCC53x0Mx: Miller	CLAMP	0 Ω	10 Ω	DNI	0 Ω
UCC53x0Ex: UVLO-GND2	GND2	DNI	10 Ω	0 Ω	DNI

3.3.1 I/O Connections

Figure 4 shows the signal path schematic of the EVM. The J1 jumper allows for stimulus or monitoring of the device I/O pins IN+ and IN-. The test points TP2 and TP3 provide additional access to the I/O pins.

3.3.2 Output and Loading

The EVM comes populated with a 330-nF load (C16) on the output side. The user can replace the populated capacitive load with a load of choice to emulate the required system scenario. The output can be monitored directly with TP6. The gate resistors, R2 and R3, control the rise and fall times of the output (OUTH and OUTL). These resistors can be modified by the user to alter the turnon and turnoff characteristics of the output.

The EVM also allows for functional evaluation of the device with an IGBT at light loads (low current and voltage < 50 V). The IGBT device that requires a heat sink (higher load current) should be externally connected and is not recommended to be populated on the EVM. During evaluation with an IGBT load, the preinstalled capacitive load (C16) must be removed.

The EVM provides an additional connection (J4) for applying an external power supply to the IGBT collector. The EVM is not intended for high voltage testing and the voltage applied to J4 should be limited to 50-V DC.

3.3.3 EVM Configurations

3.3.3.1 Split (UCC53x0S)

The OUTL pin (pin 7) is connected to the gate by a 3.3-Ω resistor (R3) while the OUTH pin is connected to the gate using a 10-Ω resistor (R2). This configuration enables separate control over rise and fall times. The R4 and R5 resistors must be removed and the R6 resistor must be connected by a 0-Ω resistor to ensure proper connection to GND2 pin (pin 8).

3.3.3.2 Miller-Clamp (UCC53x0M)

The CLAMP pin (pin 7) is connected to the gate by a 0-Ω resistor (R3). The gate must also be connected to the OUT pin with a diode and series 10-Ω resistance (R4). The R5 resistor must be removed and the R6 resistor must be connected by a 0-Ω resistor to ensure proper connection to GND2 pin (pin 8).

3.3.3.3 UVLO-GND2 (UCC53x0E)

In this configuration, pin 7 becomes the GND2 pin, while pin 8 becomes V_{EE2} where negative voltage with respect to GND2 can be applied. The R3 and R6 resistor must both be removed and the R5 resistor must be connected by a 0-Ω resistor to ensure proper connection to GND2 pin (pin 7). The gate must also be connected to the OUT pin with a diode and series 10-Ω resistance (R4).

4 Example Measurements

Figure 5 shows measurements performed under the default EVM configuration (with R3 = 3.3 Ω, R6 = 0 Ω, and R4 and R5 not populated). For these measurements, V_{IN-} is connected to GND1.

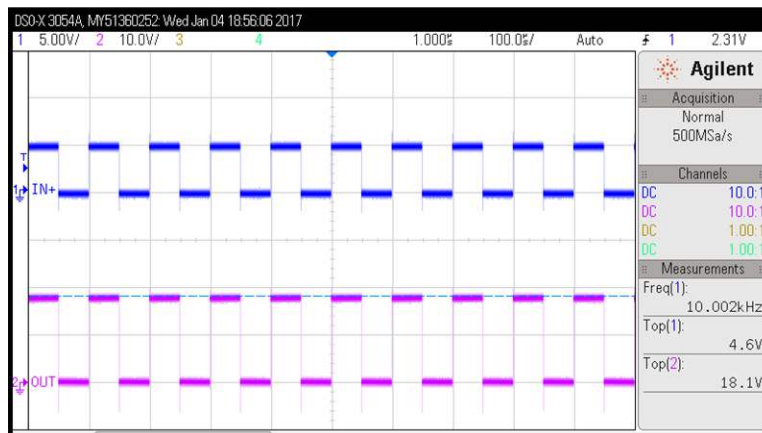


Figure 5. UCC53x0S Device Input and Output

Figure 6 shows the input and output of the UCC53x0M device for a 10-kHz input signal with R3 = 0 Ω, R4 = 10 Ω, R6 = 0, and R5 not populated.

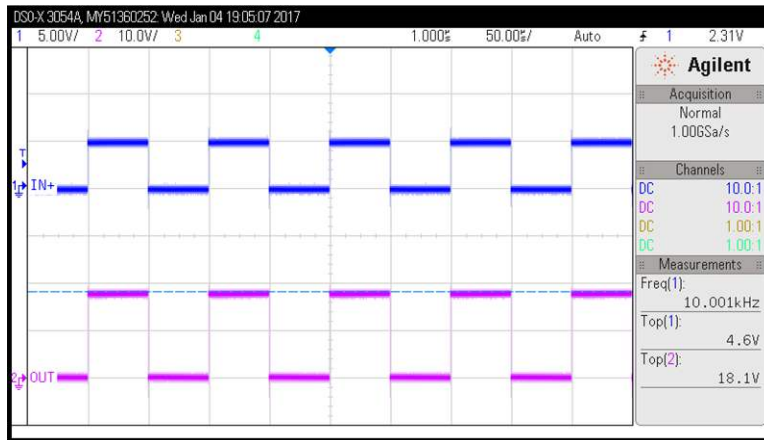


Figure 6. UCC53x0M Device Input and Output

Figure 7 shows output of the UCC53x0E EVM for a 10-kHz input signal with $R4 = 10 \Omega$, $R5 = 0 \Omega$, $R3$ and $R6$ not populated, with a unipolar output supply ($V_{CC2} = 18 \text{ V}$, $V_{EE2} = \text{GND2}$).

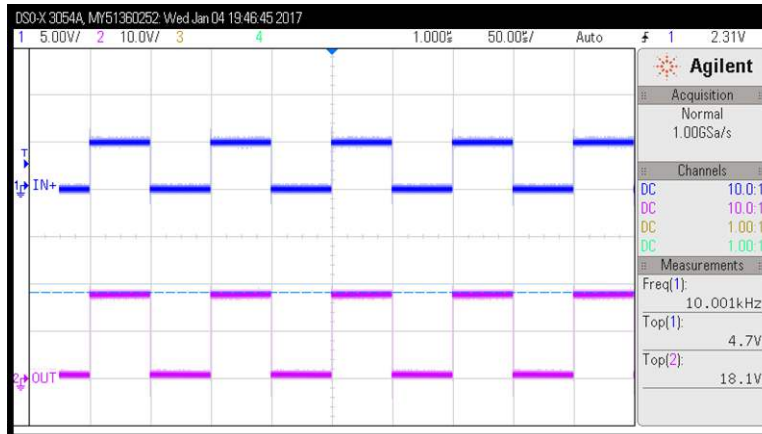


Figure 7. UCC53x0E Device Input and Output With Unipolar Output Supply

Figure 8 shows output of the UCC53x0E EVM for a 10-kHz input signal with $R4 = 10 \Omega$, $R5 = 0 \Omega$, $R3$ and $R6$ not populated, and a bipolar output supply ($V_{CC2} = 15 \text{ V}$, $V_{EE2} = -15 \text{ V}$).

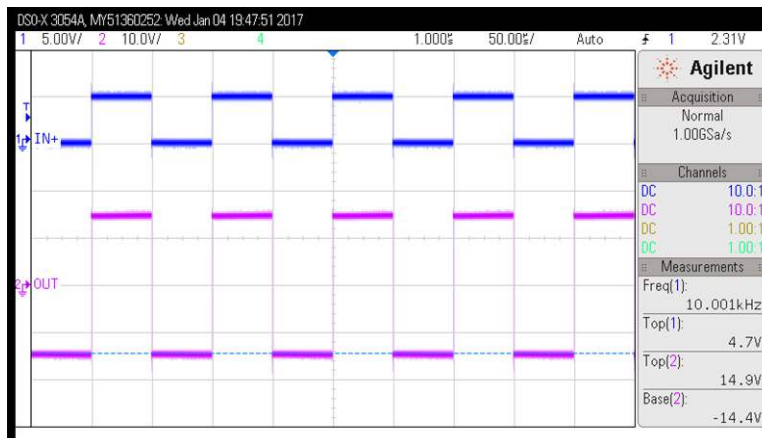


Figure 8. UCC53x0E Device Input and Output With Bipolar Output Supply

5 Printed-Circuit Board and Layout

The UCC53x0 device is an isolated gate driver with several important features. The printed-circuit board (PCB) and EVM, as shown in Figure 9, have been designed to support the UCC53x0S, UCC53x0M, UCC53x0E family of devices and to allow the user to evaluate basic operation and features. The left side of the PCB contains the interface to the input and control functions of the integrated circuit (IC). The right side of the PCB has been designed to interface to an IGBT. No electrical connections exist between the right and left sides of the PCB.

Figure 10 and Figure 11 show the PCB layout for UCC53x0D EVM.

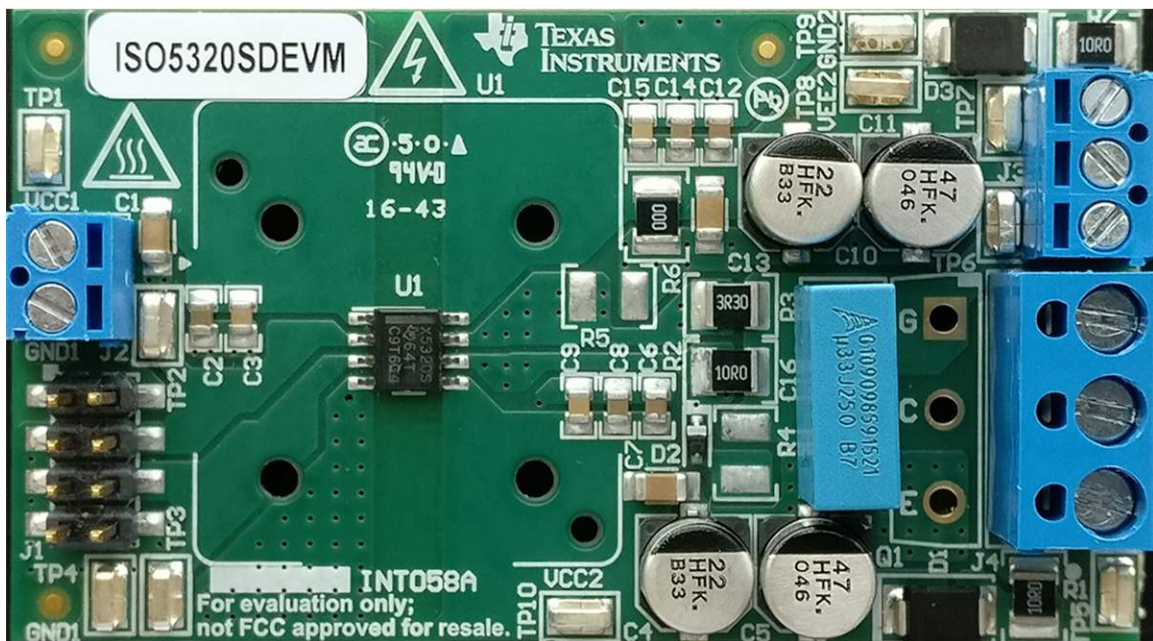


Figure 9. UCC5320SD EVM

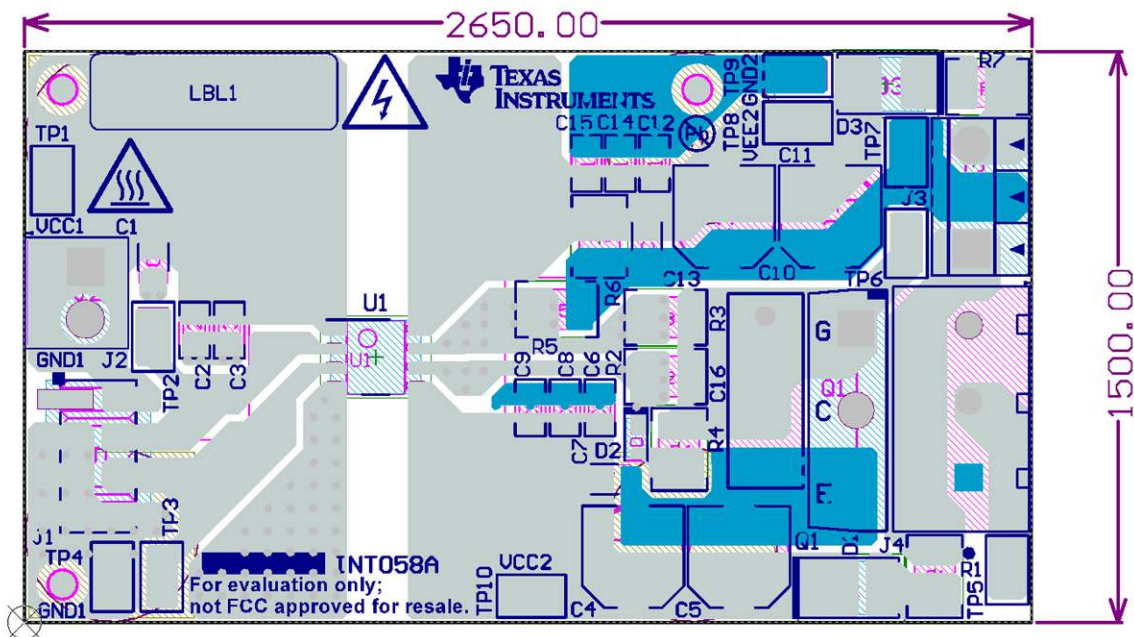


Figure 10. UCC53x0D EVM Top Layer

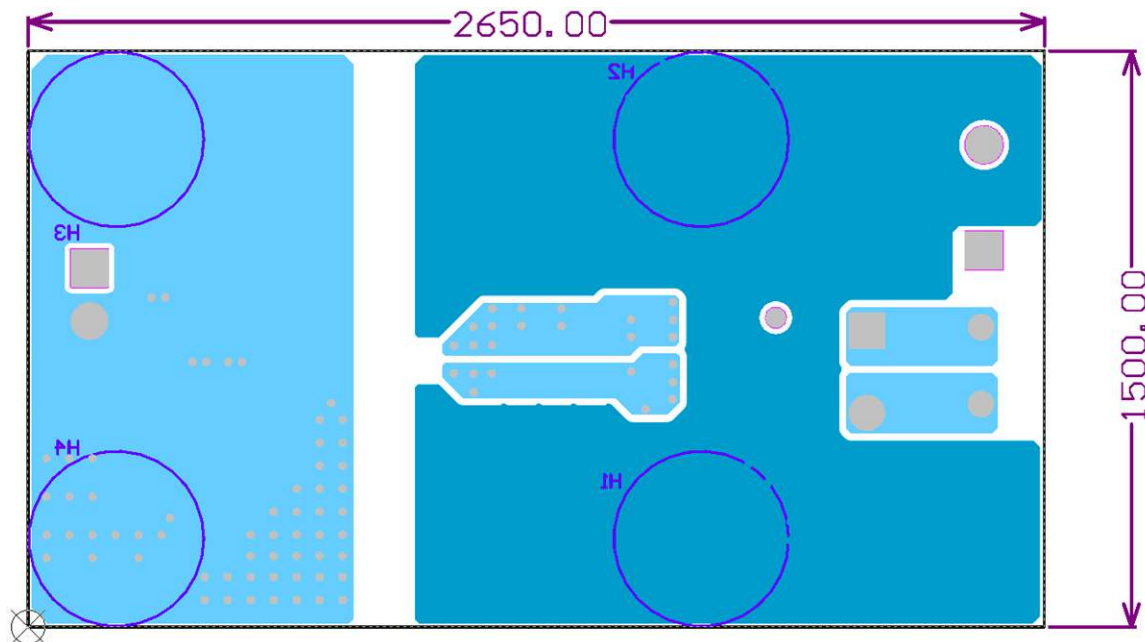


Figure 11. UCC53x0D EVM Bottom Layer

5.1 UCC53x0 Operation

5.1.1 Input-Side Operation: DC Power and Control

5.1.1.1 DC Input Power

The left side of the UCC53x0 (and therefore the PCB) can be operated using either a 3-V ($\pm 10\%$) to 15-V ($\pm 10\%$) DC power supply. The user can choose to operate the UCC53x0 EVM by battery. The DC power supply must be connected to the J2 terminal.

5.1.1.2 Control

The interface to the device is via the J1 header. It contains the IN+ and IN- inputs. The J1 header allows easy connections to test equipment using standard clip leads. The IN+ and IN- control signals have test points for additional connections. These are test points TP2 and TP3.

5.1.2 Output-Side Operation

5.1.2.1 DC Output Power

Power is provided to V_{CC2} on the right side of the device at J3 terminal as shown in [Figure 3](#). The DC supply must be able to provide a bias voltage over the range of 15 V DC to 33 V DC. The user can choose to operate the UCC53x0 EVM by battery. If a negative gate drive is required, a DC supply (or battery) must be connected across V_{EE2} (-17.5 V to 0 V) at the J3 terminal as shown in [Figure 3](#). The voltage across V_{CC2} and V_{EE2} must not exceed 33 V for operation.

5.1.2.2 Load

As shipped, the UCC53x0 EVM does not have an IGBT installed. The user can populate IGBT for low current functionality testing at the pads provided. The IGBT device that requires a heat sink (higher load current) should be externally connected and is not recommended to be populated on the EVM. Most IGBTs are available in the standard TO-247 package.

5.1.3 Test Points

Test points have been provided for ready access to signal monitoring and are listed in [Table 2](#).

Table 2. Test Points

Test point	Type	Function
TP1	Supply	V _{CC1} (side1)
TP2	Input	IN+ (side1)
TP3	Input	IN- (side1)
TP4	Ground	GND1(Side1)
TP5	Input	Collector voltage (side2)
TP6	Output	Gate voltage (side2)
TP7	Input	Emitter voltage (side2)
TP8	GND and Negative supply voltage	UCC53x0E: V _{EE2} (side2)
		UCC53x0S: GND2 (side2)
		UCC53x0M: GND2 (side2)
TP9	GND	GND2 (side2)
TP10	Supply	V _{CC2} (side 2)

5.2 UCC53x0D EVM Bill of Materials

Table 3 lists the UCC53x0D EVM bill of materials.

Table 3. Bill of Materials

Quantity	Designator	Value	Description	Manufacturer	Part Number
1	J1		Header, 100mil, 4x2, Gold, SMT	Molex	0015910080
1	C16	0.33 μ F	CAP, Film, 0.33 μ F, 250 V, \pm 5%, AEC-Q200 Grade 1, TH	TDK	B32521C3334J189
1	D2	40V	Diode, Schottky, 40 V, 0.75 A, AEC-Q101, SOD-323	Infineon Technologies	BAT165E6327HTSA1
3	C3, C9, C15	0.1 μ F	CAP, CERM, 0.1 μ F, 50 V, \pm 10%, X7R, 0805	Kemet	C0805C104K5RACTU
3	C2, C8, C14	1 μ F	CAP, CERM, 1 μ F, 50 V, \pm 10%, X7R, 0805	Kemet	C0805C105K5RACTU
2	C6, C12	4.7 μ F	CAP, CERM, 4.7 μ F, 50 V, \pm 10%, X5R, 0805	TDK	C2012X5R1H475K125AB
3	C1, C7, C13	10 μ F	CAP, CERM, 10 μ F, 50 V, \pm 10%, X5R, 1206_190	Samsung Electro-Mechanics	CL31A106KBHNNNE
1	R3	DNI (UCC53x0E)			
		0 Ω (UCC53x0M)	RES, 0, 1%, 0.75 W, AEC-Q200 Grade 0, 1210	Vishay-Dale	CRCW12100000Z0EAHP
		3.3 Ω (UCC53x0S)	RES, 3.30, 1%, 0.75 W, AEC-Q200 Grade 0, 1210	Vishay-Dale	CRCW12103R30FKEAHP
3	R1, R2, R7	10 Ω	RES, 10.0, 1%, 0.75 W, AEC-Q200 Grade 0, 1210	Vishay-Dale	CRCW121010R0FKEAHP
1	R4	10 Ω (UCC53x0E)	RES, 10.0, 1%, 0.75 W, AEC-Q200 Grade 0, 1210	Vishay-Dale	CRCW121010R0FKEAHP
		10 Ω (UCC53x0M)	RES, 10.0, 1%, 0.75 W, AEC-Q200 Grade 0, 1210	Vishay-Dale	CRCW121010R0FKEAHP
		DNI (UCC53x0S)			
1	R5	0 Ω (UCC53x0E)	RES, 0, 1%, 0.75 W, AEC-Q200 Grade 0, 1210	Vishay-Dale	CRCW12100000Z0EAHP
		DNI (UCC53x0M)			
		DNI (UCC53x0S)			
1	R6	DNI (UCC53x0E)			
		0 Ω (UCC53x0M)	RES, 0, 1%, 0.75 W, AEC-Q200 Grade 0, 1210	Vishay-Dale	CRCW12100000Z0EAHP
		0 Ω (UCC53x0S)	RES, 0, 1%, 0.75 W, AEC-Q200 Grade 0, 1210	Vishay-Dale	CRCW12100000Z0EAHP
1	J2		Terminal Block, 3.5mm Pitch, 2x1, TH	On-Shore Technology	ED555/2DS
1	J3		Terminal Block, 3.5mm Pitch, 3x1, TH	On-Shore Technology	ED555/3DS
2	C4, C10	22 μ F	CAP, AL, 22 μ F, 50 V, \pm 20%, 0.88 Ω , SMD	Panasonic	EEE-FK1H220P
2	C5, C11	47 μ F	CAP, AL, 47 μ F, 50 V, \pm 20%, 0.68 Ω , SMD	Panasonic	EEE-FK1H470XP
1	U1	UCC53x0DEV M	0.5/2/4/6A/10A Isolated IGBT Gate Drivers with High CMTI, D0008B (SOIC-8)	Texas Instruments	UCC53x0SDR
			0.5/2/4/6A/10A Isolated IGBT Gate Drivers with High CMTI, D0008B (SOIC-8)	Texas Instruments	UCC53x0MDR
			0.5/2/4/6A/10A Isolated IGBT Gate Drivers with High CMTI, D0008B (SOIC-8)	Texas Instruments	UCC53x0EDR
2	D1, D3	600V	Diode, Ultrafast, 600 V, 2 A, SMB	ON Semiconductor	MURS160T3G
1	J4		Terminal Block, 3x1, 5.08 mm, TH	On-Shore Technology	OSTTA034163
4	H1, H2, H3, H4		Bumpon, Hemisphere, 0.44 x 0.20, Clear	3M	SJ-5303 (CLEAR)
10	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10		Test Point, Miniature, SMT	Keystone	5019

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1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
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 - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.
3. *Regulatory Notices:*
 - 3.1 *United States*
 - 3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.
 - 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page

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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/llds/ti_ja/general/eStore/notice_02.page
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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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