Isolated, 4 A Dual-Channel Gate Driver

Enhanced Product

ADuM3221-EP

FEATURES

- 4 A peak output current
- Precise timing characteristics
  - 60 ns maximum isolator and driver propagation delay
  - 5 ns maximum channel to channel matching
- High junction temperature operation: 125°C
- 3.3 V to 5 V input logic
- 7.6 V to 18 V output drive
- Undervoltage lockout (UVLO) at 7.0 V V_{DD2}
- Thermal shutdown protection at >150°C
- Default low output
- High frequency operation: dc to 1 MHz
- CMOS input logic levels
- High common-mode transient immunity: 25 kV/µs
- Safety and regulatory approvals
  - UL recognition
    - 2500 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A (pending)
  - VDE certificate of conformity (pending)
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 560 V peak
- Small footprint and low profile
  - Narrow-body, RoHS compliant, 8-lead SOIC
  - 4.9 mm × 6 mm × 1.55 mm

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: −55°C to +125°C
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Isolated synchronous dc-to-dc converters
- MOSFET/IGBT gate drivers

GENERAL DESCRIPTION

The ADuM3221-EP[1] is an isolated, 4 A dual-channel gate driver based on the Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic transformer technology, this isolation component provides outstanding performance characteristics superior to the alternatives, such as the combination of pulse transformers and gate drivers.

The ADuM3221-EP provides digital isolation in two independent isolation channels. It has a maximum propagation delay of 60 ns and 5 ns channel to channel matching. In comparison to gate drivers that employ high voltage level translation methodologies, the ADuM3221-EP offers the benefit of true, galvanic isolation between the input and each output, enabling voltage translation across the isolation barrier. The ADuM3221-EP allows both outputs to be on at the same time. This device offers a default output low characteristic as required for gate drive applications.

The ADuM3221-EP operates with an input supply voltage ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems. The outputs of the ADuM3221-EP can be operated at supply voltages from 7.6 V to 18 V.

The junction temperature of the ADuM3221-EP is specified from −55°C to +125°C.

Additional application and technical information can be found in the ADuM3221 data sheet.

FUNCTIONAL BLOCK DIAGRAM

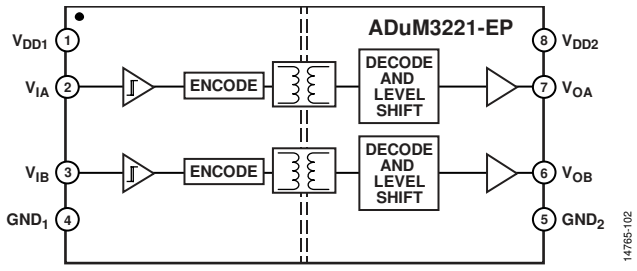

Figure 1.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,239.

Rev. 0

Document Feedback

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REVISION HISTORY

7/2016—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective ground. 4.5 V ≤ V_{DD1} ≤ 5.5 V, 7.6 V ≤ V_{DD2} ≤ 18 V, unless stated otherwise. All minimum/maximum specifications apply over T_J = −55°C to +125°C. All typical specifications are at T_J = 25°C, V_{DD1} = 5 V, V_{DD2} = 10 V. Switching specifications are tested with CMOS signal levels.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current, Two Channels, Quiescent	$I_{DDI(Q)}$		1.2	1.5	mA	
Output Supply Current, Two Channels, Quiescent	$I_{DDO(Q)}$		4.7	10	mA	
Total Supply Current, Two Channels[1]						
DC to 1 MHz						
V_{DD1} Supply Current	$I_{DD1(Q)}$		1.4	1.7	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2(Q)}$		11	17	mA	DC to 1 MHz logic signal frequency
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	0 V ≤ V_{IA}, V_{IB} ≤ V_{DD1}
Logic High Input Threshold	V_{IH}	0.7 × V_{DD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 × V_{DD1}	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	V_{DD2} − 0.1	V_{DD2}		V	I_{Ox}[2] = −20 mA, V_{Ix} = V_{IxH}[3]
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.15	V	I_{Ox}[2] = +20 mA, V_{Ix} = V_{IxL}[4]
Undervoltage Lockout, V_{DD2} Supply						
Positive Going Threshold	V_{DD2UV+}		7.0	7.5	V	
Negative Going Threshold	V_{DD2UV-}	6.0	6.5		V	
Hysteresis	V_{DD2UVH}		0.5		V	
Output Short-Circuit Pulsed Current[5]	$I_{OA(SC)}$, $I_{OB(SC)}$	2.0	4.0		A	V_{DD2} = 10 V
Output Pulsed Source Resistance	R_{OA}, R_{OB}	0.3	1.3	3.0	Ω	V_{DD2} = 10 V
Output Pulsed Sink Resistance	R_{OA}, R_{OB}	0.3	0.9	3.0	Ω	V_{DD2} = 10 V
SWITCHING SPECIFICATIONS						
Pulse Width[6]	PW	50			ns	C_L = 2 nF, V_{DD2} = 10 V
Data Rate[7]				1	MHz	C_L = 2 nF, V_{DD2} = 10 V
Propagation Delay[8]	t_{DLH}, t_{DHL}	35	45	60	ns	C_L = 2 nF, V_{DD2} = 10 V
	t_{DLH}, t_{DHL}	36	50	68	ns	C_L = 2 nF, V_{DD2} = 7.6 V
Propagation Delay Skew[9]	t_{PSK}			12	ns	C_L = 2 nF, V_{DD2} = 10 V
Channel to Channel Matching[10]	t_{PSKCD}		1	5	ns	C_L = 2 nF, V_{DD2} = 10 V
	t_{PSKCD}		1	7	ns	C_L = 2 nF, V_{DD2} = 7.6 V
Output Rise/Fall Time (10% to 90%)	t_R/t_F	14	20	25	ns	C_L = 2 nF, V_{DD2} = 10 V
Dynamic Input Supply Current per Channel	$I_{DDI(D)}$		0.05		mA/Mbps	V_{DD2} = 10 V
Dynamic Output Supply Current per Channel	$I_{DDO(D)}$		1.5		mA/Mbps	V_{DD2} = 10 V
Refresh Rate	f_r		1.2		Mbps	

[1] The supply current values for both channels are combined when running at identical data rates. Output supply current values are specified with no output load present. See Figure 8 and Figure 9 for total V_{DD1} and V_{DD2} supply currents as a function of frequency.
[2] I_{Ox} is the Channel x output current, where x = A or B.
[3] V_{IxH} is the input side logic high.
[4] V_{IxL} is the input side logic low.
[5] Short-circuit duration less than 1 µs. Average power must conform to the limit shown in the Absolute Maximum Ratings section.
[6] The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.
[7] The maximum data rate is the fastest data rate at which the specified timing parameter is guaranteed.
[8] t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 10% threshold of the V_{Ox} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the V_{Ox} signal.
[9] t_{PSK} is the magnitude of the worst case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[10] Channel to channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All voltages are relative to their respective ground. 3.0 V ≤ V_{DD1} ≤ 3.6 V, 7.6 V ≤ V_{DD2} ≤ 18 V, unless stated otherwise. All minimum/maximum specifications apply over T_J = −55°C to +125°C. All typical specifications are at T_J = 25°C, V_{DD1} = 3.3 V, V_{DD2} = 10 V. Switching specifications are tested with CMOS signal levels.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current, Two Channels, Quiescent	$I_{DDI(Q)}$		0.7	1.0	mA	
Output Supply Current, Two Channels, Quiescent	$I_{DDO(Q)}$		4.7	10	mA	
Total Supply Current, Two Channels[1]						
DC to 1 MHz						
V_{DD1} Supply Current	$I_{DD1(Q)}$		0.8	1.0	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2(Q)}$		11	17	mA	DC to 1 MHz logic signal frequency
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	0 V ≤ V_{IA}, V_{IB} ≤ V_{DD1}
Logic High Input Threshold	V_{IH}	0.7 × V_{DD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 × V_{DD1}	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	V_{DD2} − 0.1	V_{DD2}		V	I_{Ox}[2] = −20 mA, V_{Ix} = V_{IxH}[3]
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.15	V	I_{Ox}[2] = +20 mA, V_{Ix} = V_{IxL}[4]
Undervoltage Lockout, V_{DD2} Supply						
Positive Going Threshold	V_{DD2UV+}		7.0	7.5	V	
Negative Going Threshold	V_{DD2UV-}	6.0	6.5		V	
Hysteresis	V_{DD2UVH}		0.5		V	
Output Short-Circuit Pulsed Current[5]	$I_{OA(SC)}$, $I_{OB(SC)}$	2.0	4.0		A	V_{DD2} = 10 V
Output Pulsed Source Resistance	R_{OA}, R_{OB}	0.3	1.3	3.0	Ω	V_{DD2} = 10 V
Output Pulsed Sink Resistance	R_{OA}, R_{OB}	0.3	0.9	3.0	Ω	V_{DD2} = 10 V
SWITCHING SPECIFICATIONS						
Pulse Width[6]	PW	50			ns	C_L = 2 nF, V_{DD2} = 10 V
Data Rate[7]				1	MHz	C_L = 2 nF, V_{DD2} = 10 V
Propagation Delay[8]	t_{DLH}, t_{DHL}	36	48	62	ns	C_L = 2 nF, V_{DD2} = 10 V
	t_{DLH}, t_{DHL}	37	53	72	ns	C_L = 2 nF, V_{DD2} = 7.6 V
Propagation Delay Skew[9]	t_{PSK}			12	ns	C_L = 2 nF, V_{DD2} = 10 V
Channel to Channel Matching[10]	t_{PSKCD}		1	5	ns	C_L = 2 nF, V_{DD2} = 10 V
Output Rise/Fall Time (10% to 90%)	t_R/t_F	14	20	25	ns	C_L = 2 nF, V_{DD2} = 10 V
	t_R/t_F	14	22	28	ns	C_L = 2 nF, V_{DD2} = 7.6 V
Dynamic Input Supply Current per Channel	$I_{DDI(D)}$		0.025		mA/Mbps	V_{DD2} = 10 V
Dynamic Output Supply Current per Channel	$I_{DDO(D)}$		1.5		mA/Mbps	V_{DD2} = 10 V
Refresh Rate	f_r		1.1		Mbps	

[1] The supply current values for both channels are combined when running at identical data rates. Output supply current values are specified with no output load present. See Figure 8 and Figure 9 for total V_{DD1} and V_{DD2} supply currents as a function of frequency.
[2] I_{Ox} is the Channel x output current, where x = A or B.
[3] V_{IxH} is the input side logic high.
[4] V_{IxL} is the input side logic low.
[5] Short-circuit duration less than 1 µs. Average power must conform to the limit shown in the Absolute Maximum Ratings section.
[6] The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.
[7] The maximum data rate is the fastest data rate at which the specified timing parameter is guaranteed.
[8] t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 10% threshold of the V_{Ox} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the V_{Ox} signal.
[9] t_{PSK} is the magnitude of the worst case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[10] Channel to channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		1.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction to Case Thermal Resistance, Side 1	θ_{JCI}		46		°C/W	Thermocouple located at center of package underside
IC Junction to Case Thermal Resistance, Side 2	θ_{JCO}		41		°C/W	Thermocouple located at center of package underside
IC Junction to Ambient Thermal Resistance	θ_{JA}		85		°C/W	Thermocouple located at center of package underside

[1] The device is considered a 2-terminal device; Pin 1 through Pin 4 are shorted together, and Pin 5 through Pin 8 are shorted together.

REGULATORY INFORMATION

The ADuM3221-EP is approved by the organizations listed in Table 4.

Table 4.

UL	CSA (Pending)	VDE (Pending)
Recognized Under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single/Basic 2500 V rms Isolation Voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage Functional insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM3221-EP is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 5 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM3221-EP is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 second (partial discharge detection limit = 5 pC). An asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 5.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	4.90 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.01 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking on the package denotes DIN V VDE V 0884-10 approval for a 560 V peak working voltage.

Table 6.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	V_{PR}	1050	V peak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC	V_{PR}	896	V peak
After Input and/or Safety Tests Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC	V_{PR}	672	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 sec	V_{TR}	4000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	160	mA
Side 2 Current		I_{S2}	47	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

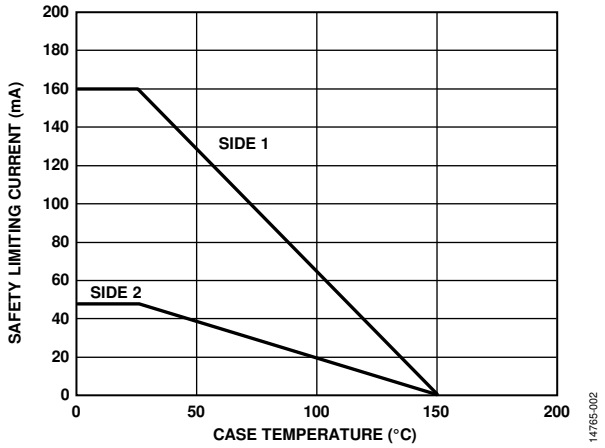

Figure 2. Thermal Derating Curve; Dependence of Safety Limiting Values on Case Temperature, per DIN V VDE V 0884-10 (Safety Limiting Current Is Defined as the Average Current at Maximum V_{DD})

RECOMMENDED OPERATING CONDITIONS

Table 7.

Parameter	Symbol	Min	Max	Unit
Operating Junction Temperature	T_J	−55	+125	°C
Supply Voltages[1]	V_{DD1}	3.0	5.5	V
	V_{DD2}	7.6	18	V
V_{DD1} Rise Time	t_{VDD1}		1	V/µs
Common-Mode Transient Immunity, Input to Output		−25	+25	kV/µs
Input Signal Rise and Fall Times			1	ms

[1] All voltages are relative to their respective ground.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Operating Temperature (T_J)	−55°C to +150°C
Supply Voltage Ranges[1]	
V_{DD1}	−0.5 V to +7.0 V
V_{DD2}	−0.5 V to +20 V
Input Voltage Range (V_{IA}, V_{IB})[1, 2]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage Range (V_{OA}, V_{OB})[1, 2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin (I_O)[3]	−23 mA to +23 mA
Common-Mode Transients, (CM_H, CM_L)[4]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.
[3] See Figure 2 for information about maximum allowable current for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 9. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Bipolar Voltage	565	V peak	50-year minimum lifetime
AC Unipolar Voltage	1131	V peak	50-year minimum lifetime
DC Voltage	1131	V peak	50-year minimum lifetime

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

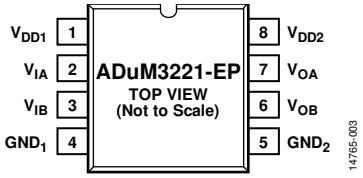

Figure 3. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. GND_1 is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. GND_2 is the g round reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2, 7.6 V to 18 V.

Table 11. Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
Low	Low	Powered	Powered	Low	Low	
Low	High	Powered	Powered	Low	High	
High	Low	Powered	Powered	High	Low	
High	High	Powered	Powered	High	High	
Don't care	Don't care	Unpowered	Powered	Low	Low	Outputs return to the input state within 1 µs of V_{DD1} power restoration.
Don't care	Don't care	Powered	Unpowered	Low	Low	Outputs return to the input state within 1 µs of V_{DD2} power restoration.

TYPICAL PERFORMANCE CHARACTERISTICS

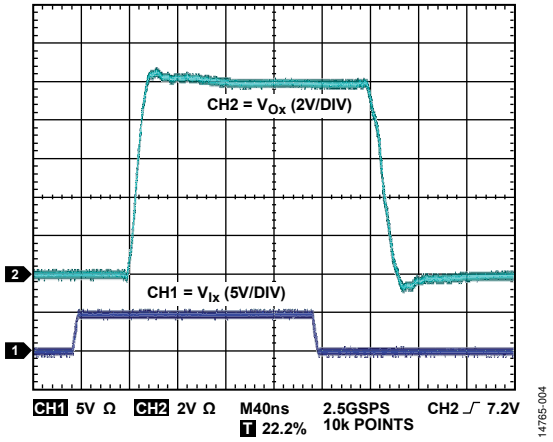

Figure 4. Output Waveform for 2 nF Load with 10 V Output Supply

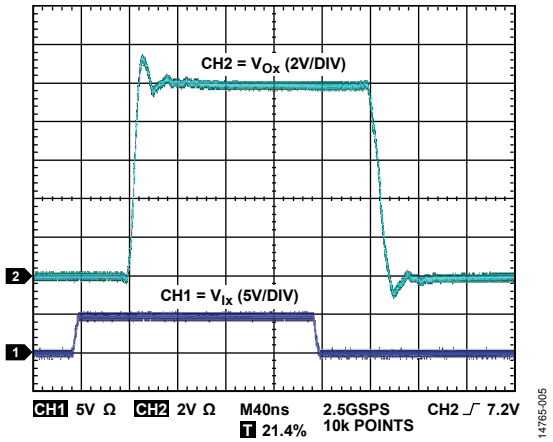

Figure 5. Output Waveform for 1 nF Load with 10 V Output Supply

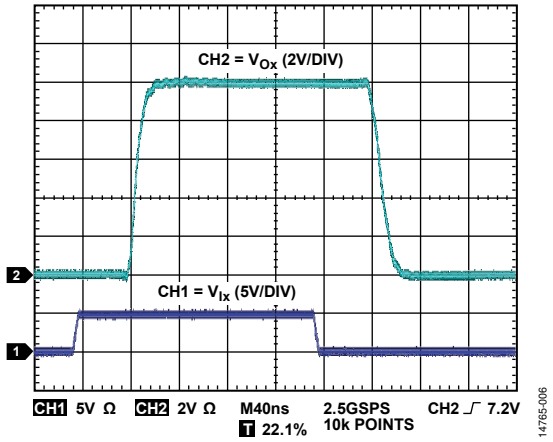

Figure 6. Output Waveform for 1 nF Load with 5 Ω Series Resistance and 10 V Output Supply

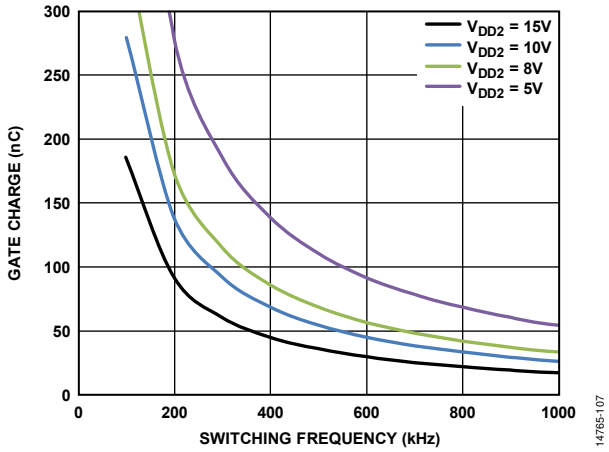

Figure 7. Maximum Load; Gate Charge vs. Switching Frequency (R_{GATE} = 1 Ω)

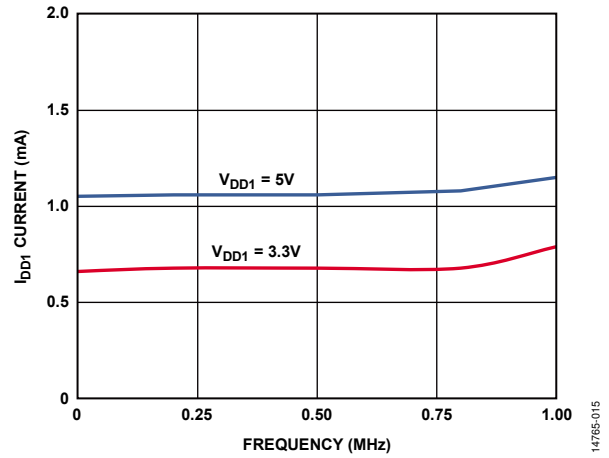

Figure 8. I_{DD1} Current vs. Frequency

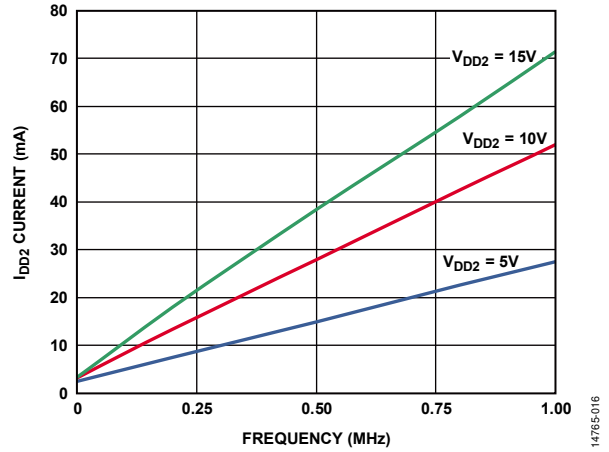

Figure 9. I_{DD2} Current vs. Frequency with 2 nF Load

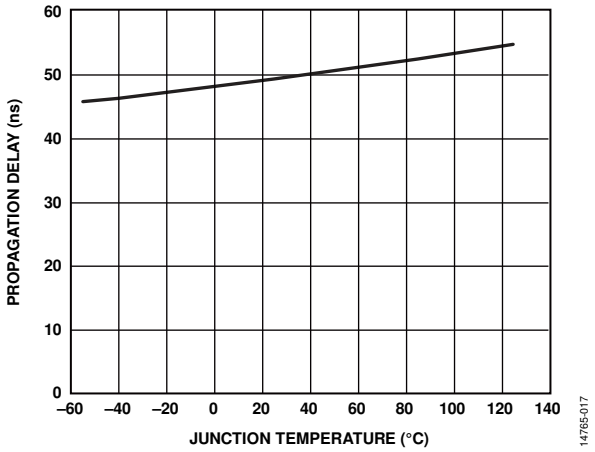

Figure 10. Propagation Delay vs. Junction Temperature

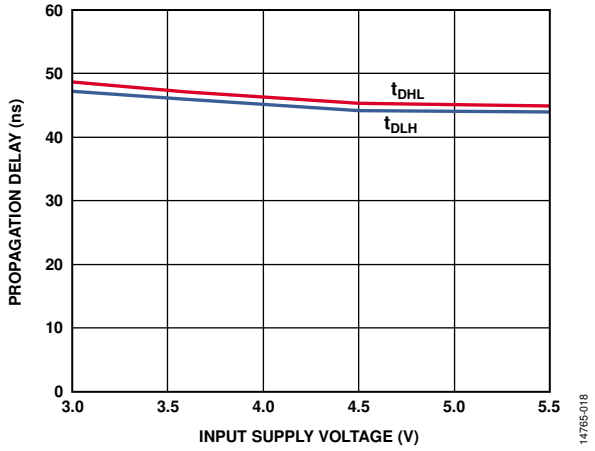

Figure 11. Propagation Delay vs. Input Supply Voltage, V_{DD2} = 10 V

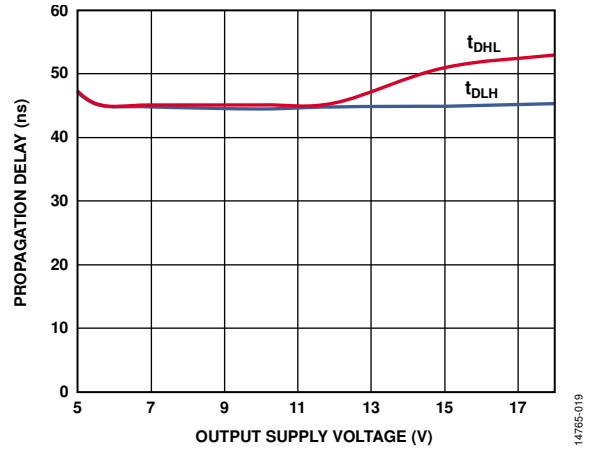

Figure 12. Propagation Delay vs. Output Supply Voltage, V_{DD1} = 5 V

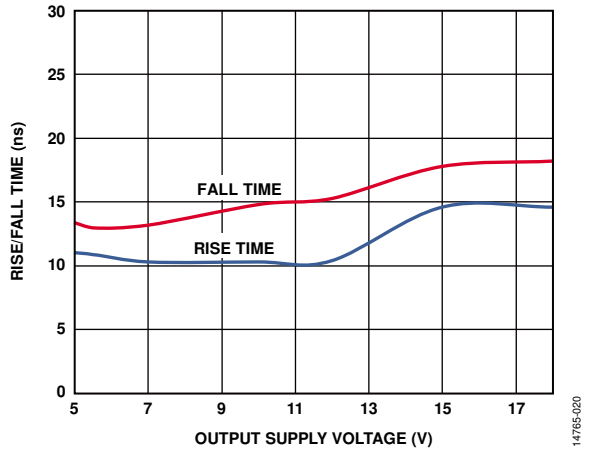

Figure 13. Rise/Fall Time vs. Output Supply Voltage

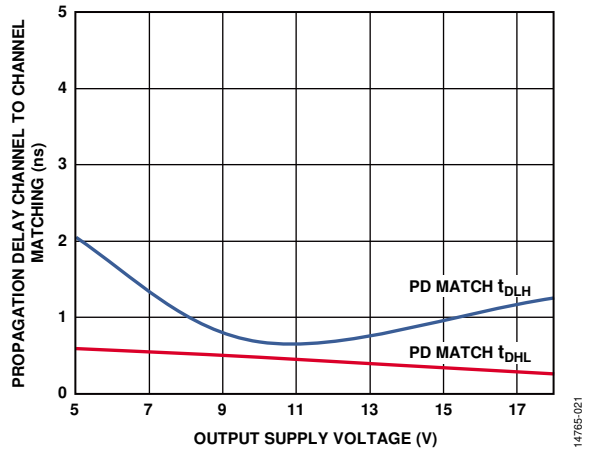

Figure 14. Propagation Delay Channel to Channel Matching vs. Output Supply Voltage

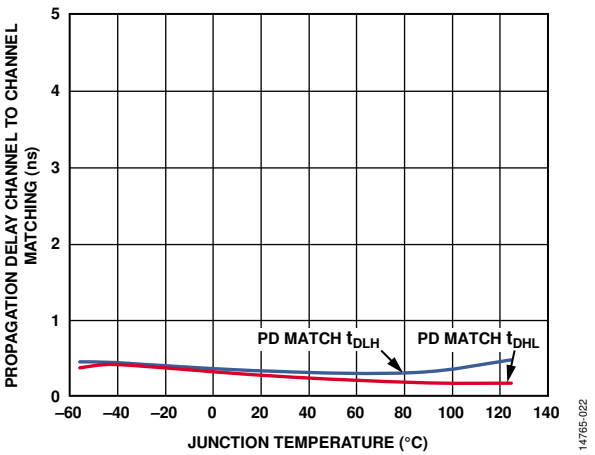

Figure 15. Propagation Delay Channel to Channel Matching vs. Junction Temperature, V_{DD2} = 10 V

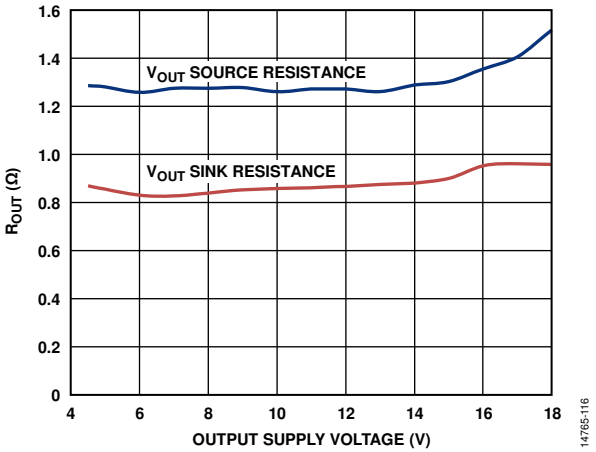

Figure 16. Output Source Resistance (R_{OUT}) vs. Output Supply Voltage

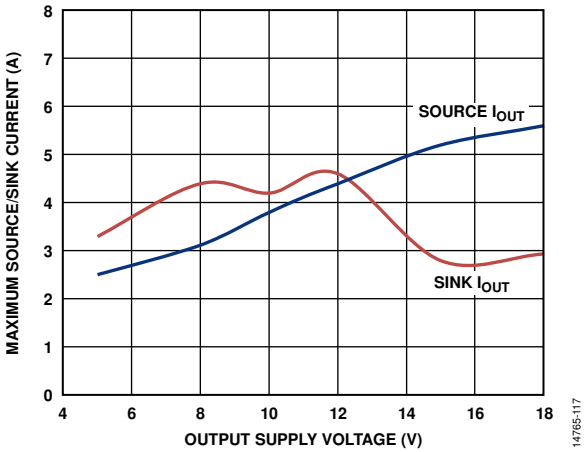

Figure 17. Maximum Source/Sink Current vs. Output Supply Voltage

OUTLINE DIMENSIONS

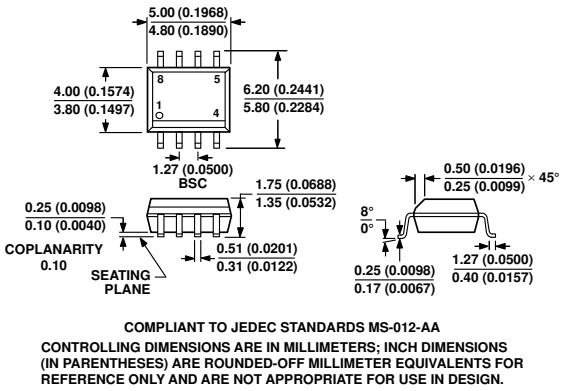

Figure 18. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	No. of Inputs, V_{DD1} Side	Maximum Data Rate (MHz)	Maximum Propagation Delay, 5 V (ns)	Minimum V_{DD2} Operating Voltage (V)	Junction Temperature Range	Package Description	Package Option
ADuM3221TRZ-EP	2	1	60	7.6	−55°C to +125°C	8-Lead SOIC_N	R-8
ADuM3221TRZ-EP-RL7	2	1	60	7.6	−55°C to +125°C	8-Lead SOIC_N	R-8

[1] Z = RoHS Compliant Part.

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