ON Semiconductor

Is Now

To learn more about onsemi™, please visit our website at www.onsemi.com

ON Semiconductor®

FAN5361
6 MHz, 600 mA / 750 mA Synchronous Buck Regulator

Features

- 6 MHz Fixed-Frequency Operation
- 35 µA Typical Quiescent Current
- Best-in-Class Load Transient Response
- Best-in-Class Efficiency
- 600 mA or 750 mA Output Current Capability
- 2.3 V to 5.5 V Input Voltage Range
- 1.0 to 1.90 V Fixed Output Voltage
- Low Ripple Light-Load PFM Mode
- Forced PWM and External Clock Synchronization
- Internal Soft-Start
- Input Under-Voltage Lockout (UVLO)
- Thermal Shutdown and Overload Protection
- 6-bump WLCSP, 0.4 mm Pitch
- 6-pin 2 x 2 mm UMLP

Applications

- Cell Phones, Smart Phones
- Tablets, Netbooks®, Ultra-Mobile PCs
- 3G, LTE, WiMAX™, WiBro®, and WiFi® Data Cards
- Gaming Devices, Digital Cameras DC/DC Micro Modules

Description

The FAN5361 is a 600 mA or 750 mA, step-down, switching voltage regulator that delivers a fixed output from a 2.3 V to 5.5 V input voltage supply. Using a proprietary architecture with synchronous rectification, the FAN5361 is capable of delivering a peak efficiency of 92%, while maintaining efficiency over 80% at load currents as low as 1 mA.

The regulator operates at a nominal fixed frequency of 6 MHz, which reduces the value of the external components to 470 nH for the output inductor and 4.7 µF for the output capacitor. The PWM modulator can be synchronized to an external frequency source.

At moderate and light loads, pulse frequency modulation is used to operate the device in power-save mode with a typical quiescent current of 35 µA. Even with such a low quiescent current, the part exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed-frequency control, operating at 6 MHz. In shutdown mode, the supply current drops below 1 µA, reducing power consumption. For applications that require minimum ripple or fixed frequency, PFM mode can be disabled using the MODE pin.

The FAN5361 is available in 6-bump, 0.4 mm pitch, Wafer-Level Chip-Scale Package (WLCSP) and a 6-lead 2 x 2 mm ultra-thin MLP package (UMLP).

Typical Applications

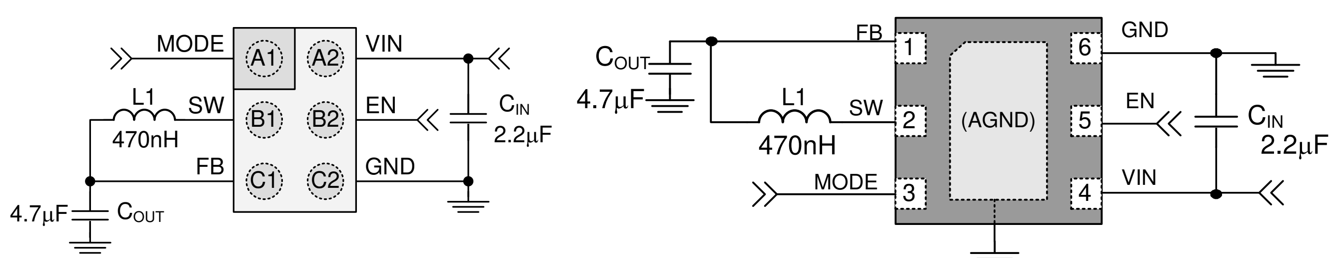


Figure 1. Typical Applications

All trademarks are the property of their respective owners.

Ordering Information

Part Number	Output Voltage(1)	Package	Temperature Range	Packing
FAN5361UC123X*	1.233 V	WLCSP-6, 0.4 mm Pitch	–40 to +85°C	Tape and Reel
FAN5361UC182X	1.820 V			
FAN5361UC19X	1.900 V			
FAN5361UMP123X	1.233 V	6-Lead, 2 x 2 mm UMLP		
FAN5361UMP15X	1.500 V			
FAN5361UMP182X	1.820 V			

Note:
1. Other voltage options available on request. Contact a ON Semiconductor representative.

* This device is End of Life. Please contact sales for additional information and assistance with replacement devices.

Pin Configurations

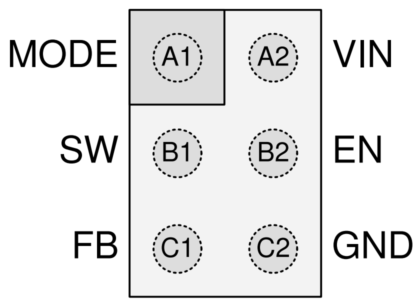


Figure 2. WLCSP, Bumps Facing Down

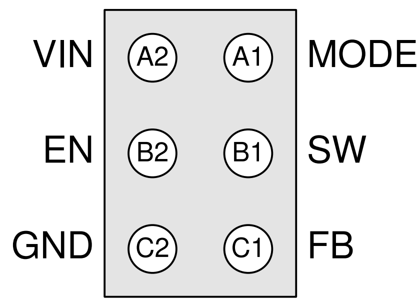


Figure 3. WLCSP, Bumps Facing Up

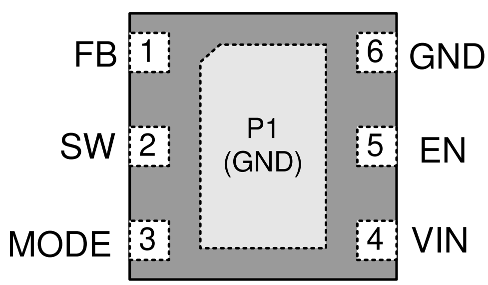


Figure 4. UMLP, Leads Facing Down

Pin Definitions

Pin #		Name	Description
WLCSP	UMLP		
A1	3	MODE	**MODE**. Logic 1 on this pin forces the IC to stay in PWM mode. A logic 0 allows the IC to automatically switch to PFM during light loads. The regulator also synchronizes its switching frequency to four times the frequency provided on this pin. Do not leave this pin floating. When tying HIGH, use at least 1kΩ series resistor if V_{IN} is expected to exceed 4.5 V.
B1	2	SW	**Switching Node**. Connect to output inductor.
C1	1	FB	**Feedback / V_{OUT}**. Connect to output voltage.
C2	6	GND	**Ground**. Power and IC ground. All signals are referenced to this pin.
B2	5	EN	**Enable**. The device is in shutdown mode when voltage to this pin is <0.4 V and enabled when >1.2 V. Do not leave this pin floating. When tying HIGH, use at least 1 kΩ series resistor if V_{IN} is expected to exceed 4.5 V.
A2	4	VIN	**Input Voltage**. Connect to input power source.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	Input Voltage		–0.3	7.0	V
V_{SW}	Voltage on SW Pin		–0.3	V_{IN} + 0.3(2)	V
V_{CTRL}	EN and MODE Pin Voltage		–0.3	V_{IN} + 0.3(2)	V
	Other Pins		–0.3	V_{IN} + 0.3(2)	V
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	4.0		kV
		Charged Device Model per JESD22-C101	1.5		
T_J	Junction Temperature		–40	+150	°C
T_{STG}	Storage Temperature		–65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Note:
2. Lesser of 7 V or V_{IN}+0.3 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Range	2.3		5.5	V
I_{OUT}	Output Current	0		600	mA
L	Inductor		0.47		µH
C_{IN}	Input Capacitor		2.2		µF
C_{OUT}	Output Capacitor	1.6	4.7	12.0	µF
T_A	Operating Ambient Temperature	–40		+85	°C
T_J	Operating Junction Temperature	–40		+125	°C

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 1s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperate T_A.

Symbol	Parameter		Typical	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	WLCSP	150	°C/W
		UMLP	49	°C/W

Electrical Characteristics

Minimum and maximum values are at $V_{IN} = V_{EN} = 2.3V$ to 5.5V, $V_{MODE} = 0V$ (AUTO Mode), T_A = -40°C to +85°C; circuit of Figure 1, unless otherwise noted. Typical values are at T_A = 25°C, $V_{IN} = V_{EN} = 3.6$ V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supplies						
I_Q	Quiescent Current	No Load, Not Switching		35	55	µA
		PWM Mode		6		mA
$I_{(SD)}$	Shutdown Supply Current	V_{IN} = 3.6 V, EN = GND		0.05	1.00	µA
V_{UVLO}	Under-Voltage Lockout Threshold	Rising V_{IN}		2.15	2.25	V
V_{UVHYST}	Under-Voltage Lockout Hysteresis			150		mV
Logic Inputs: EN and MODE Pins						
V_{IH}	Enable HIGH-Level Input Voltage		1.2			V
V_{IL}	Enable LOW-Level Input Voltage				0.4	V
V_{LHYST}	Logic Input Hysteresis Voltage			100		mV
I_{IN}	Enable Input Leakage Current	Pin to V_{IN} or GND		0.01	1.00	µA
Switching and Synchronization						
f_{SW}	Switching Frequency(3)	V_{IN} = 3.6 V, T_A = 25°C	5.4	6.0	6.6	MHz
f_{SYNC}	MODE Synchronization Range(3)	Square Wave at MODE Input	1.3	1.5	1.7	MHz
Regulation						
V_O	Output Voltage Accuracy, 1.900 V	I_{LOAD} = 0 to 750 mA(4)	1.832	1.900	1.957	V
	1.900 V	PWM Mode(4)	1.832	1.900	1.938	V
	1.820 V	I_{LOAD} = 0 to 600 mA	1.784	1.820	1.875	V
	1.820 V	PWM Mode	1.784	1.820	1.856	V
	1.500 V	I_{LOAD} = 0 to 600 mA	1.470	1.500	1.545	V
	1.500 V	PWM Mode	1.470	1.500	1.530	V
	1.233 V	I_{LOAD} = 0 to 600 mA	1.207	1.233	1.272	V
	1.233 V	PWM Mode	1.207	1.233	1.259	V
t_{SS}	Soft-Start	From EN Rising Edge		180	300	µs
Output Driver						
$R_{DS(on)}$	PMOS On Resistance	$V_{IN} = V_{GS}$ = 3.6 V		350		mΩ
	NMOS On Resistance	$V_{IN} = V_{GS}$ = 3.6 V		225		mΩ
$I_{LIM(OL)}$	PMOS Open-Loop Peak Current Limit(5)	V_{OUT} = 1.233 V, 1.5 V, 1.82 V	900	1100	1250	mA
		V_{OUT} = 1.9 V	1180	1375	1550	mA
T_{TSD}	Thermal Shutdown	CCM Only		150		°C
T_{HYS}	Thermal Shutdown Hysteresis			15		°C

Notes:

3. Limited by the effect of t_{OFF} minimum *(see Figure 14 and Figure 15 in Typical Performance Characteristics)*.
4. Output voltage accuracy minimum: 1.862 V for V_{IN} 2.7 to 5.5 V on 1.9 V option.
5. *Refer to Operation Description and Typical Characteristics for closed-loop data.*

Typical Performance Characteristics

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6$ V, $V_{MODE} = 0$ V (AUTO Mode), $V_{OUT} = 1.82$ V, $T_A = 25°C$.

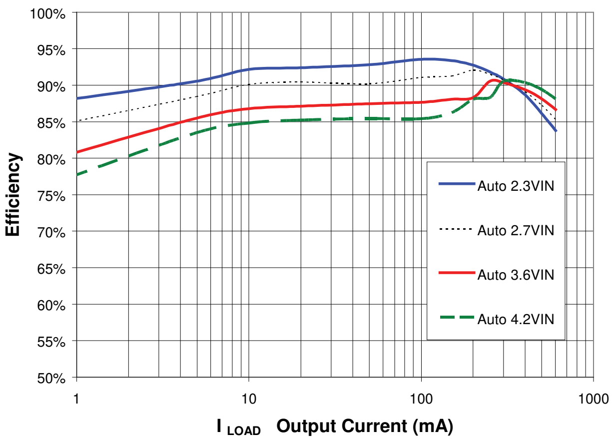


Figure 5. Efficiency vs. Load Current and Input Supply

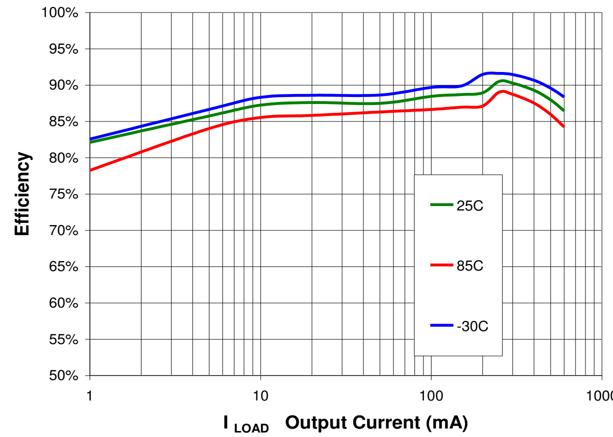


Figure 6. Efficiency vs. Load Current and Temperature

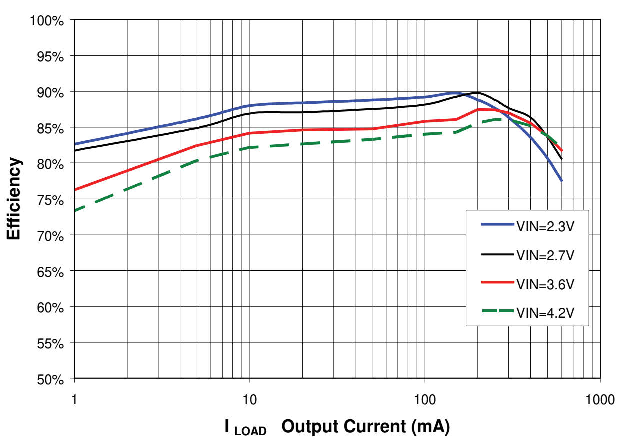


Figure 7. 1.233 V_{OUT} Efficiency vs. Load Current and Supply

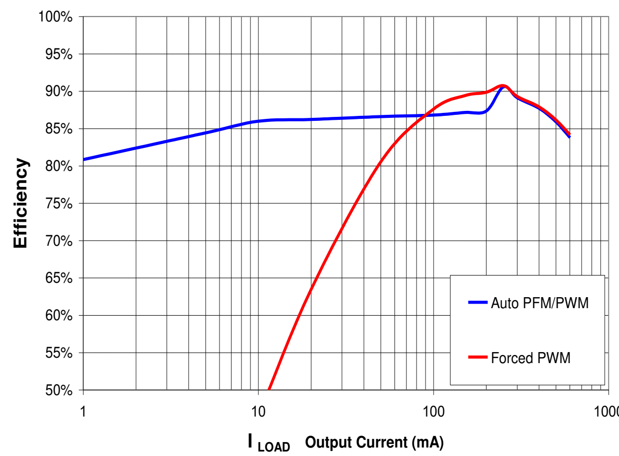


Figure 8. Efficiency, Auto PWM/PFM vs. Forced PWM

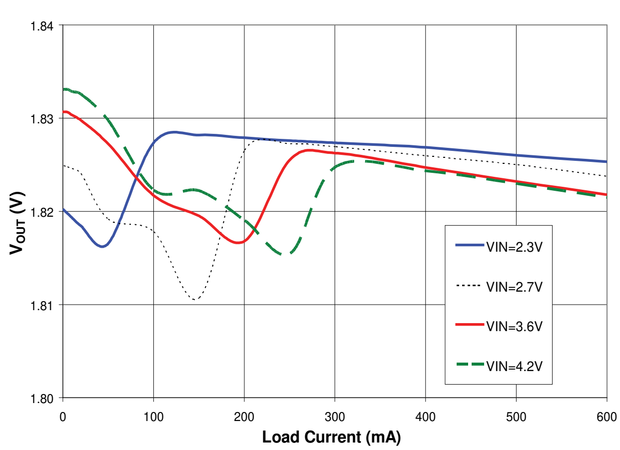


Figure 9. Load Regulation

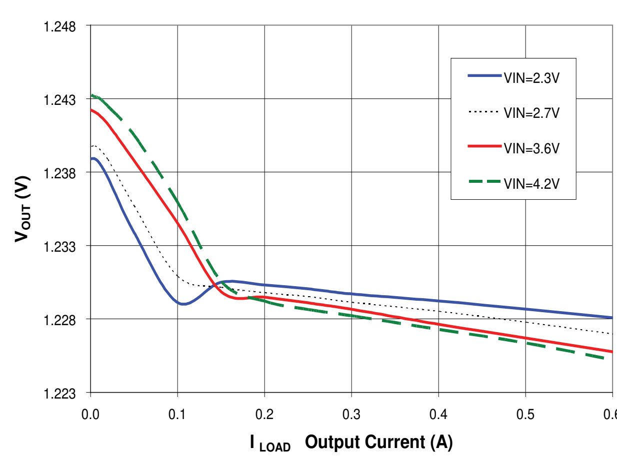


Figure 10. 1.233 V_{OUT} Load Regulation vs. Input Supply

Typical Performance Characteristics (Continued)

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6$ V, $V_{MODE} = 0$ V (AUTO M

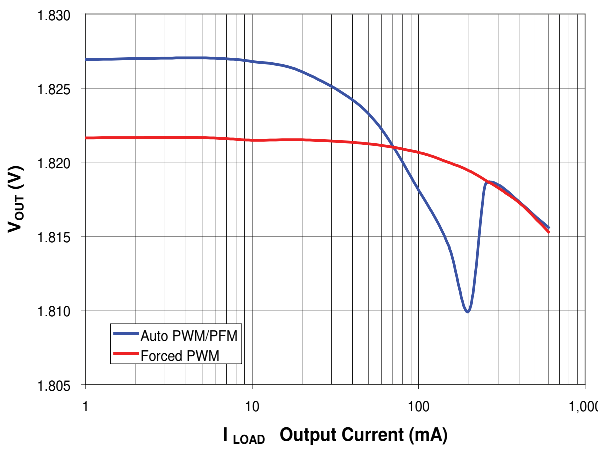


Figure 11. Load Regulation, Auto PFM / PWM and Forced PWM

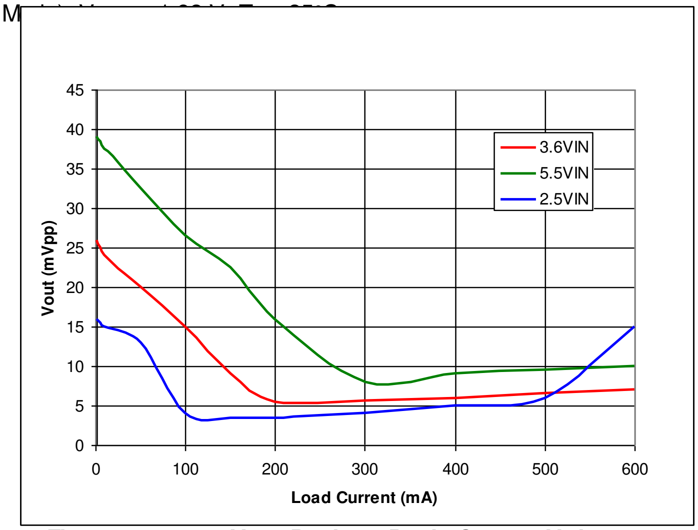


Figure 12. 1.82 V_{OUT} Peak-to-Peak Output Voltage Ripple

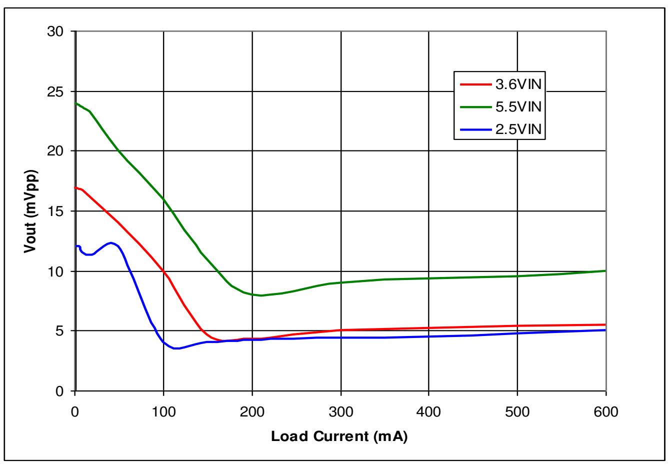


Figure 13. 1.233 V_{OUT} Peak-to-Peak Output Voltage Ripple

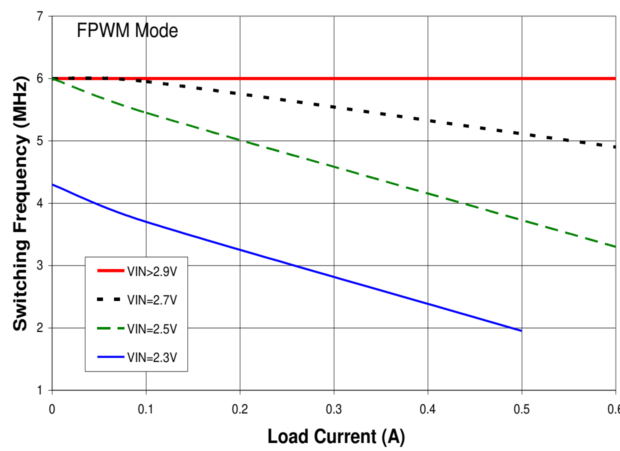


Figure 14. Effect of $t_{OFF(MIN)}$ on Reducing Switching Frequency

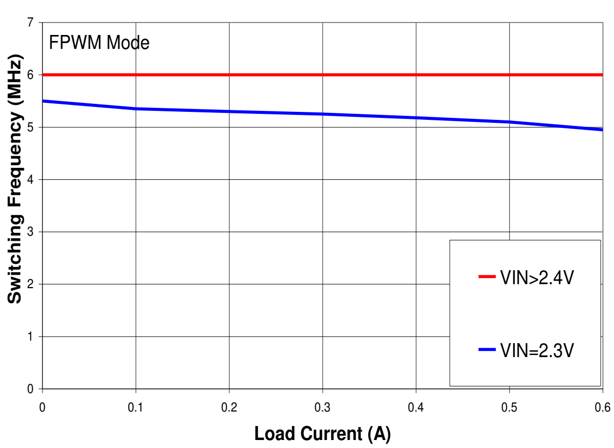


Figure 15. 1.233 V_{OUT} Effect of $t_{OFF(MIN)}$ on Reducing Switching Frequency

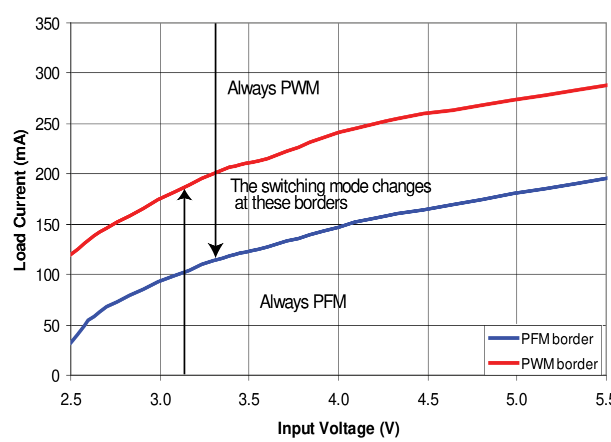


Figure 16. PFM / PWM Boundaries

Typical Performance Characteristics (Continued)

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6$ V, $V_{MODE} = 0$ V (AUTO Mode), $V_{OUT} = 1.82$ V, $T_A = 25°C$.

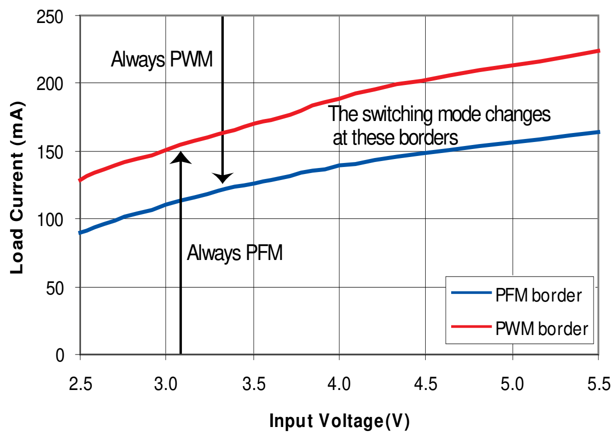


Figure 17. 1.233 V_{OUT} PFM / PWM Boundaries

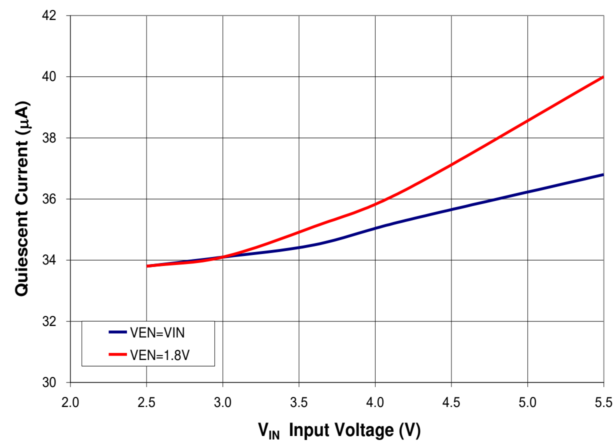


Figure 18. Quiescent Current vs. Input Voltage

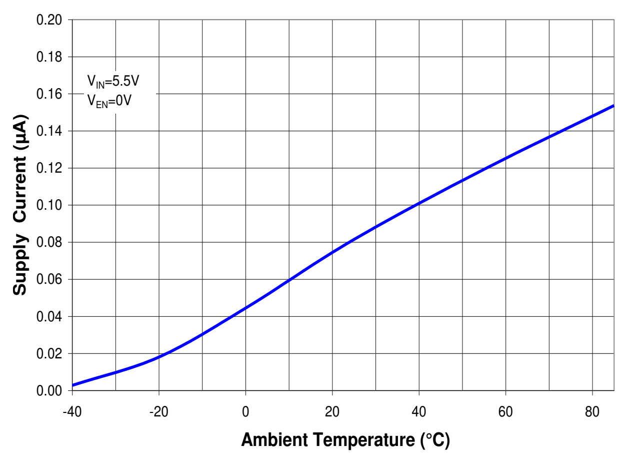


Figure 19. Shutdown Current vs. Temperature

Typical Performance Characteristics (Continued)

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6$ V, $V_{MODE} = 0$ V (AUTO Mode), $V_{OUT} = 1.82$ V, $T_A = 25°C$, 5µs/div. horizontal sweep.

Figure 20. Line Transient 3.3 V_{IN} to 3.9 V_{IN}, 50 mA Load, 10 µs/div.

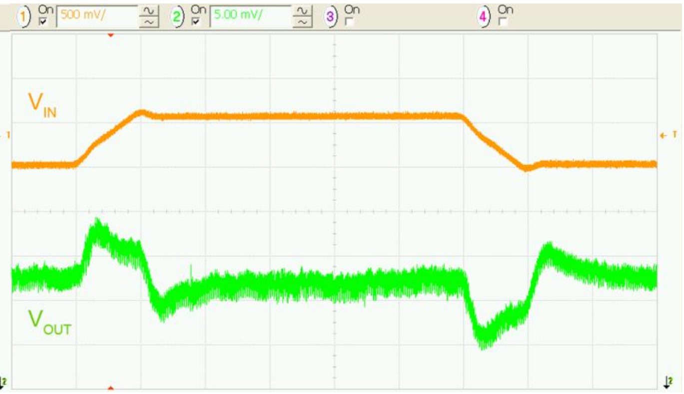


Figure 21. Line Transient 3.3 V_{IN} to 3.9 V_{IN}, 250 mA Load, 10 µs/div.

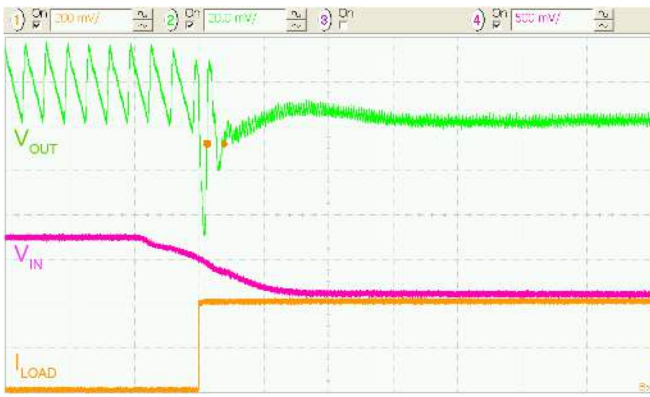


Figure 22. Combined Line/Load Transient 3.9 to 3.3 V_{IN} Combined with 40 mA to 400 mA Load Transient

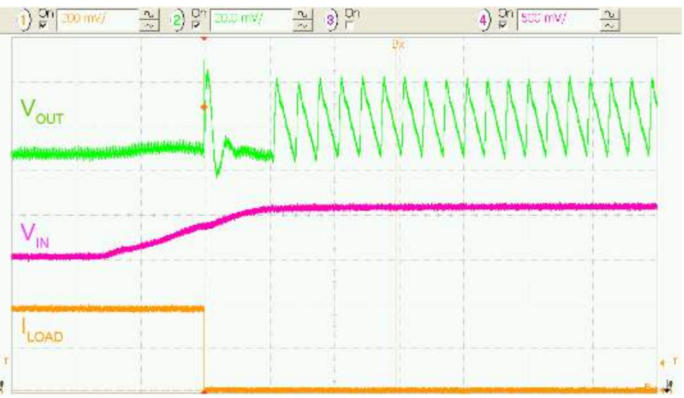


Figure 23. Combined Line/Load Transient 3.3 to 3.9 V_{IN} Combined with 400 mA to 40 mA Load Transient

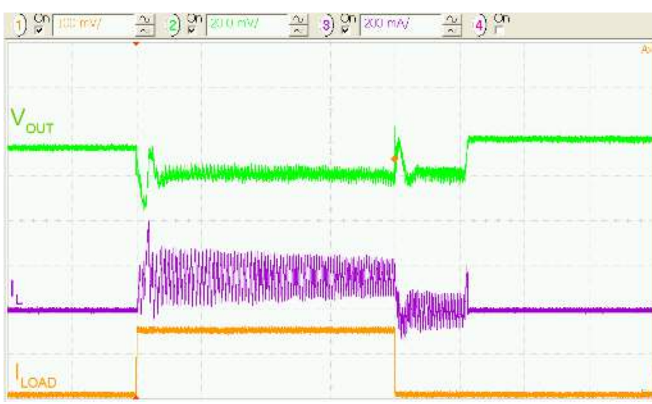


Figure 24. Load Transient 0 to 150 mA, 2.5 V_{IN}

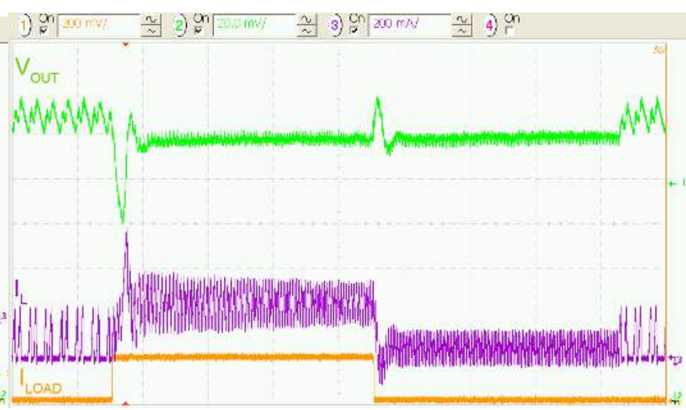


Figure 25. Load Transient 50 to 250 mA, 2.5 V_{IN}

Typical Performance Characteristics (Continued)

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6$ V, $V_{MODE} = 0$ V (AUTO Mode), $V_{OUT} = 1.82$ V, $T_A = 25°C$, 5 µs/div. horizontal sweep.

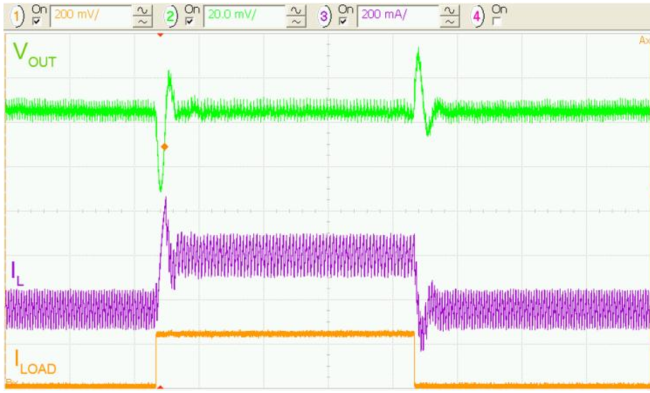


Figure 26. Load Transient 150 to 400 mA, 2.5 V_{IN}

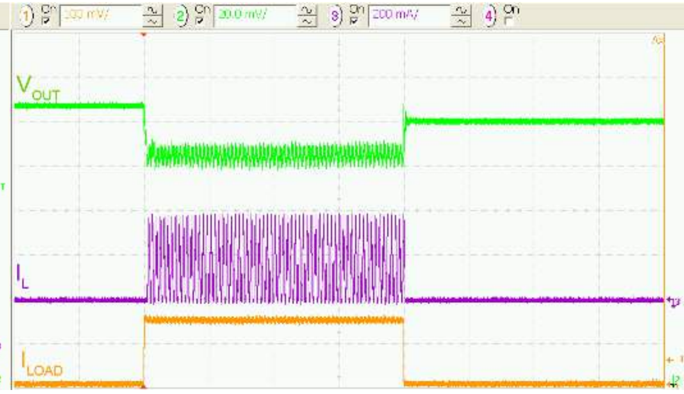


Figure 27. Load Transient 0 to 150 mA, 3.6 V_{IN}

Figure 28. Load Transient 50 to 250 mA, 3.6 V_{IN}

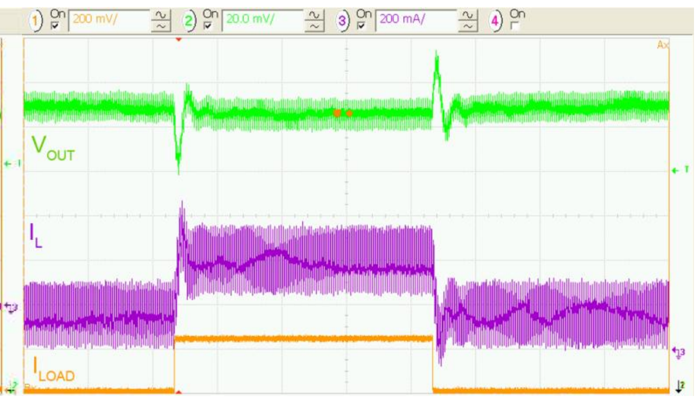


Figure 29. Load Transient 150 to 400 mA, 3.6 V_{IN}

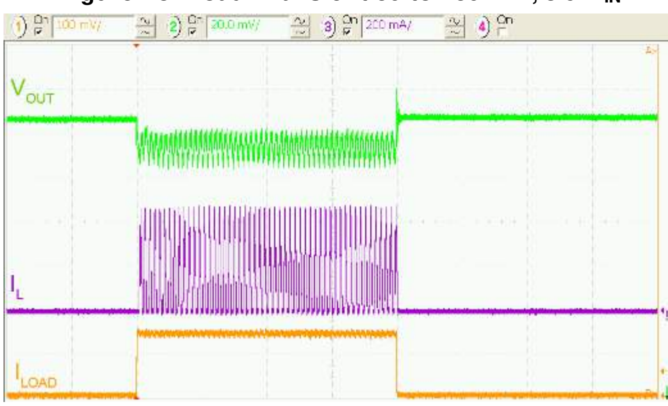


Figure 30. Load Transient 0 to 150 mA, 4.5 V_{IN}

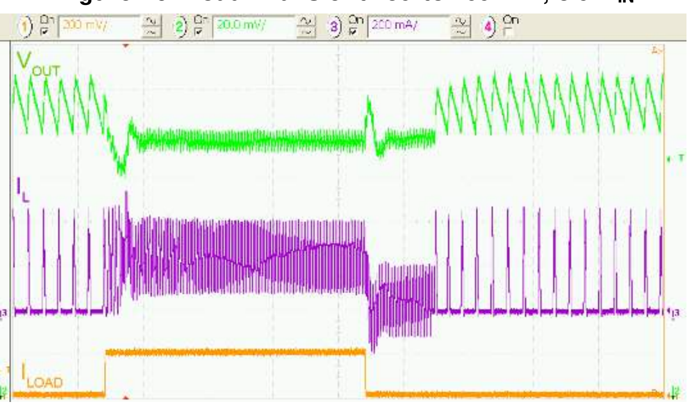


Figure 31. Load Transient 50 to 250 mA, 4.5 V_{IN}

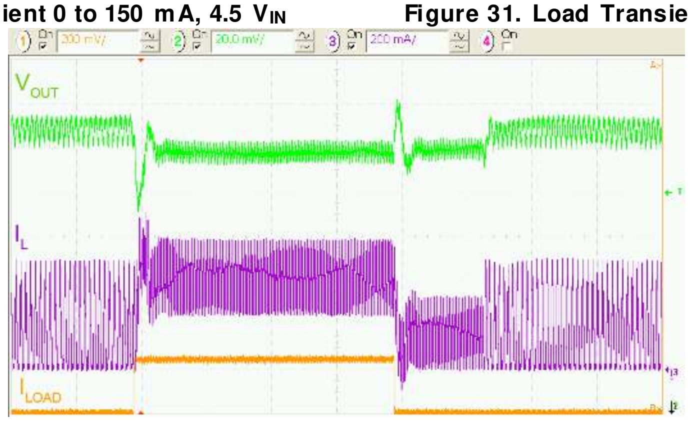


Figure 32. Load Transient 150 to 400 mA, 4.5 V_{IN}

Typical Performance Characteristics (Continued)

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6$ V, $V_{MODE} = 0$ V (AUTO Mode), $V_{OUT} = 1.82$ V, $T_A = 25°C$, 5 µs/div. horizontal sweep.

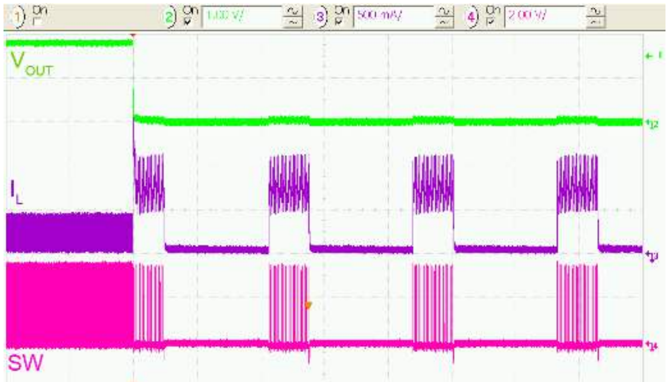


Figure 33. Metallic Short Applied at V_{OUT}, 50 µs/div.

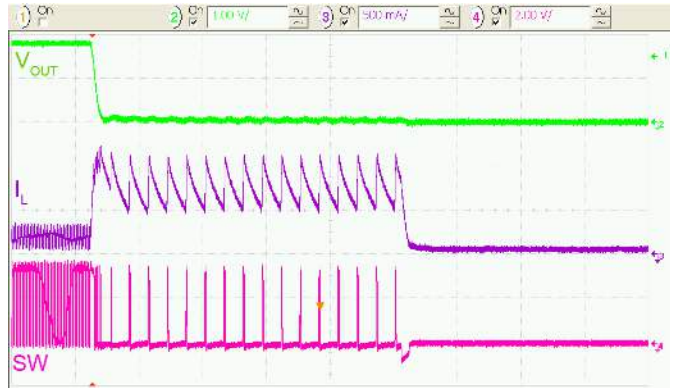


Figure 34. Metallic Short Applied at V_{OUT}

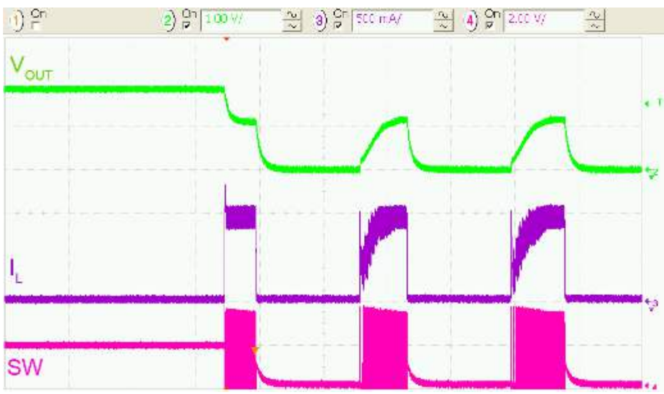


Figure 35. Over-Current Fault Response, $R_{LOAD} = 1\ \Omega$, 50 µs/div.

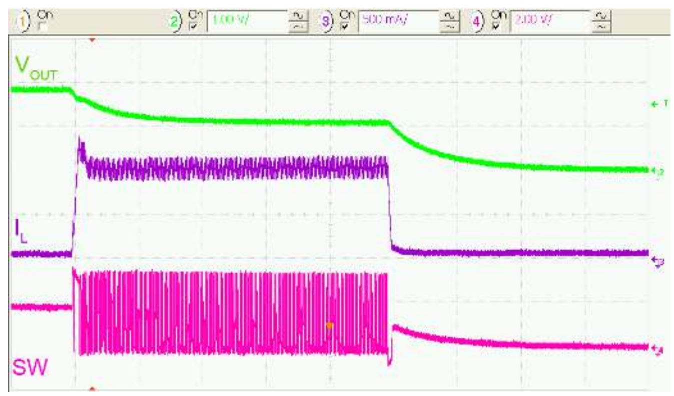


Figure 36. Over-Current Fault Response, $R_{LOAD} = 1\ \Omega$

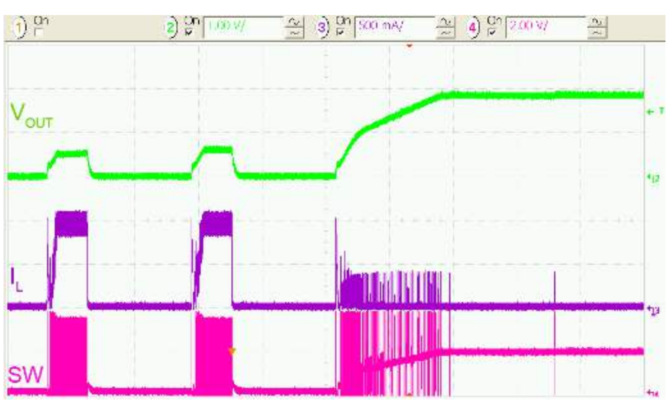


Figure 37. Overload Recovery to Light Load, 50 µs/div.

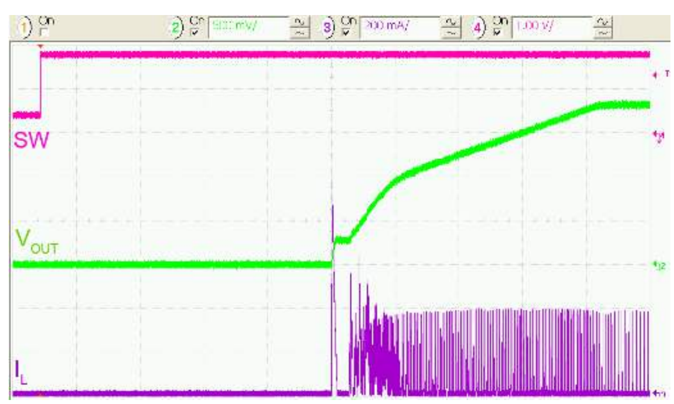


Figure 38. Soft-Start, $R_{LOAD} = 50\ \Omega$, 20 µs/div.

Typical Performance Characteristics (Continued)

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6$ V, $V_{MODE} = 0$ V (AUTO Mode), $V_{OUT} = 1.82$ V, $T_A = 25°C$.

Figure 39. SW-Node Jitter (Infinite Persistence), $I_{LOAD} = 200$ mA, 50 ns/div.

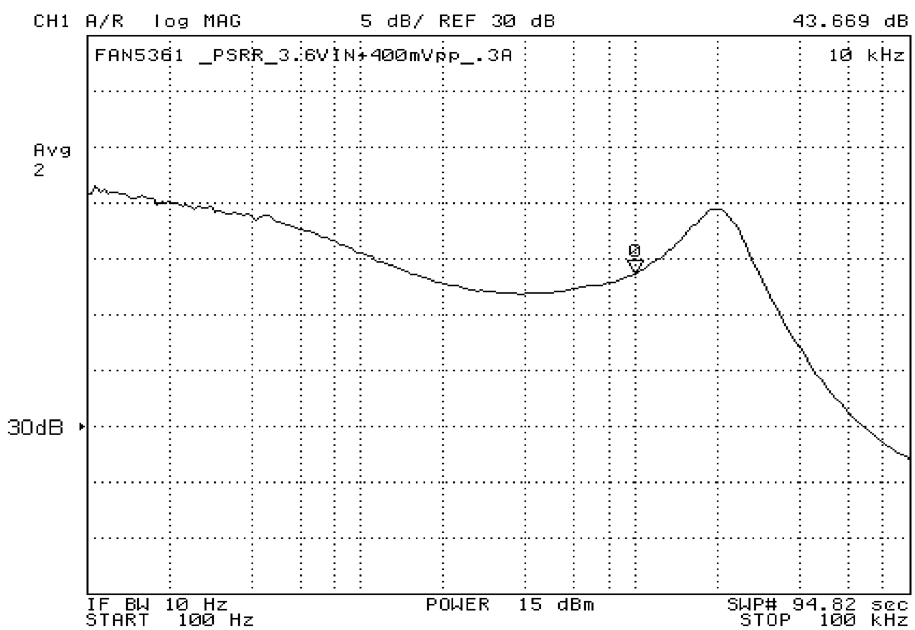


Figure 40. Power Supply Rejection Ratio at 300 mA Load

Operation Description

The FAN5361 is a 600 mA or 750 mA, step-down, switching voltage regulator that delivers a fixed output from an input voltage supply of 2.3 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN5361 is capable of delivering a peak efficiency of 92%, while maintaining efficiency over 80% at load currents as low as 1 mA. The regulator operates at a nominal frequency of 6 MHz at full load, which reduces the value of the external components to 470 nH for the inductor and 4.7 µF for the output capacitor.

Control Scheme

The FAN5361 uses a proprietary, non-linear, fixed-frequency PWM modulator to deliver a fast load transient response, while maintaining a constant switching frequency over a wide range of operating conditions. The regulator performance is independent of the output capacitor ESR, allowing for the use of ceramic output capacitors. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency loop holds the switching frequency constant over a large range of input voltages and load currents.

For very light loads, the FAN5361 operates in Discontinuous Current Mode (DCM) single-pulse PFM mode, which produces low output ripple compared with other PFM architectures. Transition between PWM and PFM is seamless, with a glitch of less than 18 mV at V_{OUT} during the transition between DCM and CCM modes.

Combined with exceptional transient response characteristics, the very low quiescent current of the controller (35 µA) maintains high efficiency; even at very light loads, while preserving fast transient response for applications requiring tight output regulation.

Enable and Soft-Start

When EN is LOW, all circuits in FAN5361 are off and the IC draws ~50 nA of current. When EN is HIGH and V_{IN} is above its UVLO threshold, the regulator begins a soft-start cycle. The output ramp during soft-start is a fixed slew rate of 50 mV/µs from 0 to 1 V_{OUT}, then 12.5 mV/µs until the output reaches its setpoint. Regardless of the state of the MODE pin, PFM mode is enabled to prevent current from being discharged from C_{OUT} if soft-start begins when C_{OUT} is charged.

The IC may fail to start if heavy load is applied during startup and/or if excessive C_{OUT} is used. This is due to the current-limit fault response, which protects the IC in the event of an over-current condition present during soft-start.

The current required to charge C_{OUT} during soft-start is commonly referred to as “displacement current” is given as:

$$I_{DISP} = C_{OUT} \bullet \frac{dV}{dt} \qquad (1)$$

where the $\frac{dV}{dt}$ term refers to the soft-start slew rate above.

To prevent shut-down during soft-start, the following condition must be met:

$$I_{DISP} + I_{LOAD} < I_{MAX(DC)} \qquad (2)$$

where $I_{MAX(DC)}$ is the maximum load current the IC is guaranteed to support (600 mA or 750 mA).

Table 1 shows combinations of C_{OUT} that allow the IC to start successfully with the minimum R_{LOAD} that can be supported.

Table 1. Minimum R_{LOAD} Values for Soft-Start with Various C_{OUT} Values

C_{OUT}	Minimum R_{LOAD}
4.7 µF, 0402	V_{OUT} / 0.60
2 X 4.7 µF, 0402	V_{OUT} / 0.60
10 µF, 0603	V_{OUT} / 0.60
10 µF, 0805	V_{OUT} / 0.50

Startup into Large C_{OUT}

Multiple soft-start cycles are required for no-load startup if C_{OUT} is greater than 15 µF. Large C_{OUT} requires light initial load to ensure the FAN5361 starts appropriately. The IC shuts down for 85 µs when I_{DISP} exceeds I_{LIMIT} for more than 21 µs of current limit. The IC then begins a new soft-start cycle. Since C_{OUT} retains its charge when the IC is off, the IC reaches regulation after multiple soft-start attempts.

MODE Pin

Logic 1 on this pin forces the IC to stay in PWM mode. A logic 0 allows the IC to automatically switch to PFM during light loads. If the MODE pin is toggled, the converter synchronizes its switching frequency to four times the frequency on the mode pin (f_{MODE}).

The MODE pin is internally buffered with a Schmitt trigger, which allows the MODE pin to be driven with slow rise and fall times. An asymmetric duty cycle for frequency synchronization is also permitted as long as the minimum time below $V_{IL(MAX)}$ or above $V_{IH(MAX)}$ is 100 ns.

Current Limit, Fault Shutdown, and Restart

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high-side switch. Upon reaching this point, the high-side switch turns off, preventing high currents from causing damage. The regulator continues to limit the current cycle-by-cycle. After 21 µs of current limit, the regulator triggers an over-current fault, causing the regulator to shut down for about 85µs before attempting a restart.

If the fault was caused by short circuit, the soft-start circuit attempts to restart and produces an over-current fault after about 32 µs, which results in a duty cycle of less than 30%, limiting power dissipation.

The closed-loop peak-current limit, $I_{LIM(PK)}$, is not the same as the open-loop tested current limit, $I_{LIM(OL)}$, in the Electrical Characteristics table. This is primarily due to the effect of propagation delays of the IC current limit comparator.

Under-Voltage Lockout (UVLO)

When EN is HIGH, the under-voltage lockout keeps the part from operating until the input supply voltage rises high enough to properly operate. This ensures no misbehavior of the regulator during startup or shutdown.

Thermal Shutdown (TSD)

When the die temperature increases, due to a high load condition and/or a high ambient temperature, the output switching is disabled until the temperature on the die has fallen sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 15°C hysteresis.

Minimum Off-Time Effect on Switching Frequency

$t_{OFF(MIN)}$ is 50 ns. This imposes constraints on the maximum $\frac{V_{OUT}}{V_{IN}}$ that the FAN5361 can provide, or the maximum output voltage it can provide at low V_{IN} while maintaining a fixed switching frequency in PWM mode.

When V_{IN} is LOW, fixed switching is maintained as long as $\frac{V_{OUT}}{V_{IN}} \leq 1 - t_{OFF(MIN)} \bullet f_{SW} \approx 0.7$.

The switching frequency drops when the regulator cannot provide sufficient duty cycle at 6MHz to maintain regulation. This occurs when V_{OUT} is greater than or equal to 1.82 V and V_{IN} is below 2.9 V at high load currents *(see Figure 15)*.

The calculation for switching frequency is given by:

$$f_{SW} = \min\left(\frac{1}{t_{SW(MAX)}}, 6MHz\right) \quad (3)$$

where:

$$t_{SW(MAX)} = 50ns \bullet \left(1 + \frac{V_{OUT} + I_{OUT} \bullet R_{OFF}}{V_{IN} - I_{OUT} \bullet R_{ON} - V_{OUT}}\right) \quad (4)$$

where:

$$R_{OFF} = R_{DSON\_N} + DCR_L$$

$$R_{ON} = R_{DSON\_P} + DCR_L$$

Applications Information

Selecting the Inductor

The output inductor must meet both the required inductance and the energy handling capability of the application. The inductor value affects average current limit, the PWM-to-PFM transition point, output voltage ripple, and efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \bullet \left(\frac{V_{IN} - V_{OUT}}{L \bullet f_{SW}} \right) \quad (5)$$

The maximum average load current, $I_{MAX(LOAD)}$, is related to the peak current limit, $I_{LIM(PK)}$ by the ripple current, given by:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2} \quad (6)$$

The transition between PFM and PWM operation is determined by the point at which the inductor valley current crosses zero. The regulator DC current when the inductor current crosses zero, I_{DCM}, is:

$$I_{DCM} = \frac{\Delta I}{2} \quad (7)$$

The FAN5361 is optimized for operation with L = 470 nH, but is stable with inductances up to 1.2 µH (nominal). Up to 2.2 µH(nominal) may be used; however, in that case, V_{IN} must be greater than or equal to 2.7 V. The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but since ΔI increases, the RMS current increases, as do the core and skin effect losses.

$$I_{RMS} = \sqrt{I_{OUT(DC)}^2 + \frac{\Delta I^2}{12}} \quad (8)$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs, as well as the inductor DCR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current and higher DCR.

Table 2 shows the effects of inductance higher or lower than the recommended 470 nH on regulator performance.

Output Capacitor

Table 3 suggests 0402 capacitors. 0603 capacitors may further improve performance in that the effective capacitance is higher. This improves transient response and output ripple.

Increasing C_{OUT} has no effect on loop stability and can therefore be increased to reduce output voltage ripple or to improve transient response. Output voltage ripple, ΔV_{OUT}, is:

$$\Delta V_{OUT} = \Delta I \bullet \left(\frac{1}{8 \bullet C_{OUT} \bullet f_{SW}} + ESR \right) \quad (9)$$

Input Capacitor

The 2.2 µF ceramic input capacitor should be placed as close as possible between the VIN pin and GND to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional "bulk" capacitance (electrolytic or tantalum) should be placed between C_{IN} and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

The effective capacitance value decreases as V_{IN} increases due to DC bias effects.

Table 2. Effects of Changes in Inductor Value (from 470 nH Recommended Value) on Regulator Performance

Inductor Value	$I_{MAX(LOAD)}$	ΔV_{OUT}	Transient Response
Increase	Increase	Decrease	Degraded
Decrease	Decrease	Increase	Improved

Table 3. Recommended Passive Components and their Variation Due to DC Bias

Component	Description	Vendor	Min.	Typ.	Max.[6]	Comment
L1	470 nH, 2012, 90 mΩ,1.1 A	Murata LQM21PNR47MC0 Murata LQM21PNR54MG0 Hitachi Metals HSLI-201210AG-R47	300 nH	470 nH	520 nH	Minimum value occurs at maximum current
C_{IN}	2.2 µF, 6.3 V, X5R, 0402	Murata or Equivalent GRM155R60J225ME15 GRM188R60J225KE19D	1.0 µF	2.2 µF	2.4 µF	Decrease primarily due to DC bias (V_{IN}) and elevated temperature
C_{OUT}	4.7 µF, X5R, 0402	Murata or Equivalent GRM155R60G475M GRM155R60E475ME760	1.6 µF	4.7 µF	5.2 µF	Decrease primarily due to DC bias (V_{OUT})

Note:
6. Higher inductance values are also acceptable. *See "Selecting the Inductor" instructions in Applications Information.*

PCB Layout Guidelines

There are only three external components: the inductor and the input and output capacitors. For any buck switcher IC, including the FAN5361, it is important to place a low-ESR input capacitor very close to the IC, as shown in Figure 41. The input capacitor ensures good input decoupling, which helps reduce noise appearing at the output terminals and ensures that the control sections of the IC do not behave erratically due to excessive noise. This reduces switching cycle jitter and ensures good overall performance. It is important to place the common GND of C_{IN} and C_{OUT} as close as possible to the FAN5361 C2 terminal. There is some flexibility in moving the inductor further away from the IC; in that case, V_{OUT} should be considered at the C_{OUT} terminal.

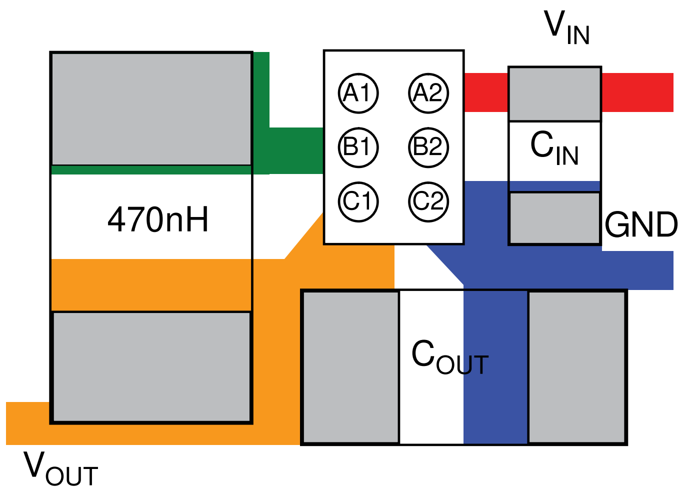


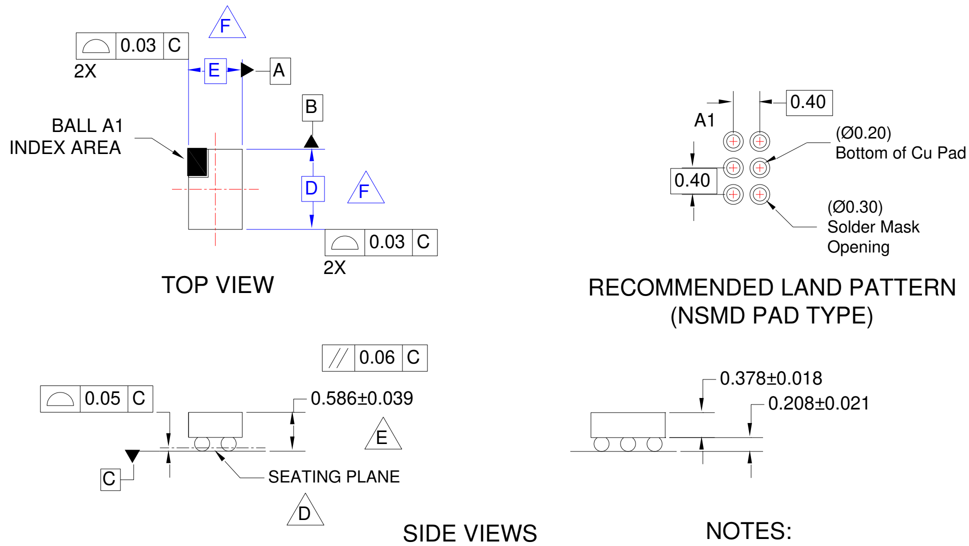
Figure 41. PCB Layout Guidance

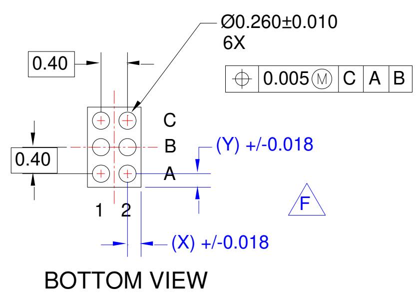
The table below pertains to the Marketing Outline Drawing on the following page.

Product-Specific Dimensions

Product	D	E	X	Y
FAN5361UCX	1.370 ±0.040	0.970 ±0.040	0.285	0.285

Physical Dimensions





NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASMEY14.5M, 2009.

D. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

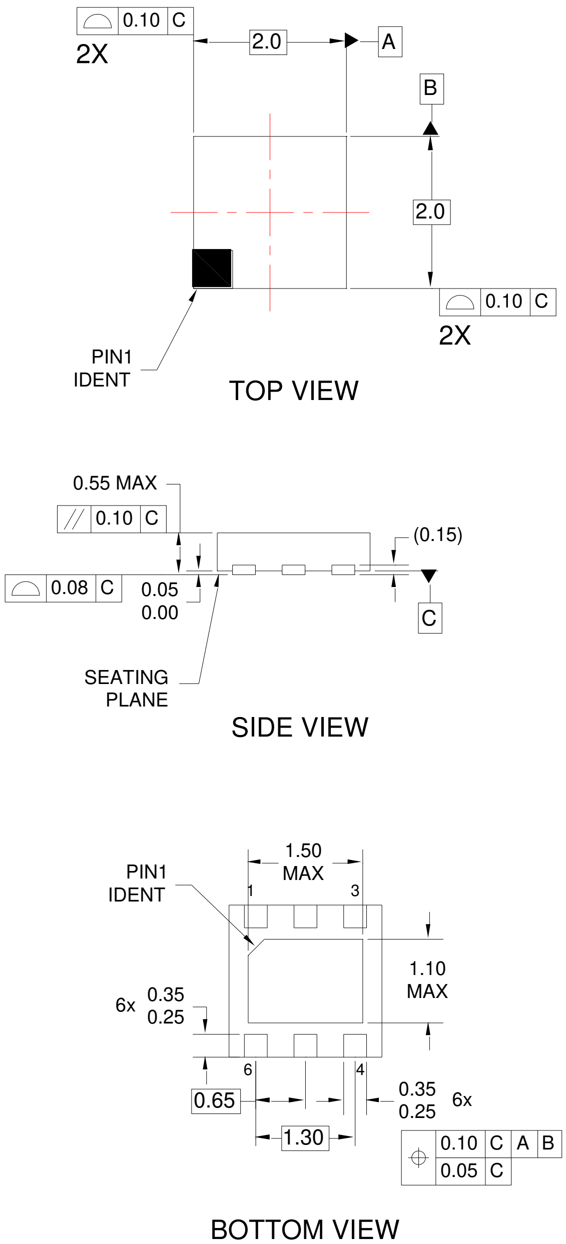
E. PACKAGE TYPICAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

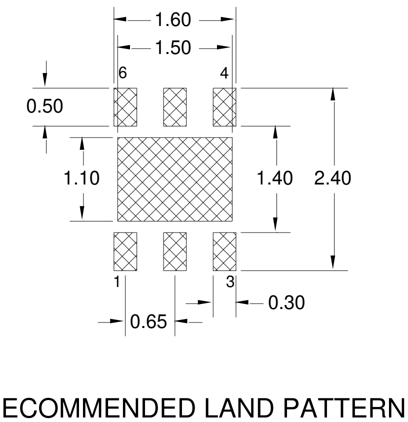
F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILENAME: UC006ACrev5.

Figure 42. 6-Bump WLCSP, 0.4mm Pitch

Physical Dimensions





NOTES:

A. OUTLINE BASED ON JEDEC REGISTRATION MO-229, VARIATION VCCC.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. DRAWING FILENAME: MKT-UMLP06Crev1

Figure 43. 6-Lead, 2 x 2 mm, Ultra-Thin Molded Leadless Package (UMLP)

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax : 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada.

Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative