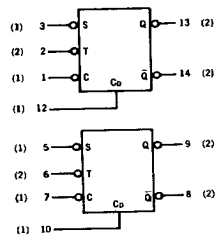
DUAL J-K FLIP-FLOPS

PLASTIC mW MRTL MC700P/800P series

MC776P • MC876P

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



f_{max} = 3 MHz min
P_D = 41 mW (Only Clock Input High)
29 mW (All Inputs Low)

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR

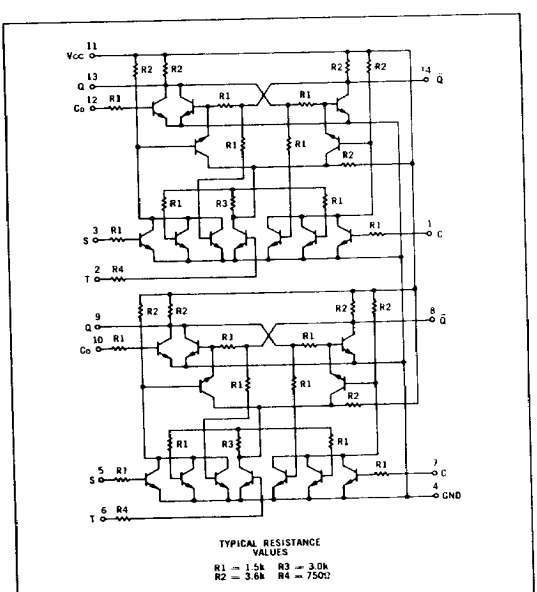
CLOCKED INPUT OPERATION③

t_n②		t_{n+1}	
S	C	Q	Q̄
1	1	Q_{n-1}	$\bar{Q}_{n-1}$
1	0	1	0
0	1	0	1
0	0	Q_n	$\bar{Q}_n$④

① Direct input (Co) must be low.

② The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+}.

④ Q_n is the state of the Q output in the time period t_n.



TYPICAL RESISTANCE VALUES

R1 = 1.5k R3 = 3.0k
R2 = 3.6k R4 = 750Ω

ELECTRICAL CHARACTERISTICS

Test procedures are shown for one flip-flop only.
The other flip-flop is tested in the same manner.

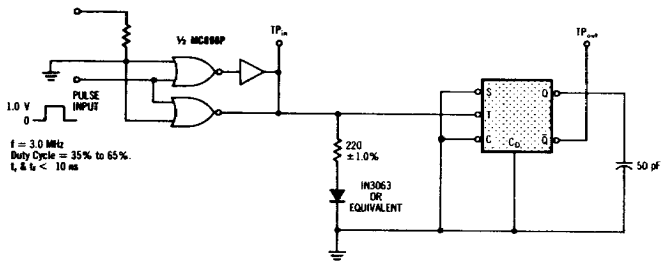
	@ Test Temperature	TEST VALUES (Volts) V_{in}	V_{en}	V_{out}	V_{off}	V_{cc}	μA I_D
MC876P	0°C	0.880	0.850	1.80	0.500	3.60	270
	+25°C	0.830	0.800	1.80	0.460	3.60	290
	+75°C	0.740	0.710	1.80	0.400	3.60	255
MC776P	+15°C	0.865	0.865	1.80	0.475	3.60	270
	+25°C	0.850	0.850	1.80	0.460	3.60	270
	+ 55°C	0.800	0.800	1.80	0.430	3.60	270

Characteristic	Symbol	Pin Under Test	MC876P Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	MC776P Test Limits +15°C Min	+15°C Max	+25°C Min	+25°C Max	+55°C Min	+55°C Max	Unit	TEST VALUES APPLIED TO PINS LISTED BELOW: V_{in}	V_{en}	V_{out}	V_{off}	V_{cc}	I_D	Gnd
Input Current	I_{in}	1	-	150	-	140	-	140	μAdc	-	150	-	150	-	150	μAdc	1	-	13	-	11	-	4
	$2\ I_{in}$	2	-	300	-	280	-	280		-	300	-	300	-	300		2	-	1, 3	-		-	
	I_{in}	3	-	150	-	140	-	140		-	150	-	150	-	150		3	-	14	-		-	
	I_{in}	12	-	150	-	140	-	140		-	150	-	150	-	150		12	-	14	-		-	
Output Current	I_{A2}	13	320	-	320	-	300	-	μAdc	320	-	320	-	320	-	μAdc	-	13	1	12	11	-	4, 14 §
		14		-		-		-			-		-		-		-	14	3, 12	-		-	
		14		-		-		-			-		-		-		-	12, 14	3	-		-	
Output Voltage	V_{out}	13	-	400	-	350	-	300	mVdc	-	400	-	300	-	320	mVdc	-	12	-	-		-	4, 14
		13	-		-		-			-		-		-			-	14	-	-		-	4, 13 §
		13*†	-		-		-			-		-		-			-	1, 3	-	-		14	4, 12
		13*#	-		-		-			-		-		-			-	1	-	3			
		13*#	-		-		-			-		-		-			-	-	-	1, 3			
		14	-		-		-			-		-		-			-	13	-	-		-	14 §
Saturation Voltage	$V_{CE(sat)}$	13	-	250	-	250	-	250	mVdc	-	220	-	230	-	320	mVdc	-	-	12	-	11	-	4, 14
		13	-		-		-			-		-		-			-	-	-	-		-	4, 13 §
		14	-		-		-			-		-		-			-	-	-	12		-	4, 14 §
Turn On Voltage	V_{on}	13*#	850	-	800	-	710	-	mVdc	865	-	850	-	800	-	mVdc	-	1, 3	-	-	11	13	4, 12
		13*†		-		-		-			-		-		-		-	3	-	1			
		13*†		-		-		-			-		-		-		-	-	-	1, 3			

* Clock Pulse to pin 2
† Pin 13 = LOW } Set by a momentary ground prior to the
# Pin 14 = LOW } application of the negative-going clock.

§ ground thru diode (cathode to ground).
Ground inputs of flip-flop not under test.
Other pins not listed are left open.

TOGGLE MODE TEST CIRCUIT



1. Set up the circuit with the Input Pulse as given.
2. The circuit should toggle with an output (TP_{out}) sense frequency of 1.5 MHz as the duty cycle is varied between 35% and 65%.

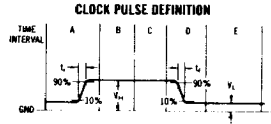
CLOCK PULSE

MC776P		
T_A	V_L	V_H
15°C	0.475 V	0.915 V
25°C	0.460 V	0.900 V
55°C	0.430 V	0.850 V

MC876P		
T_A	V_L	V_H
0°C	0.50 V	0.900 V
25°C	0.46 V	0.850 V
75°C	0.40 V	0.760 V

All values are ± 2.0mV

CLOCK PULSE DEFINITION



SEQUENCE OF EVENTS:

A. Voltage applied to Clock pin is raised to V_H. t_r is not critical, but should be < 1.0 μs.

B. Biases of all other inputs are applied. V_{CC} is applied without interruption throughout the testing.

C. Apply momentary ground (when applicable).

D. Clock pulse is allowed to fall to V_L. t_f must remain within 10 ns minimum and 200 ns maximum.

E. Electrical measurements are read out. Load current overshoot must be limited to 10% or the flip-flop may be tripped and the wrong output conditions occur.