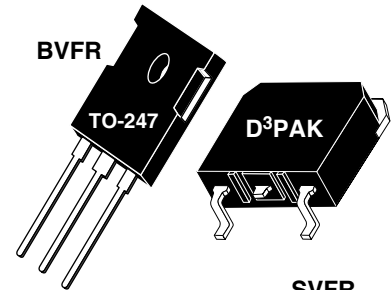
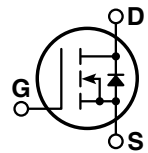




Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.



- **Faster Switching**
- **Lower Leakage**
- **TO-247 or Surface Mount D³PAK Package**
- **Avalanche Energy Rated**
- 




### MAXIMUM RATINGS

All Ratings:  $T_C = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	APT1201R6BVFR_SVFR	UNIT
$V_{DSS}$	Drain-Source Voltage	1200	Volts
$I_D$	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	8	Amps
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	32	
$V_{GS}$	Gate-Source Voltage Continuous	$\pm 30$	Volts
$V_{GSM}$	Gate-Source Voltage Transient	$\pm 40$	
$P_D$	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	280	Watts
	Linear Derating Factor	2.24	W/°C
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150	°C
$T_L$	Lead Temperature: 0.063" from Case for 10 Sec.	300	
$I_{AR}$	Avalanche Current <sup>①</sup> (Repetitive and Non-Repetitive)	8	Amps
$E_{AR}$	Repetitive Avalanche Energy <sup>①</sup>	30	mJ
$E_{AS}$	Single Pulse Avalanche Energy <sup>④</sup>	1210	

### STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-Source Breakdown Voltage ( $V_{GS} = 0V, I_D = 250\mu A$ )	1200			Volts
$I_{D(on)}$	On State Drain Current <sup>②</sup> ( $V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$ )	8			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance <sup>②</sup> ( $V_{GS} = 10V, I_D = 4A$ )			1.600	Ohms
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{DS} = 1200V, V_{GS} = 0V$ )			250	$\mu A$
	Zero Gate Voltage Drain Current ( $V_{DS} = 960V, V_{GS} = 0V, T_C = 125^\circ\text{C}$ )			1000	
$I_{GSS}$	Gate-Source Leakage Current ( $V_{GS} = \pm 30V, V_{DS} = 0V$ )			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage ( $V_{DS} = V_{GS}, I_D = 1.0mA$ )	2		4	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

**DYNAMIC CHARACTERISTICS**

APT1201R6BVFR\_SVFR

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> = 0V		3050	3660	pF
C <sub>OSS</sub>	Output Capacitance	V <sub>DS</sub> = 25V		255	360	
C <sub>RSS</sub>	Reverse Transfer Capacitance	f = 1 MHz		125	190	
Q <sub>g</sub>	Total Gate Charge <sup>③</sup>	V <sub>GS</sub> = 10V		155	230	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DD</sub> = 0.5 V <sub>DSS</sub>		15	23	
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	I <sub>D</sub> = I <sub>D</sub> [Cont.] @ 25°C		78	115	
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>GS</sub> = 15V		12	24	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 0.5 V <sub>DSS</sub>		10	20	
t <sub>d(off)</sub>	Turn-off Delay Time	I <sub>D</sub> = I <sub>D</sub> [Cont.] @ 25°C		50	75	
t <sub>f</sub>	Fall Time	R <sub>G</sub> = 1.6Ω		15	30	

**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS**

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I <sub>S</sub>	Continuous Source Current (Body Diode)			8	Amps
I <sub>SM</sub>	Pulsed Source Current <sup>①</sup> (Body Diode)			32	Amps
V <sub>SD</sub>	Diode Forward Voltage <sup>②</sup> (V <sub>GS</sub> = 0V, I <sub>S</sub> = -I <sub>D</sub> [Cont.])			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt <sup>⑤</sup>			18	V/ns
t <sub>rr</sub>	Reverse Recovery Time (I <sub>S</sub> = -I <sub>D</sub> [Cont.], di/dt = 100A/μs)	T <sub>j</sub> = 25°C		220	ns
		T <sub>j</sub> = 125°C		450	
Q <sub>rr</sub>	Reverse Recovery Charge (I <sub>S</sub> = -I <sub>D</sub> [Cont.], di/dt = 100A/μs)	T <sub>j</sub> = 25°C		1.0	μC
		T <sub>j</sub> = 125°C		3.0	
I <sub>RRM</sub>	Peak Recovery Current (I <sub>S</sub> = -I <sub>D</sub> [Cont.], di/dt = 100A/μs)	T <sub>j</sub> = 25°C		10	Amps
		T <sub>j</sub> = 125°C		14	

**THERMAL CHARACTERISTICS**

Symbol	Characteristic	MIN	TYP	MAX	UNIT
R <sub>θJC</sub>	Junction to Case			0.45	°C/W
R <sub>θJA</sub>	Junction to Ambient			40	

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Pulse Test: Pulse width < 380 μs, Duty Cycle < 2%

- ③ See MIL-STD-750 Method 3471
- ④ Starting T<sub>j</sub> = +25°C, L = 37.81mH, R<sub>G</sub> = 25Ω, Peak I<sub>L</sub> = 8A
- ⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. I<sub>S</sub> ≤ I<sub>D</sub>-8A di/dt ≤ 700A/μs v<sub>R</sub> ≤ 1200V T<sub>j</sub> ≤ 150°C

APT Reserves the right to change, without notice, the specifications and information contained herein.

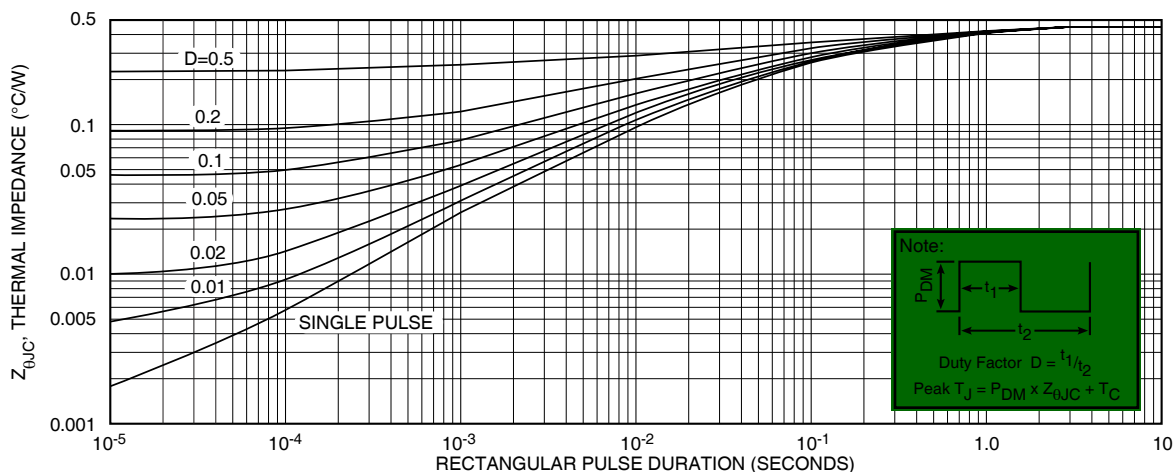


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

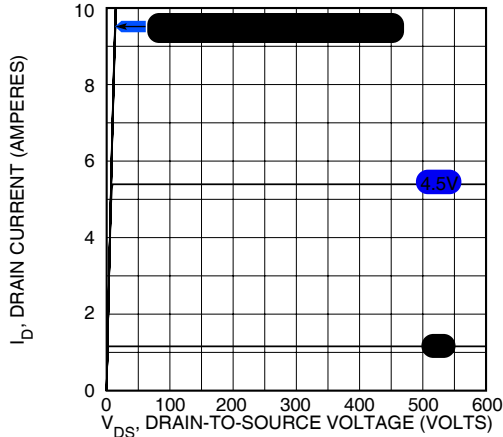


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

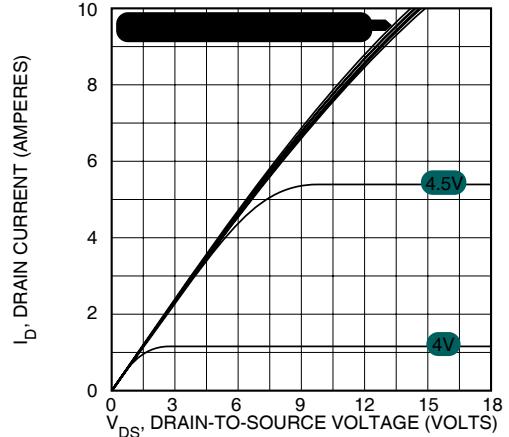


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

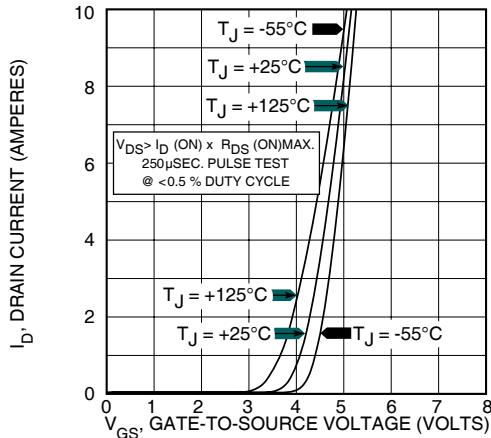


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

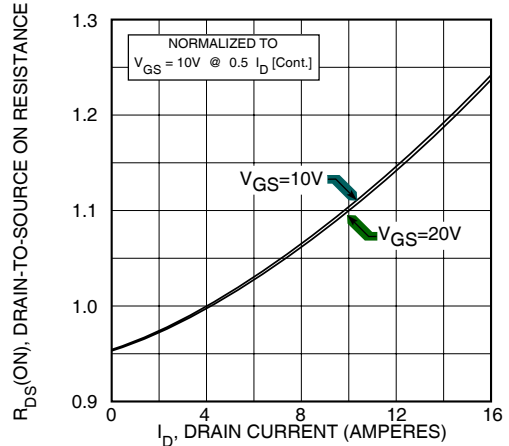


FIGURE 5,  $R_{DS(ON)}$  vs DRAIN CURRENT

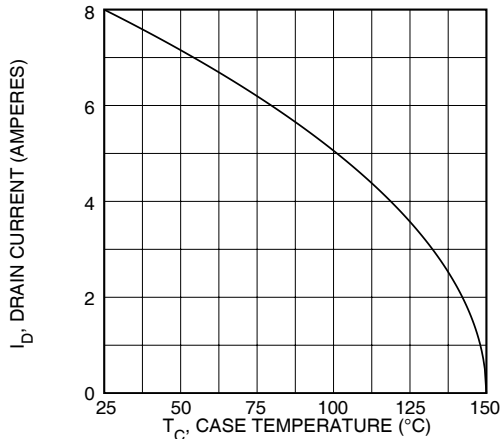


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

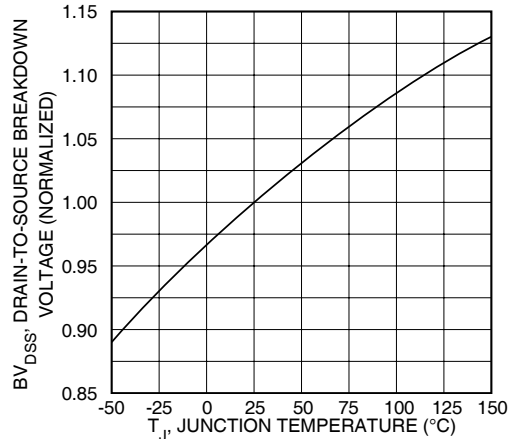


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

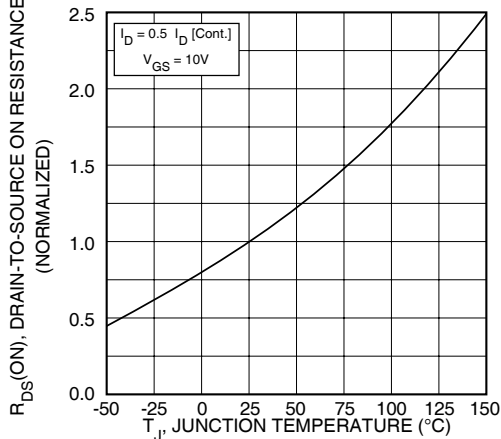


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

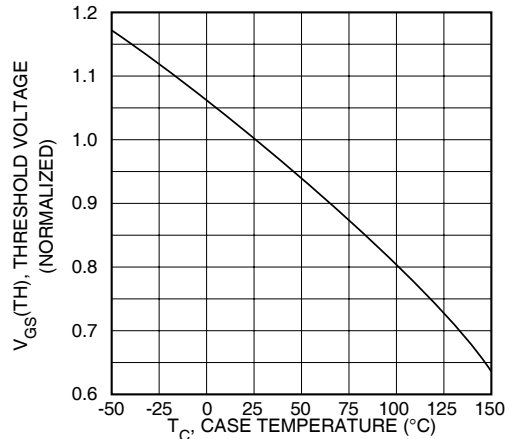


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

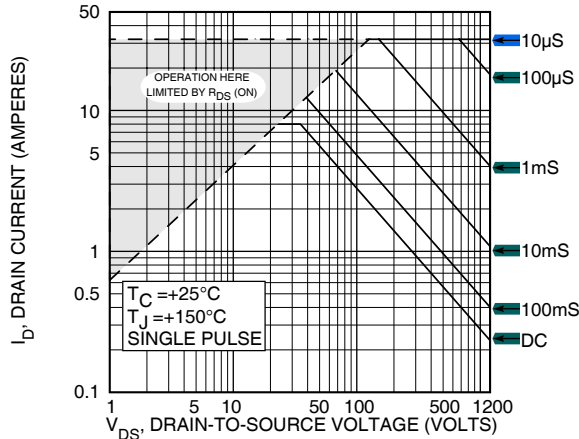


FIGURE 10, MAXIMUM SAFE OPERATING AREA

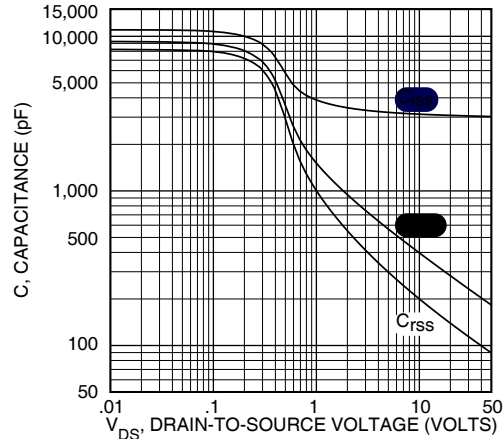


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

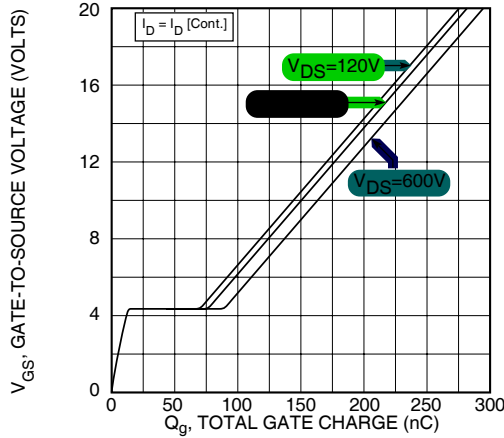


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

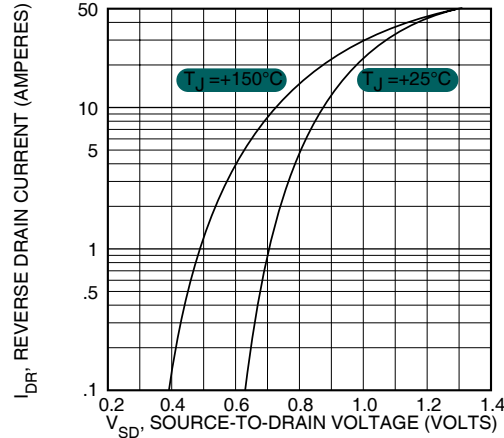
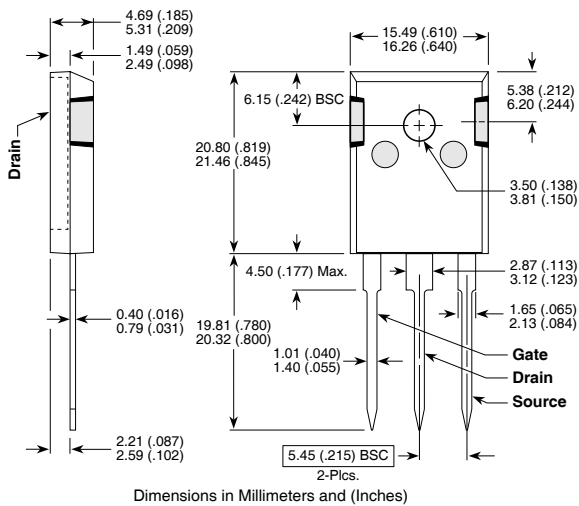
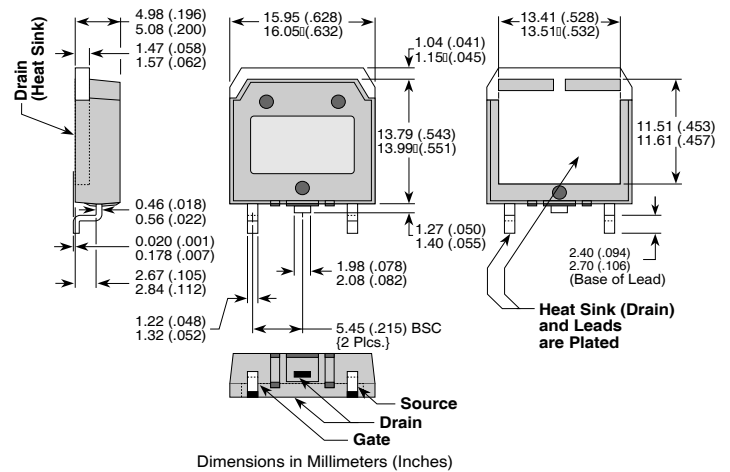


FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

TO-247 Package Outline (BVFR)



D<sup>3</sup>PAK Package Outline (SVFR)



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