

Features

- 32.768 kHz ± 3 and ± 5 ppm all-inclusive frequency stability
- World's smallest TCXO Footprint: 1.2 mm²
 - 1.5 x 0.8 mm CSP
 - No external bypass cap required
- Improved stability reduces system power with fewer network timekeeping updates
- Low integrated phase jitter (IPJ) suitable for multiplying up for portable audio: 2.5 nSRMS
- Ultra-low power: 4.5 μ A
- Operating supply voltage range: 1.62 V to 3.63 V
- Operating temperature ranges: -20°C to +70°C, -40°C to +85°C
- Pb-free, RoHS and REACH compliant

Applications

- Smart watches, health and wellness monitors
- Ultra-accurate RTC reference clock
- Smart utility meters, E-meters
- Internet-of-Things (IoT) with BLE



Electrical Specifications

Conditions: Min/Max limits are over temperature, Vdd = 1.8V $\pm 10\%$, unless otherwise stated. Typicals are at 25°C and Vdd = 1.8V.

Table 1. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency and Stability						
Output Frequency	F _{out}	32.768			kHz	
Total Frequency Stability ^[1]	F _{stab}	-3		3	ppm	All inclusive, 1.62V to 3.63V
		-5		5		
Allan Deviation	AD		1e-8	4e-8		1 second averaging time
First Year Frequency Aging	F _{aging}		± 1		ppm	T _A = 25°C, Vdd = 1.8V
Jitter and Frequency Response Performance						
Integrated Phase Jitter	IPJ		1.8	2.5	nSRMS	Integration bandwidth = 100 Hz to 16.384 kHz. Inclusive of 50 mV peak-to-peak sinusoidal noise on Vdd. Noise frequency 100 Hz to 20 MHz.
RMS Period Jitter	PJ _{RMS}		2.5	4	nSRMS	10,000 samples, per JEDEC standard 65B
Peak-to-Peak Period Jitter	PJ _{p-p}		20	35	ns _{p-p}	
Dynamic Temperature Frequency Response		-0.5		+0.5	ppm/sec	Under temp ramp up to 1.5°C/sec
Supply Voltage and Current Consumption						
Operating Supply Voltage	Vdd	1.62	1.8	1.98	V	
		1.62		3.63		
Supply Current	I _{dd}		4.5	5.3	μ A	No load
Start-up Time at Power-up	t _{start}			300	ms	Measured when supply reaches 90% of final Vdd to the first output pulse.
Operating Temperature Range						
Operating Temperature Range	Op_Temp	-20		70	°C	"C" ordering code
		-40		85	°C	"I" ordering code
LVC MOS Output						
Output Rise/Fall Time	tr, tf		9	20	ns	10 – 90% Vdd, 15pF load
Output Clock Duty Cycle	DC	45		55	%	
Output Voltage High	VOH	90%			Vdd	I _{OH} = -50 μ A, 15 pF load
Output Voltage Low	VOL			10%	Vdd	I _{OL} = 50 μ A, 15 pF load

Note:

- Relative to 32.768 kHz, includes initial tolerance, over temp stability, Vdd, 20% load variation, hysteresis, board-level underfill (5 ppm only), 2x reflow. Tested with Agilent 53132A frequency counter. Measured with 100 ms gate time for accurate frequency measurement.

Table 2. Pin Configuration

Pin	Symbol	I/O	Functionality
1	NC	Internal Test	Leave Floating. Do not connect to GND.
2	CLK Out	OUT	Oscillator clock output. LVCMOS compatible logic.
3	Vdd	Power Supply	1.8V \pm 10% power supply. Under normal operating conditions, Vdd does not require external bypass/decoupling capacitor(s). SiT1566 includes on-chip filtering capacitors. Under extreme noise on the supply, a 10-100 nF low ESR ceramic bypass capacitor may be recommended close to the Vdd pin.
4	GND	Power Supply Ground	Connect to ground.

CSP Package (Top View)

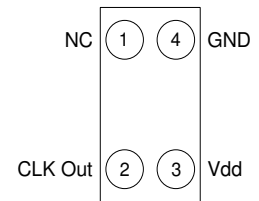


Figure 1. Pin Assignment

Table 3. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameters	Test Conditions	Value	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 4.0	V
Continuous Maximum Operating Temperature Range		105	$^{\circ}$ C
Short Duration Maximum Operating Temperature Range	\leq 30 minutes	125	$^{\circ}$ C
Human Body Model (HBM) ESD Protection	JESD22-A114	2000	V
Charge-Device Model (CDM) ESD Protection	JESD22-C101	750	V
Machine Model (MM) ESD Protection	T _A = 25 $^{\circ}$ C	200	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	Mil 883, Method 2002	20,000	g
Mechanical Vibration Resistance	Mil 883, Method 2007	70	g
1508 CSP Junction Temperature		150	$^{\circ}$ C
Storage Temperature		-65 to 150	$^{\circ}$ C

System Block Diagram

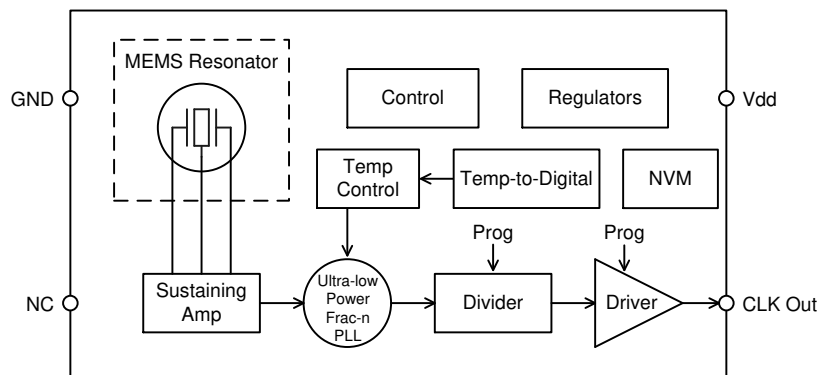


Figure 2. SiT1566 Block Diagram

Description

SiT1566 is an ultra-small, micro-power 32.768 kHz TCXO optimized for battery-powered applications. SiTime's silicon MEMS technology enables the first 32 kHz TCXO in the world's smallest footprint and chip-scale packaging (CSP). Typical supply current is 4.5 μ A under no load condition.

SiTime's MEMS oscillator consists of a MEMS resonator and a programmable analog circuit. SiT1566 MEMS resonator is built with SiTime's unique MEMS First™ process. A key manufacturing step is EpiSeal™ during which the MEMS resonator is annealed with temperatures over 1000°C. EpiSeal creates an extremely strong, clean, vacuum chamber that encapsulates the MEMS resonator and ensures the best performance and reliability. During EpiSeal, a poly silicon cap is grown on top of the resonator cavity, which eliminates the need for additional cap wafers or other exotic packaging. As a result, SiTime's MEMS resonator die can be used like any other semiconductor die. One unique result of SiTime's MEMS First and EpiSeal manufacturing processes is the capability to integrate SiTime's MEMS die with a SOC, ASIC, microprocessor or analog die within a package to eliminate external timing components and provide a highly integrated, smaller, cheaper solution to the customer.

TCXO Frequency Stability

SiT1566 is factory calibrated (trimmed) over multiple temperature points to guarantee extremely tight stability over temperature. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover point with a 0.04 ppm/C² temperature coefficient, the SiT1566 temperature coefficient is calibrated and corrected over temperature with an active temperature correction circuit. The result is a 32 kHz TCXO with extremely tight frequency variation over the -40°C to +85°C temperature range.

When measuring the output frequency of SiT1566 with a frequency counter, it is important to make sure the counter's gate time is >100 ms. Shorter gate times may lead to inaccurate measurements.

Dynamic Temperature Frequency Response

Dynamic Temperature Frequency Response is the rate of frequency change during temperature ramps. This is an important performance metric when the oscillator is mounted near a high power component (e.g. SoC or power management) that may rapidly change the temperature of surrounding components.

For moderate temperature ramp rates (<2°C/sec), the dynamic response is primarily determined by the steady-state frequency vs. temperature of the device. The best dynamic response is obtained from parts which have been trimmed to be flat in frequency over temperature.

For high temperature ramp rates (>5°C/sec), the latency in the temperature compensation loop contributes a larger frequency error, which is dependent on the temperature compensation update rate. This part achieves excellent performance at the default 3 Hz refresh update rate. This device family supports faster update rates for further reducing dynamic frequency error at the expense of slightly increased current consumption. Other compensation refresh rate options include 6 Hz, 12 Hz, and 24 Hz. [Contact SiTime](#) for other options.

Typical Operating Curves

($T_A = 25^\circ\text{C}$, $V_{DD} = 1.8\text{V}$, unless otherwise stated)

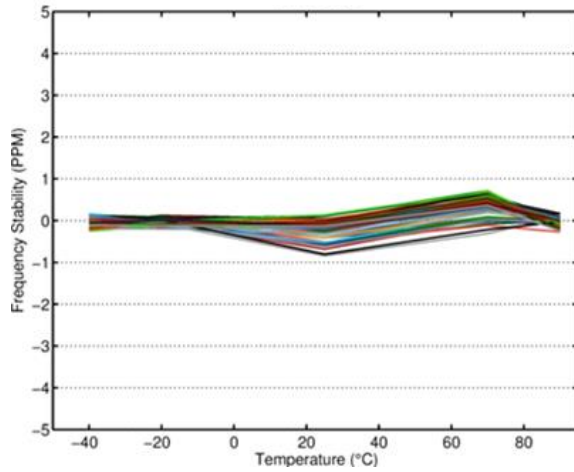


Figure 3. Frequency Stability over Temperature

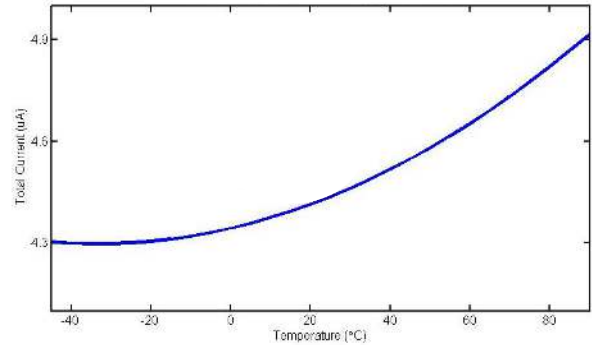


Figure 4. Supply Current over Temperature (No Load)

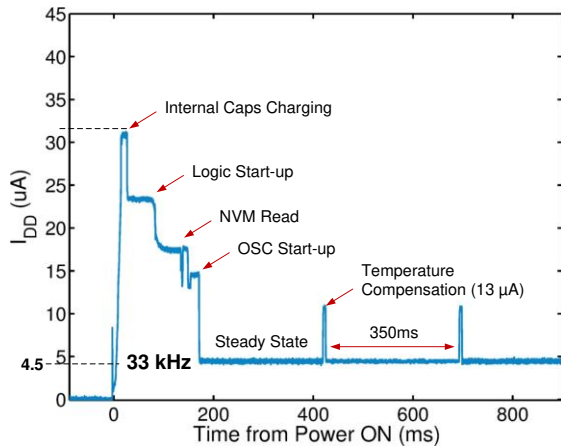


Figure 5. Start-up and Steady-State Current Profile

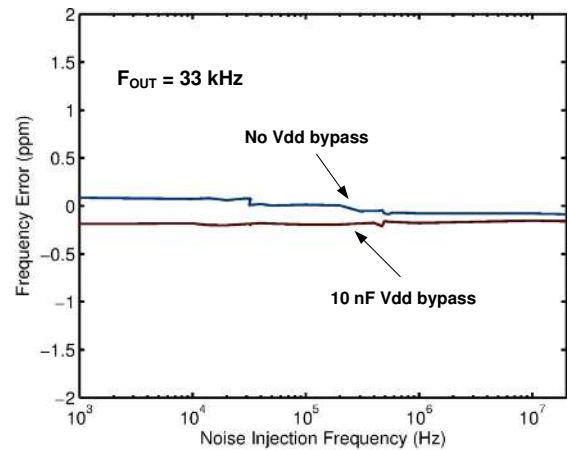
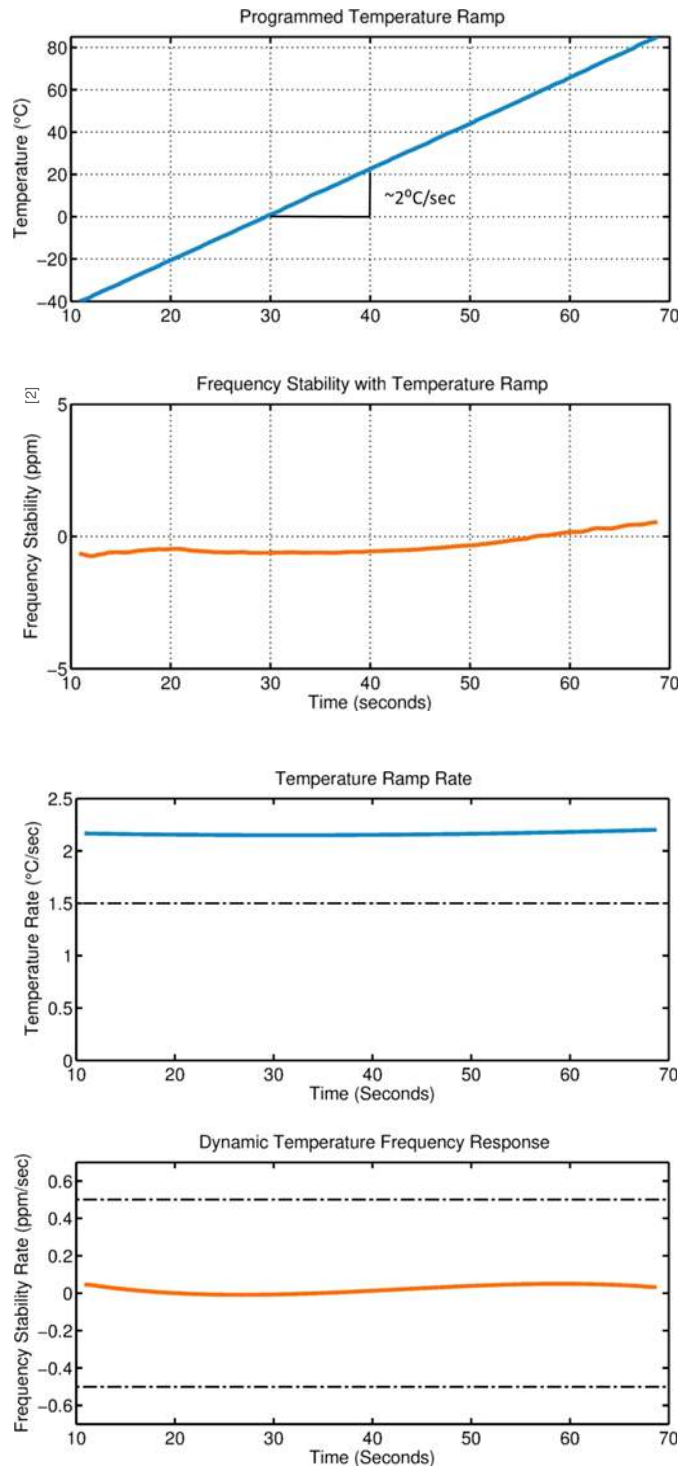


Figure 6. Power Supply Noise Rejection (PSNR)



Figure 7. LVC MOS Output Sing

Dynamic Frequency Response for Moderate Temperature Ramps

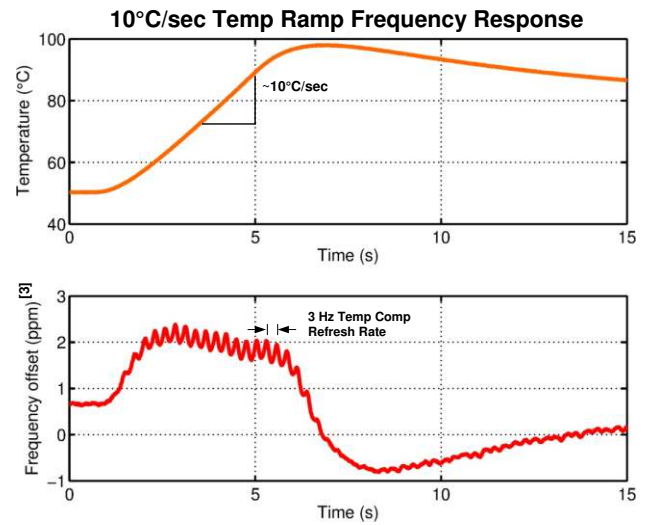
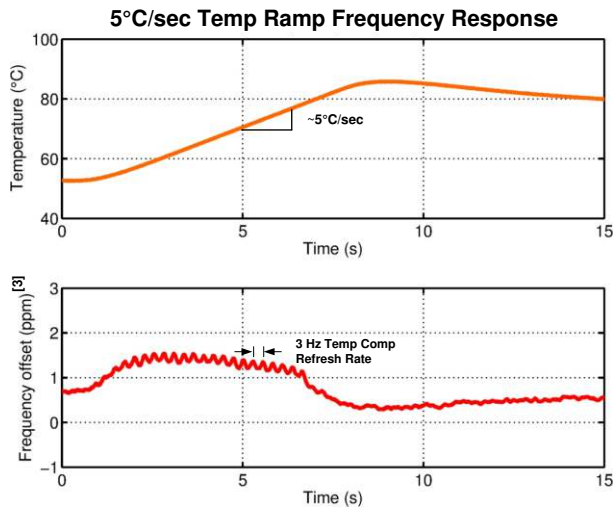


Note:

2. Measured relative to 32.768 kHz.

Frequency accuracy under a moderate temperature ramp up to 2°C/sec is limited by the TCXO's trimmed accuracy of the frequency stability over-temperature.

Dynamic Frequency Response for Fast Temperature Ramps



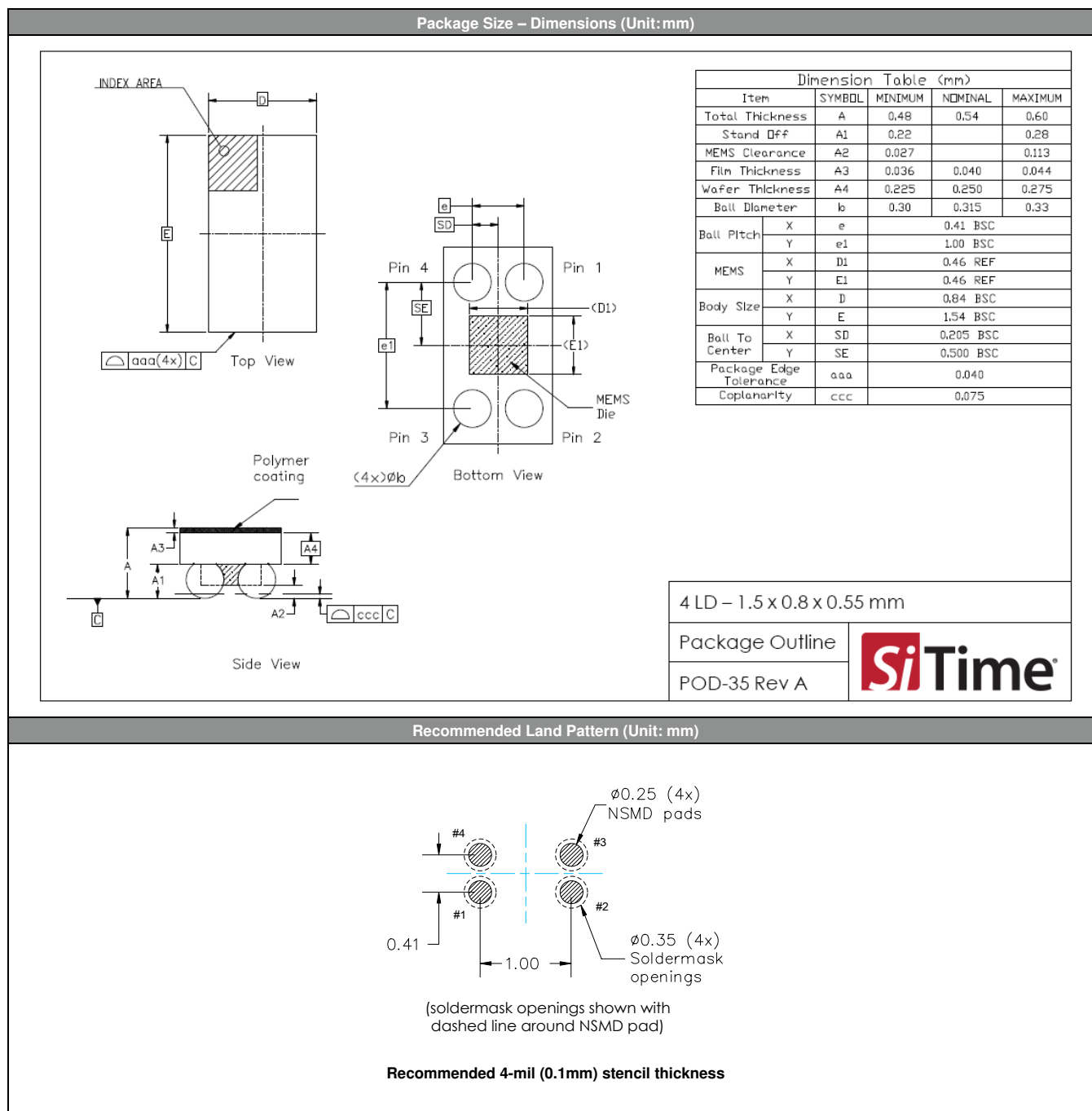
Note:

3. Measured relative to 32.768 kHz.

For temperature ramps >5°C/sec, the frequency accuracy is limited by the update rate of the temperature compensation path (see the 5°C/sec and 10°C/sec plots above).

Contact [SiTime](http://www.sitime.com) for applications that require improved dynamic performance.

Dimensions and Patterns



Manufacturing Guidelines

1. No Ultrasonic or Megasonic cleaning: Do not subject SiT1566 to an ultrasonic or megasonic cleaning environment. Permanent damage or long term reliability issues may occur.
2. Applying board-level underfill and overmold is acceptable and will not impact the reliability of the device.
3. Reflow profile, per JESD22-A113D.
4. The SiT1566 CSP includes a protective, opaque polymer top-coat. If the SiT1566 will see intense light, especially in the 1.0-1.2 μ m IR spectrum, we recommend a protective “glob-top” epoxy or other cover to keep the light from negatively impacting the frequency stability.
5. For additional manufacturing guidelines and marking/tape-reel instructions, refer to [SiTime Manufacturing Notes](#).

Ordering Information

SiT1566A-I-JE-18E-32.768S

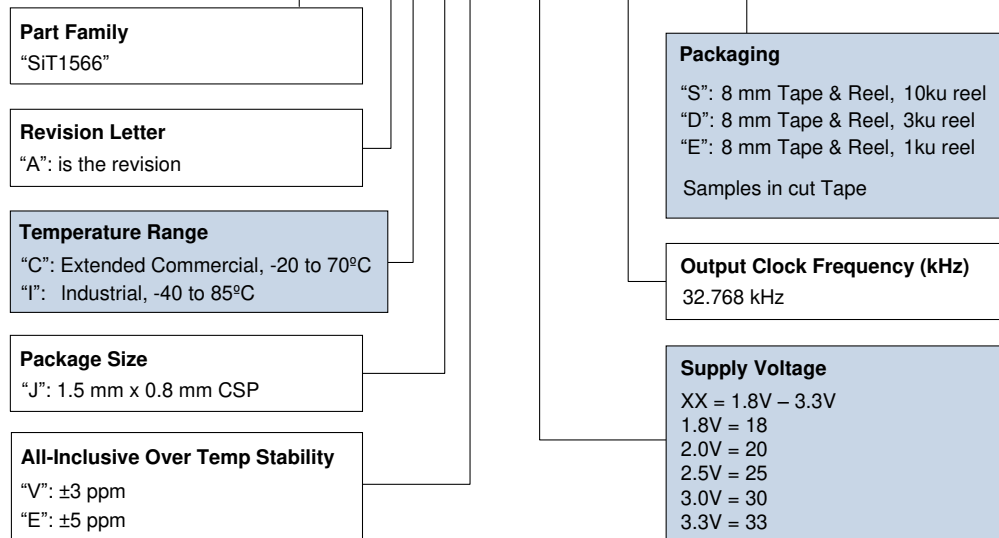


Table 4. Revision History

Version	Release Date	Change Summary
0.1	06/30/2015	Advanced datasheet initial release
0.7	03/11/2016	Preliminary datasheet initial release
1.0	03/15/2018	Production Datasheet Release, added ± 3 ppm option Updated logo and company address, other page layout changes
1.01	01/16/2019	Updated the frequency stability specification in Table 1, Electrical Characteristics, to be valid for 1.62V to 3.63V.

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439

© SiTime Corporation 2015-2019. The information contained herein is subject to change at any time without notice. SiTime assumes no responsibility or liability for any loss, damage or defect of a Product which is caused in whole or in part by (i) use of any circuitry other than circuitry embodied in a SiTime product, (ii) misuse or abuse including static discharge, neglect or accident, (iii) unauthorized modification or repairs which have been soldered or altered during assembly and are not capable of being tested by SiTime under its normal test conditions, or (iv) improper installation, storage, handling, warehousing or transportation, or (v) being subjected to unusual physical, thermal, or electrical stress.

Disclaimer: SiTime makes no warranty of any kind, express or implied, with regard to this material, and specifically disclaims any and all express or implied warranties, either in fact or by operation of law, statutory or otherwise, including the implied warranties of merchantability and fitness for use or a particular purpose, and any implied warranty arising from course of dealing or usage of trade, as well as any common-law duties relating to accuracy or lack of negligence, with respect to this material, any SiTime product and any product documentation. Products sold by SiTime are not suitable or intended to be used in a life support application or component, to operate nuclear facilities, or in other mission critical applications where human life may be involved or at stake. All sales are made conditioned upon compliance with the critical uses policy set forth below.

CRITICAL USE EXCLUSION POLICY

BUYER AGREES NOT TO USE SITIME'S PRODUCTS FOR ANY APPLICATION OR IN ANY COMPONENTS USED IN LIFE SUPPORT DEVICES OR TO OPERATE NUCLEAR FACILITIES OR FOR USE IN OTHER MISSION-CRITICAL APPLICATIONS OR COMPONENTS WHERE HUMAN LIFE OR PROPERTY MAY BE AT STAKE.

SiTime owns all rights, title and interest to the intellectual property related to SiTime's products, including any software, firmware, copyright, patent, or trademark. The sale of SiTime products does not convey or imply any license under patent or other rights. SiTime retains the copyright and trademark rights in all documents, catalogs and plans supplied pursuant to or ancillary to the sale of products or services by SiTime. Unless otherwise agreed to in writing by SiTime, any reproduction, modification, translation, compilation, or representation of this material shall be strictly prohibited.