Integrated Device Technology, Inc.

128K x 32, 256K x 32 3.3V CMOS STATIC RAM MODULES

PRELIMINARY
IDT7MPV4060
IDT7MPV4145

FEATURES:

- High density 4 megabit and 8 megabit static RAM modules
- Low profile 72-lead, gold plated SIMM (Single In-line Memory Modules)
- Fast access time: 12ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 3.3V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

PIN CONFIGURATION

		1	NC
NC	2	3	PD_2
PD_3	4	5	GND
PD_0	6	7	PD_1
I/O_0	8	9	I/O_8
I/O_1	10	11	I/O_9
I/O_2	12	13	I/O_{10}
I/O_3	14	15	I/O_{11}
V_{CC}	16	17	A_0
A_7	18	19	A_1
A_8	20	21	A_2
A_9	22	23	I/O_{12}
I/O_4	24	25	I/O_{13}
I/O_5	26	27	I/O_{14}
I/O_6	28	29	I/O_{15}
I/O_7	30	31	GND
$\overline{WE}$	32	33	A_{15}
A_{14}	34	35	$\overline{CS_2}$
$\overline{CS_1}$	36		
		37	$\overline{CS_4}$
$\overline{CS_3}$	38	39	A_{17} (1)
A_{16}	40	41	$\overline{OE}$
GND	42	43	I/O_{24}
I/O_{16}	44	45	I/O_{25}
I/O_{17}	46	47	I/O_{26}
I/O_{18}	48	49	I/O_{27}
I/O_{19}	50	51	A_3
A_{10}	52	53	A_4
A_{11}	54	55	A_5
A_{12}	56	57	V_{CC}
A_{13}	58	59	A_6
I/O_{20}	60	61	I/O_{28}
I/O_{21}	62	63	I/O_{29}
I/O_{22}	64	65	I/O_{30}
I/O_{23}	66	67	I/O_{31}
GND	68	69	NC
NC	70	71	NC
NC	72		

TOP VIEW

4054 drw 01

NOTE:
1. A_{17} is a no connect for the 7MPV4060.

DESCRIPTION:

The IDT7MPV4060 is a 128K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using four 128K x 8 static RAMs in plastic SOJ packages.

The IDT7MPV4145 is a 256K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 256K x 4 static RAMs in plastic SOJ packages.

The IDT7MPV4060/7MPV4145 are available with access times as fast as 12ns with minimal power consumption.

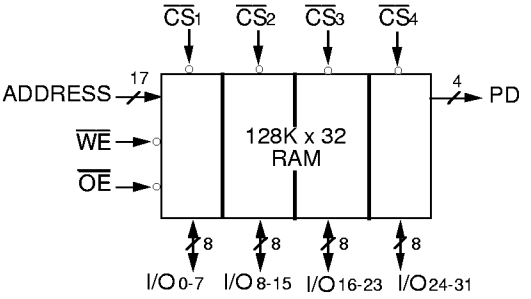
The IDT7MPV4060/7MPV4145 are packaged in a 72-lead SIMM. The SIMM configuration allows use of edge mounted sockets to secure the module and with variable angled sockets, ideal for low profile requirements.

All inputs and outputs of the IDT7MPV4060/7MPV4145 are TTL compatible and operate from a single 3.3V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

The contact pins are plated with 100 micro-inches of nickel covered by 30 micro-inches minimum of selective gold.

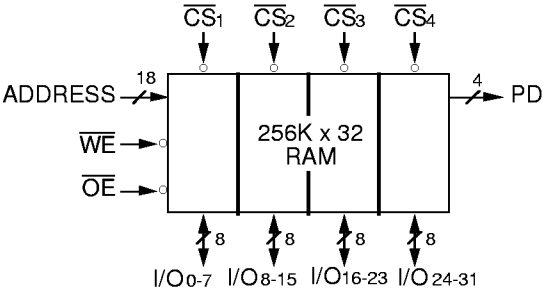
FUNCTIONAL BLOCK DIAGRAM

7MPV4060



4054 drw 02

7MPV4145



4054 drw 03

PIN NAMES

I/O_{0-31}	Data Inputs/Outputs
A_{0-17}	Addresses
$\overline{CS}_{1-4}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground
NC	No Connect
PD_{0-3}	Presence Detect

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

4054 tbl 01

Symbol	Parameter[1]	Conditions	4060	4145	Unit
$C_{I/O}$	I/O Capacitance	$V_{(OUT)}$ = 3dV	10	10	pF
$C_{IN(CS)}$	Input Capacitance ($\overline{CS}_{1-4}$)	$V_{(IN)}$ = 3dV	12	20	pF
$C_{IN(A)}$	Input Capacitance (Address, $\overline{WE}$, $\overline{OE}$)	$V_{(IN)}$ = 3dV	40	72	pF

NOTE: 4054 tbl 02

1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3[1]	—	0.8	V

NOTE: 4054 tbl 03

1. V_{IL} (min) = –1.0V for pulse width less than 5ns, once per cycle..

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 10%

4054 tbl 04

PRESENT DETECT TABLE

Module	PD_0	PD_1	PD_2	PD_3
7MPV4060	Open	Open	Open	GND
7MPV4145	GND	GND	Open	Open

4054 tbl 05

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Output Disable	L	H	H	High-Z	Active

4054 tbl 06

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.1	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTES: 4054 tbl 07

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC}+0.5V.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	'4060	'4145	Unit
$\|I_{LI}\|$	Input Leakage Data	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	5	5	µA
$\|I_{LI}\|$	Input Leakage $\overline{CS}$	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	5	10	µA
$\|I_{LI}\|$	Input Leakage (Address, $\overline{WE}$, and $\overline{OE}$)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	20	40	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	5	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	—	V

4054 tbl 08

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	'4060	'4145	Unit
I_{CC}	Dymanic Operating Current	f = f_{MAX}; $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	600	1200	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}	160	320	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; f = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V	40	80	mA

4054 tbl 09

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

4054 tbl 10

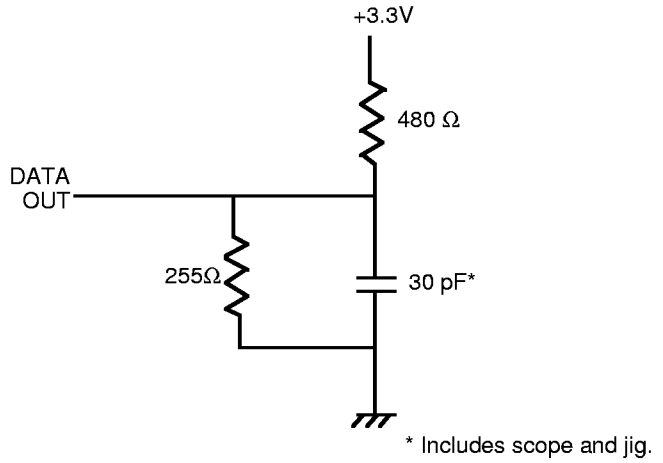


Figure 1. Output Load

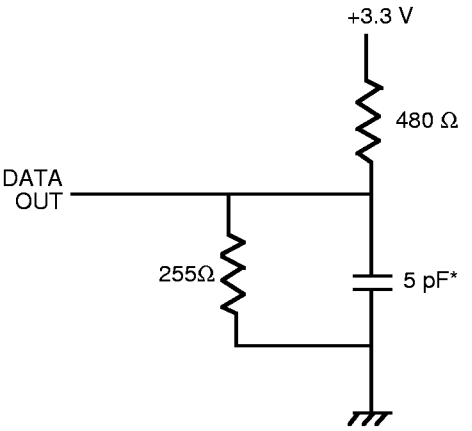


Figure 2. Output Load
(for tOLZ, tOHZ, tCHZ, tCLZ, tWHZ, tOW)

4054 drw 04

AC ELECTRICAL CHARACTERISTICS

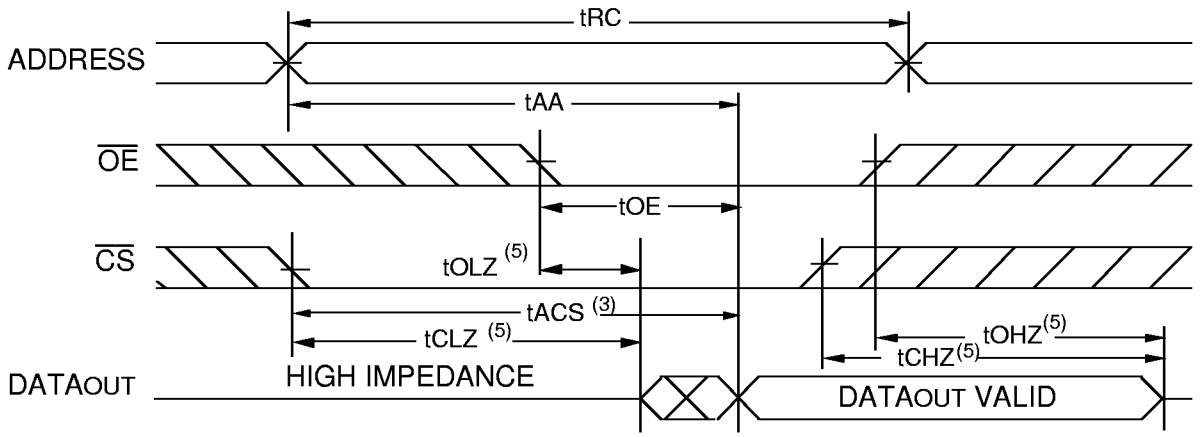
(V_{CC} = 3.3V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	-12		-15		-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	ns
t_{ACS}	Chip Select Access Time	—	12	—	15	—	20	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	3	—	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	8	—	10	—	12	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	8	—	12	—	15	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	8	—	12	—	15	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	4	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	—	0	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	12	—	15	—	20	ns
Write Cycle								
t_{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t_{CW}	Chip Select to End of Write	10	—	12	—	15	—	ns
t_{AW}	Address Valid to End of Write	10	—	12	—	15	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	—	0	ns
t_{WP}	Write Pulse Width	10	—	12	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	—	0	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	8	—	13	—	16	ns
t_{DW}	Data to Write Time Overlap	10	—	12	—	15	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}(1)	Output Active from End of Write	3	—	3	—	3	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

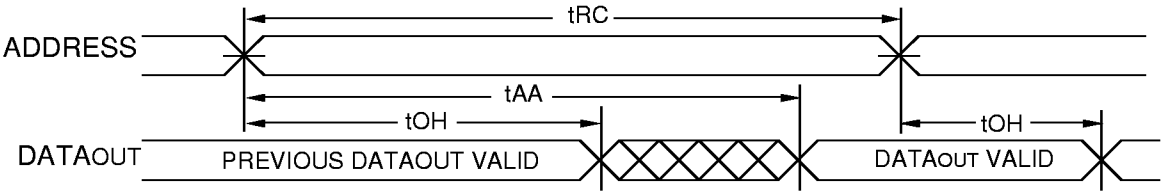
4054 tbl 11

TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



4054 drw 05

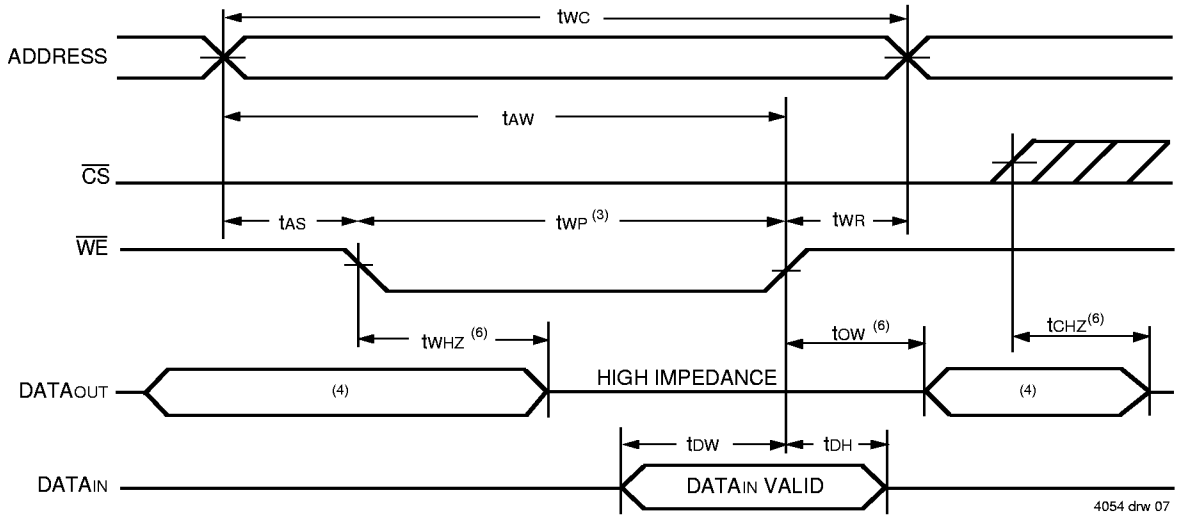
TIMING WAFEFORM OF READ CYCLE NO. 2(1, 2, 4)



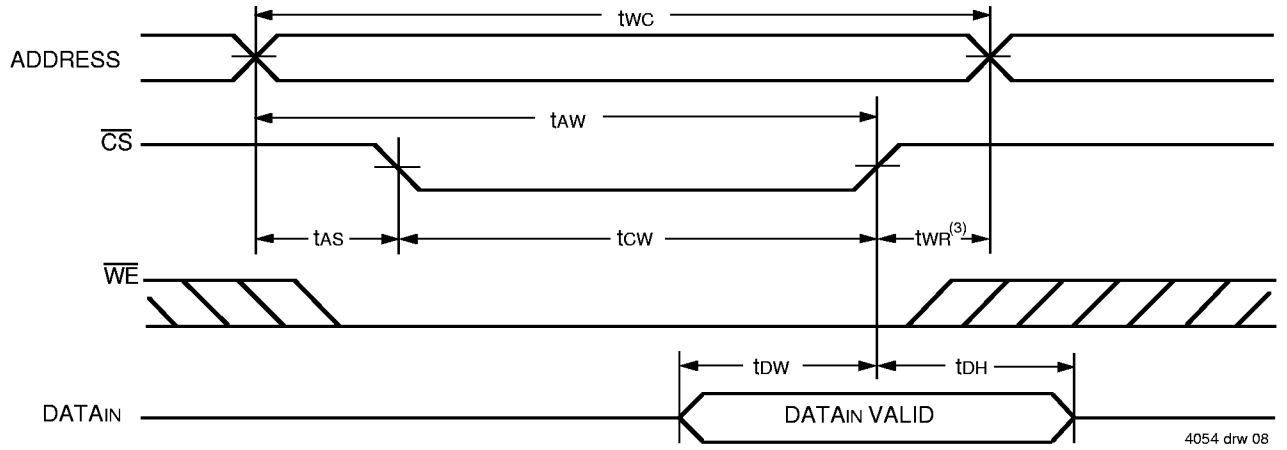
4054 drw 06

NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 5)

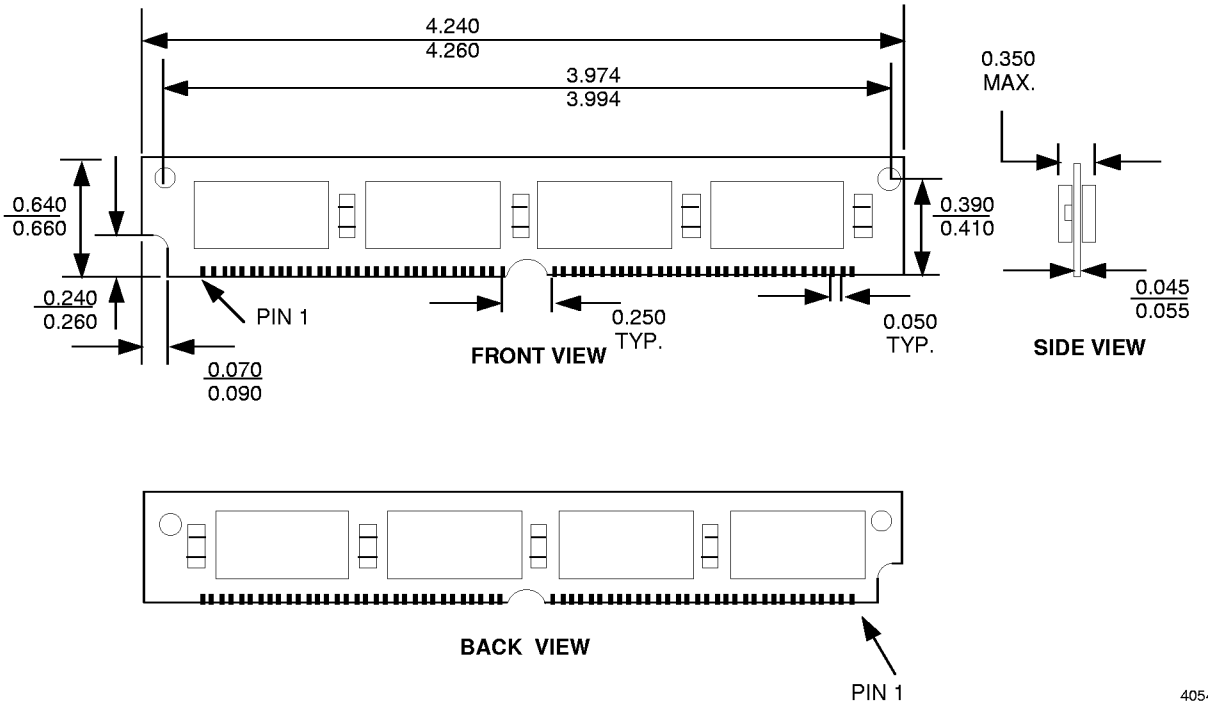


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 5)



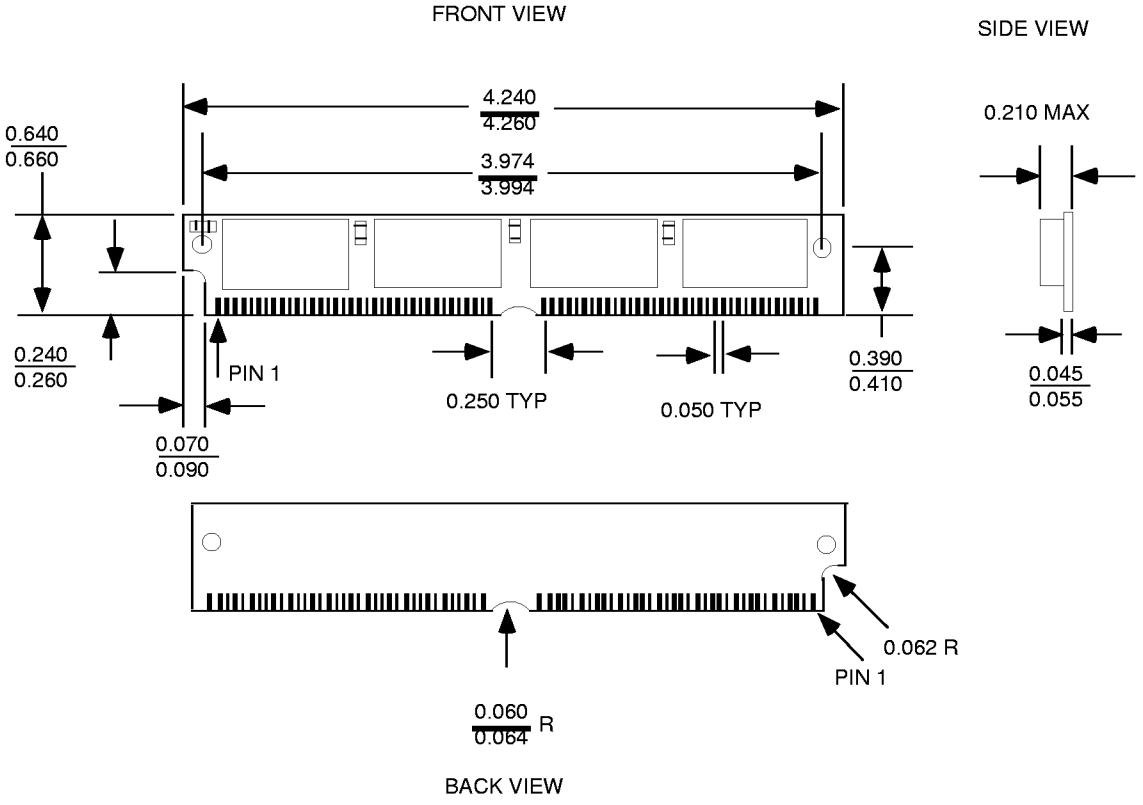
NOTES:
1. $\overline{WE}$ must be HIGH, $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state. $\overline{CS}$ must be active during the t_{CW} write period.
6. Transition is measured ±200mV from steady state.

PACKAGE DIMENSIONS – IDT7MPV4145



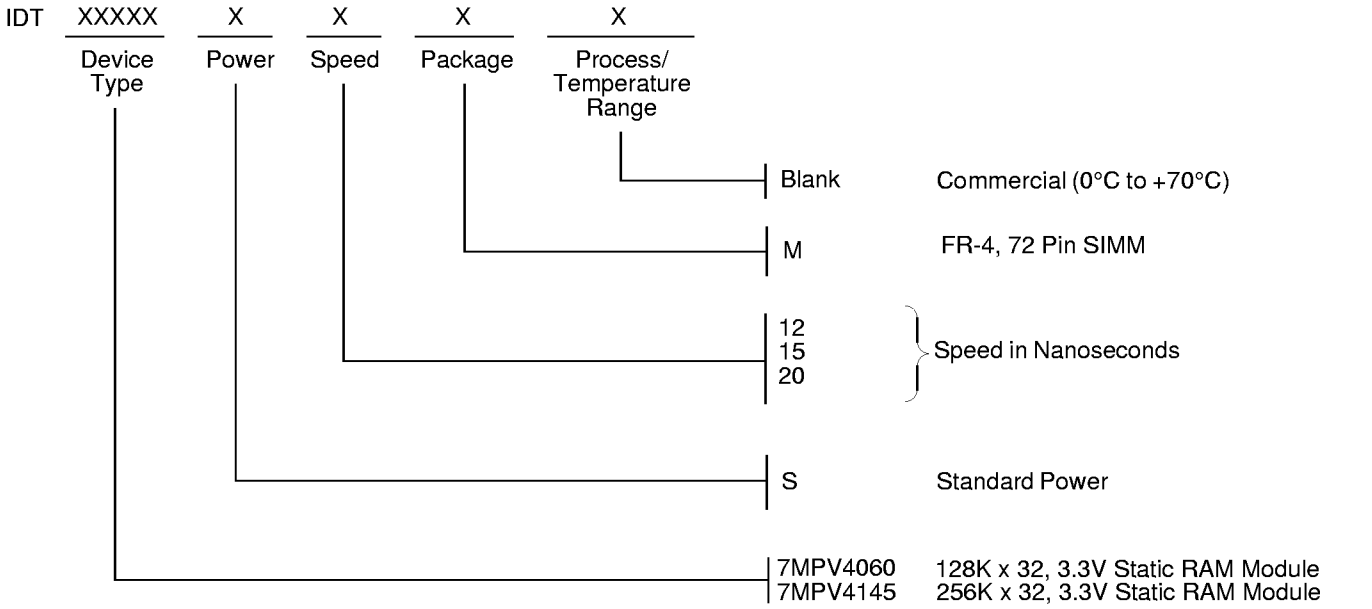
4054 drw 09

PACKAGE DIMENSIONS – IDT7MPV4060



4054 drw 10

ORDERING INFORMATION



4054 drw 11