IGBT

Low $V_{CE(sat)}$ IGBT in TRENCHSTOP™ 5 technology copacked with RAPID 1 fast and soft antiparallel diode

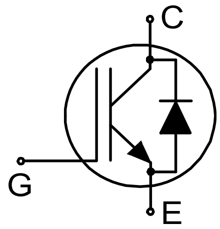
IKW75N65EL5

650V DuoPack IGBT and diode
Low $V_{CE(sat)}$ series fifth generation

Data sheet

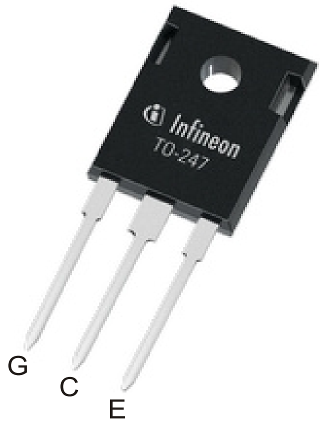
Industrial Power Control

Low $V_{CE(sat)}$ IGBT in TRENCHSTOP™ 5 technology copacked with RAPID 1 fast and soft antiparallel diode



Features and Benefits:

Low $V_{CE(sat)}$ L5 technology offering
- Very low collector-emitter saturation voltage V_{CEsat}
- Best-in-Class tradeoff between conduction and switching losses
- 650V breakdown voltage
- Low gate charge Q_G
- Maximum junction temperature 175°C
- Qualified according to JEDEC for target applications
- Pb-free lead plating
- RoHS compliant
- Complete product spectrum and PSpice models:
http://www.infineon.com/igbt/



Applications:

- Uninterruptible power supplies
- Solar photovoltaic inverters
- Welding machines

Key Performance and Package Parameters

Type	V_{CE}	I_C	V_{CEsat}, T_{vj}=25°C	T_{vjmax}	Marking	Package
IKW75N65EL5	650V	75A	1.1V	175°C	K75EEL5	PG-TO247-3

Table of Contents

Maximum Ratings

For optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

Parameter	Symbol	Value	Unit
Collector-emitter voltage, $T_{vj} \geq 25°C$	V_{CE}	650	V
DC collector current, limited by T_{vjmax}[1)] T_c = 25°C T_c = 100°C	I_C	 80.0 80.0	A
Pulsed collector current, t_p limited by T_{vjmax}[2)]	I_{Cpuls}	300.0	A
Turn off safe operating area $V_{CE} \leq 650V$, $T_{vj} \leq 175°C$, $t_p = 1µs$[2)]	-	300.0	A
Diode forward current, limited by T_{vjmax} T_c = 25°C value limited by bondwire T_c = 100°C	I_F	 90.0 89.0	A
Diode pulsed current, t_p limited by T_{vjmax}[2)]	I_{Fpuls}	300.0	A
Gate-emitter voltage Transient Gate-emitter voltage ($t_p \leq 10µs$, $D < 0.010$)	V_{GE}	±20 ±30	V
Power dissipation T_c = 25°C Power dissipation T_c = 100°C	P_{tot}	536.0 268.0	W
Operating junction temperature	T_{vj}	-40...+175	°C
Storage temperature	T_{stg}	-55...+150	°C
Soldering temperature,[3)] wave soldering 1.6mm (0.063in.) from case for 10s		 260	°C
Mounting torque, M3 screw Maximum of mounting processes: 3	M	0.6	Nm

Thermal Resistance

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
R_{th} Characteristics						
IGBT thermal resistance, junction - case	$R_{th(j-c)}$		-	-	0.28	K/W
Diode thermal resistance, junction - case	$R_{th(j-c)}$		-	-	0.46	K/W
Thermal resistance junction - ambient	$R_{th(j-a)}$		-	-	40	K/W

[1)] Both values limited by bondwires.
[2)] Defined by design. Not subject to production test.
[3)] Package not recommended for surface mount applications.

Electrical Characteristic, at T_{vj} = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Static Characteristic						
Collector-emitter breakdown voltage	$V_{(BR)CES}$	V_{GE} = 0V, I_C = 0.20mA	650	-	-	V
Collector-emitter saturation voltage	V_{CEsat}	V_{GE} = 15.0V, I_C = 75.0A T_{vj} = 25°C T_{vj} = 100°C T_{vj} = 150°C	 - - -	 1.10 1.11 1.12	 1.35 - -	V
Diode forward voltage	V_F	V_{GE} = 0V, I_F = 75.0A T_{vj} = 25°C T_{vj} = 100°C T_{vj} = 150°C	 - - -	 1.40 1.42 1.40	 1.70 - -	V
Gate-emitter threshold voltage	$V_{GE(th)}$	I_C = 1.00mA, V_{CE} = 20V	4.2	5.0	5.8	V
Zero gate voltage collector current	I_{CES}	V_{CE} = 650V, V_{GE} = 0V T_{vj} = 25°C T_{vj} = 150°C T_{vj} = 175°C	 - - -	 - 1000 5000	 40 - -	µA
Gate-emitter leakage current	I_{GES}	V_{CE} = 0V, V_{GE} = 20V	-	-	100	nA
Transconductance	g_{fs}	V_{CE} = 20V, I_C = 75.0A	-	155.0	-	S

Electrical Characteristic, at T_{vj} = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Dynamic Characteristic						
Input capacitance	C_{ies}	V_{CE} = 25V, V_{GE} = 0V f = 1000kHz	-	12100	-	pF
Output capacitance	C_{oes}		-	150	-	
Reverse transfer capacitance	C_{res}		-	42	-	
Gate charge	Q_G	V_{CC} = 520V, I_C = 75.0A, V_{GE} = 15V	-	436.0	-	nC
Internal emitter inductance measured 5mm (0.197 in.) from case	L_E		-	13.0	-	nH

Switching Characteristic, Inductive Load

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
IGBT Characteristic, at T_{vj} = 25°C						
Turn-on delay time	$t_{d(on)}$	T_{vj} = 25°C, V_{CC} = 400V, I_C = 75.0A, V_{GE} = 0.0/15.0V, $R_{G(on)}$ = 4.0Ω, $R_{G(off)}$ = 4.0Ω, $L\sigma$ = 40nH, $C\sigma$ = 30pF $L\sigma$, $C\sigma$ from Fig. E Energy losses include "tail" and diode reverse recovery.	-	40	-	ns
Rise time	t_r		-	11	-	ns
Turn-off delay time	$t_{d(off)}$		-	275	-	ns
Fall time	t_f		-	50	-	ns
Turn-on energy	E_{on}		-	1.61	-	mJ
Turn-off energy	E_{off}		-	3.20	-	mJ
Total switching energy	E_{ts}		-	4.81	-	mJ

Diode Characteristic, at T_{vj} = 25°C

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Diode reverse recovery time	t_{rr}	T_{vj} = 25°C, V_R = 400V, I_F = 75.0A, di_F/dt = 1500A/μs	-	114	-	ns
Diode reverse recovery charge	Q_{rr}		-	1.37	-	μC
Diode peak reverse recovery current	I_{rrm}		-	29.0	-	A
Diode peak rate of fall of reverse recovery current during t_b	di_{rr}/dt		-	-2170	-	A/μs

Switching Characteristic, Inductive Load

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
IGBT Characteristic, at T_{vj} = 150°C						
Turn-on delay time	$t_{d(on)}$	T_{vj} = 150°C, V_{CC} = 400V, I_C = 75.0A, V_{GE} = 0.0/15.0V, $R_{G(on)}$ = 4.0Ω, $R_{G(off)}$ = 4.0Ω, $L\sigma$ = 40nH, $C\sigma$ = 30pF $L\sigma$, $C\sigma$ from Fig. E Energy losses include “tail” and diode reverse recovery.	-	39	-	ns
Rise time	t_r		-	14	-	ns
Turn-off delay time	$t_{d(off)}$		-	330	-	ns
Fall time	t_f		-	144	-	ns
Turn-on energy	E_{on}		-	2.12	-	mJ
Turn-off energy	E_{off}		-	5.10	-	mJ
Total switching energy	E_{ts}		-	7.22	-	mJ

Diode Characteristic, at T_{vj} = 150°C

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Diode reverse recovery time	t_{rr}	T_{vj} = 150°C, V_R = 400V, I_F = 75.0A, di_F/dt = 1500A/μs	-	95	-	ns
Diode reverse recovery charge	Q_{rr}		-	2.43	-	μC
Diode peak reverse recovery current	I_{rrm}		-	40.0	-	A
Diode peak rate of fall of reverse recovery current during t_b	di_{rr}/dt		-	-2900	-	A/μs

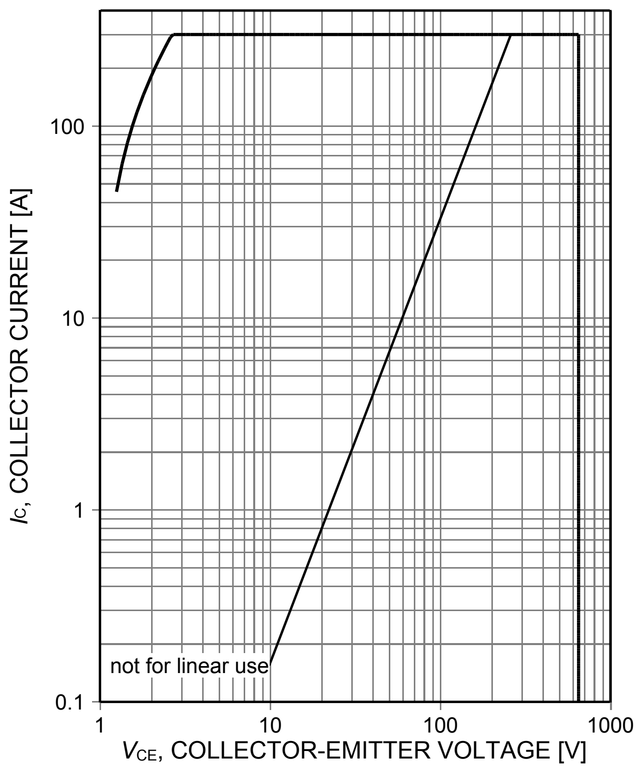


Figure 1. **Forward bias safe operating area**
(D=0, T_C=25°C, T_{vj}≤175°C, V_{GE}=15V, t_p=1µs, I_{Cmax} defined by design - not subject to production test)

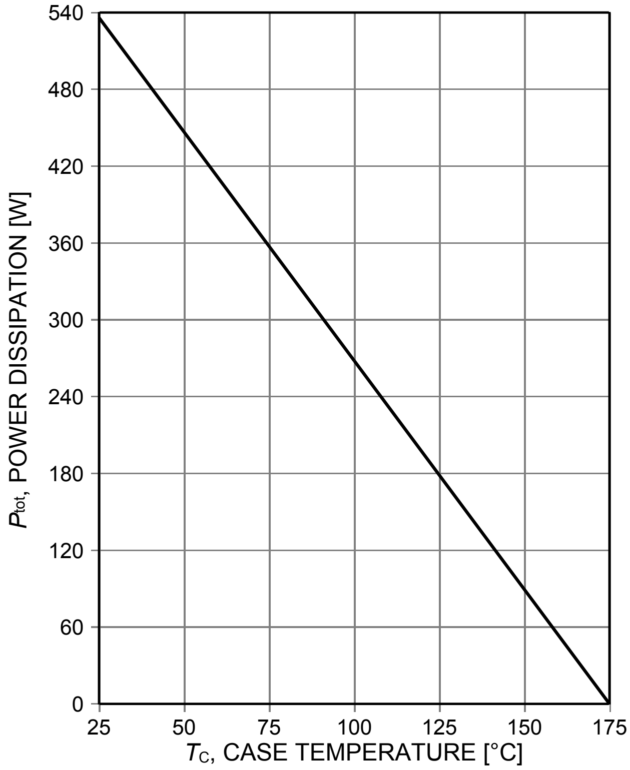


Figure 2. **Power dissipation as a function of case temperature**
(T_{vj}≤175°C)

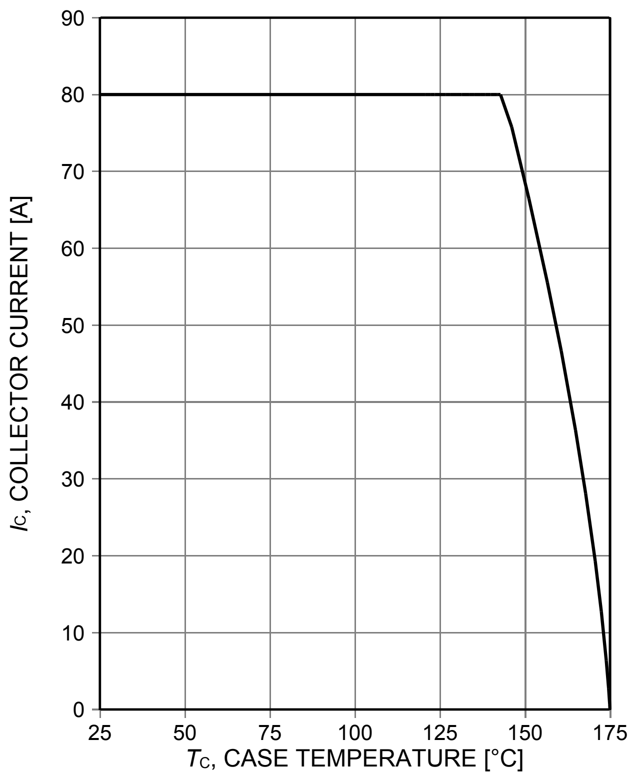


Figure 3. **Collector current as a function of case temperature**
(V_{GE}≥15V, T_{vj}≤175°C)

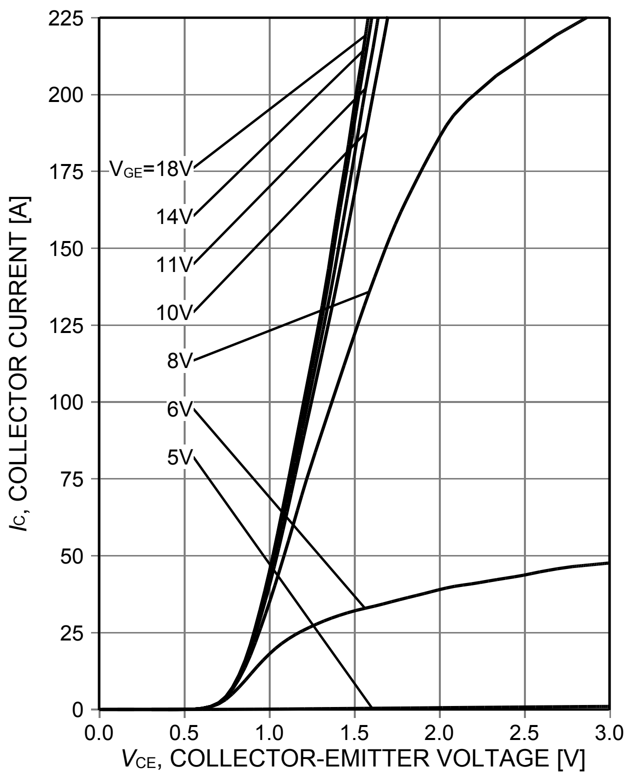


Figure 4. **Typical output characteristic**
(T_{vj}=25°C)

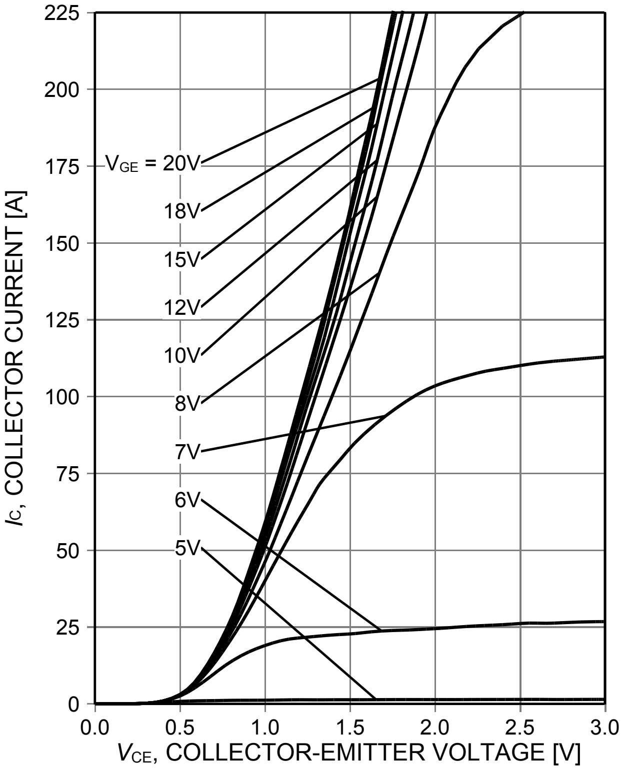


Figure 5. **Typical output characteristic**
(T_{vj}=175°C)

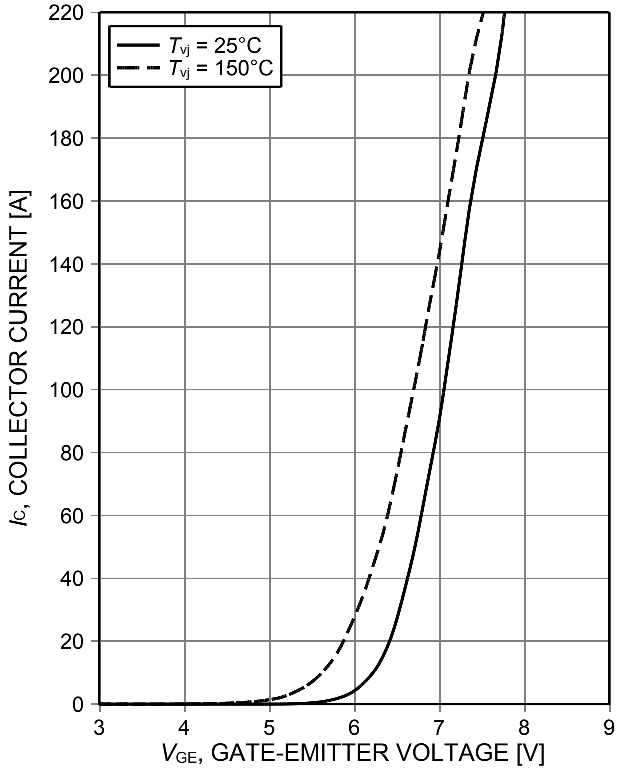


Figure 6. **Typical transfer characteristic**
(V_{CE}=20V)

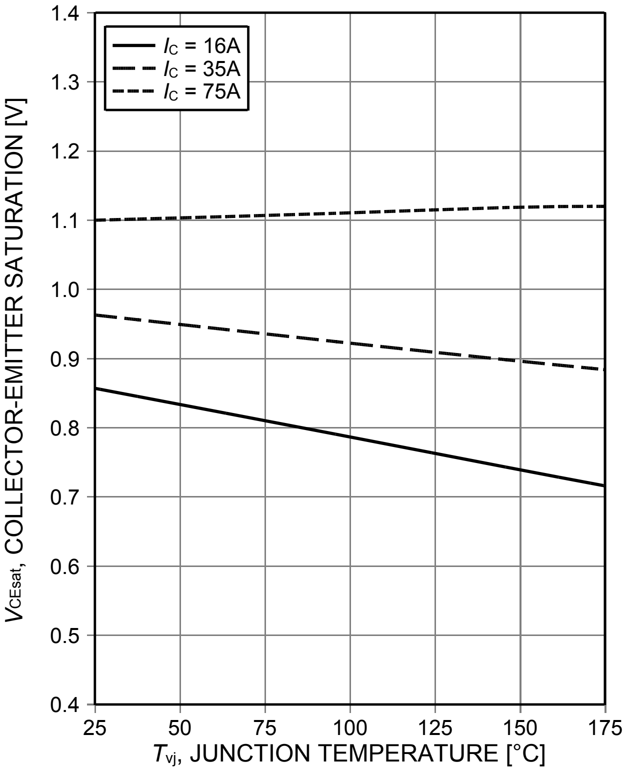


Figure 7. **Typical collector-emitter saturation voltage as a function of junction temperature**
(V_{GE}=15V)

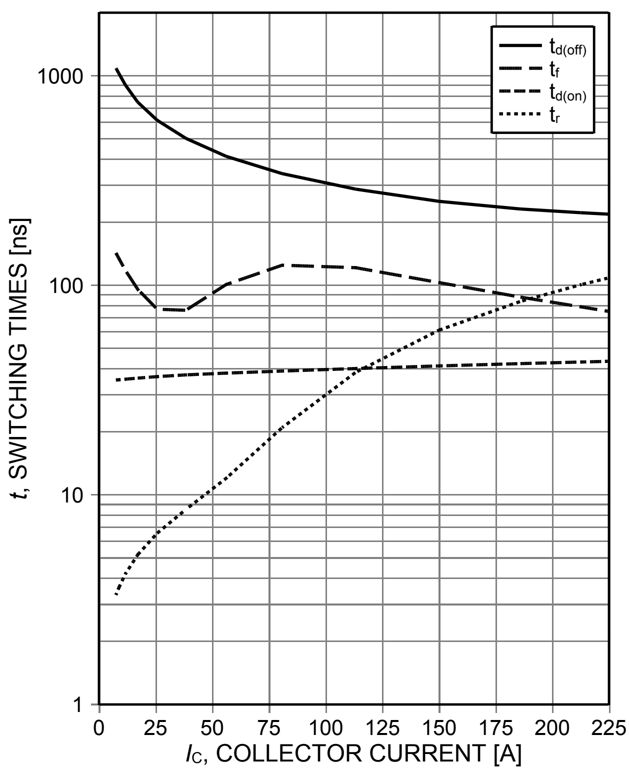


Figure 8. **Typical switching times as a function of collector current**
(inductive load, T_{vj}=150°C, V_{CE}=400V, V_{GE}=0/15V, $R_{G(on)}$=4Ω, $R_{G(off)}$=4Ω, dynamic test circuit in Figure E)

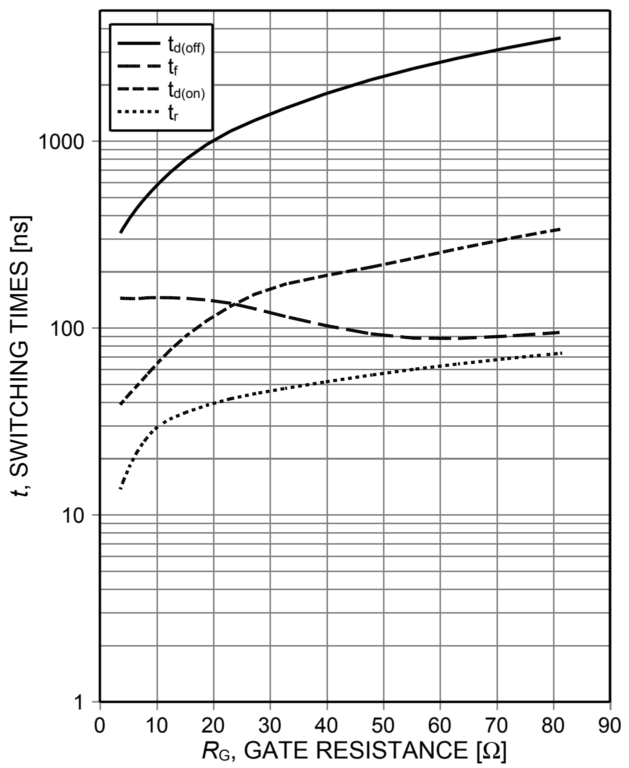


Figure 9. **Typical switching times as a function of gate resistance**
(inductive load, T_{vj}=150°C, V_{CE}=400V, V_{GE}=0/15V, I_C=75A, dynamic test circuit in Figure E)

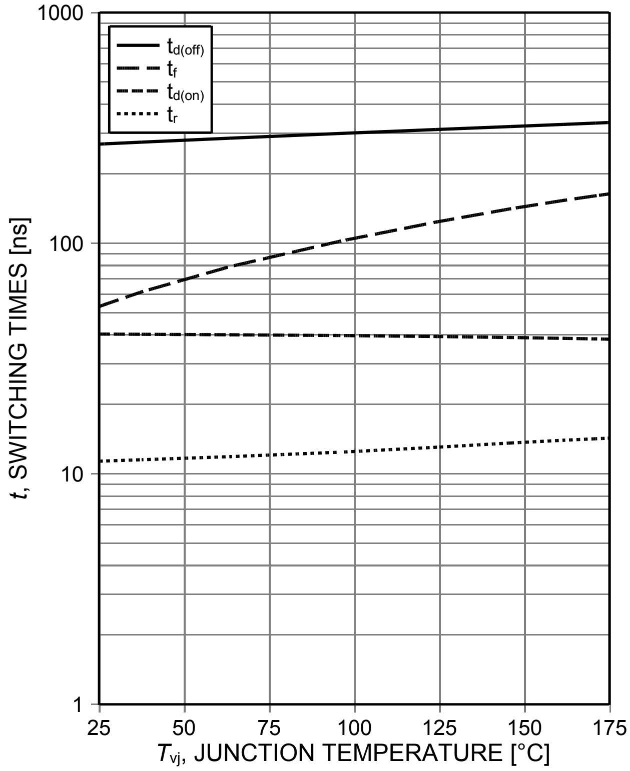


Figure 10. **Typical switching times as a function of junction temperature**
(inductive load, V_{CE}=400V, V_{GE}=0/15V, I_C=75A, $R_{G(on)}$=4Ω, $R_{G(off)}$=4Ω, dynamic test circuit in Figure E)

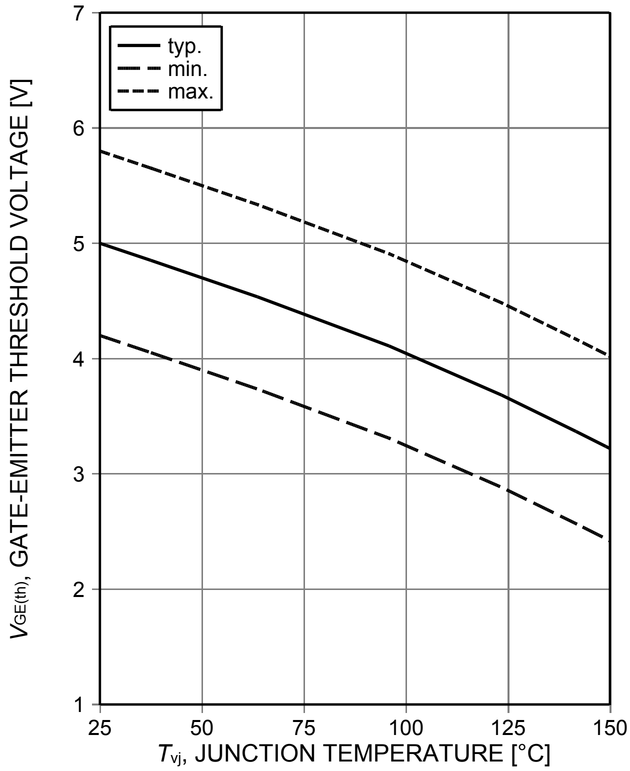


Figure 11. **Gate-emitter threshold voltage as a function of junction temperature**
(I_C=1mA)

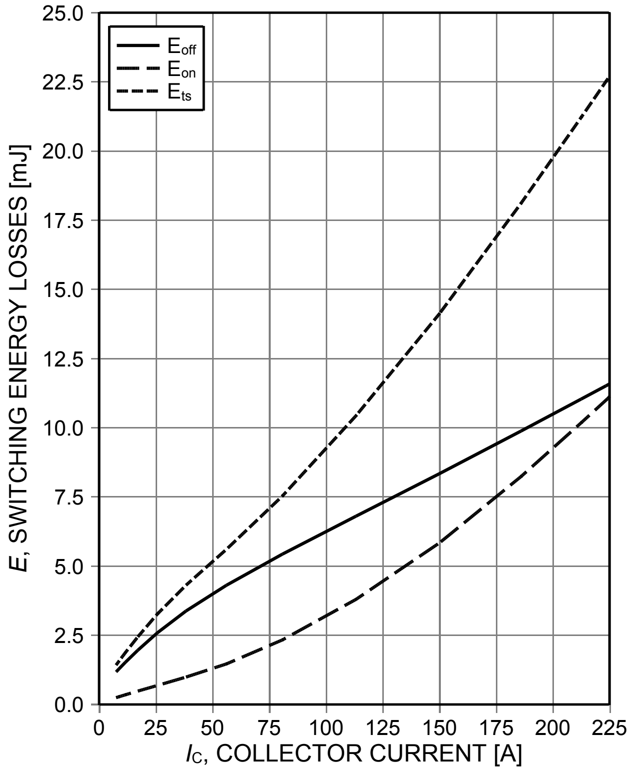


Figure 12. **Typical switching energy losses as a function of collector current**
(inductive load, T_{vj}=150°C, V_{CE}=400V, V_{GE}=0/15V, $R_{G(on)}$=4Ω, $R_{G(off)}$=4Ω, dynamic test circuit in Figure E)

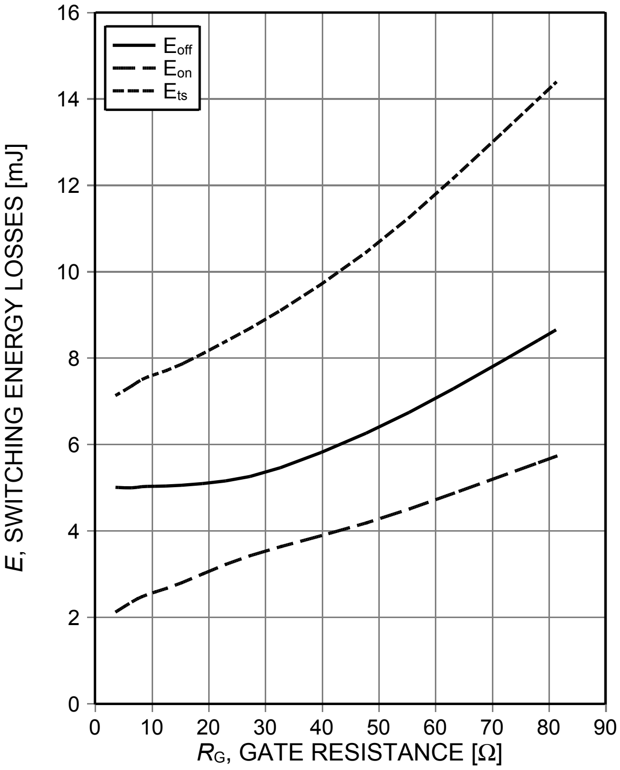


Figure 13. **Typical switching energy losses as a function of gate resistance**
(inductive load, T_{vj}=150°C, V_{CE}=400V, V_{GE}=0/15V, I_C=75A, dynamic test circuit in Figure E)

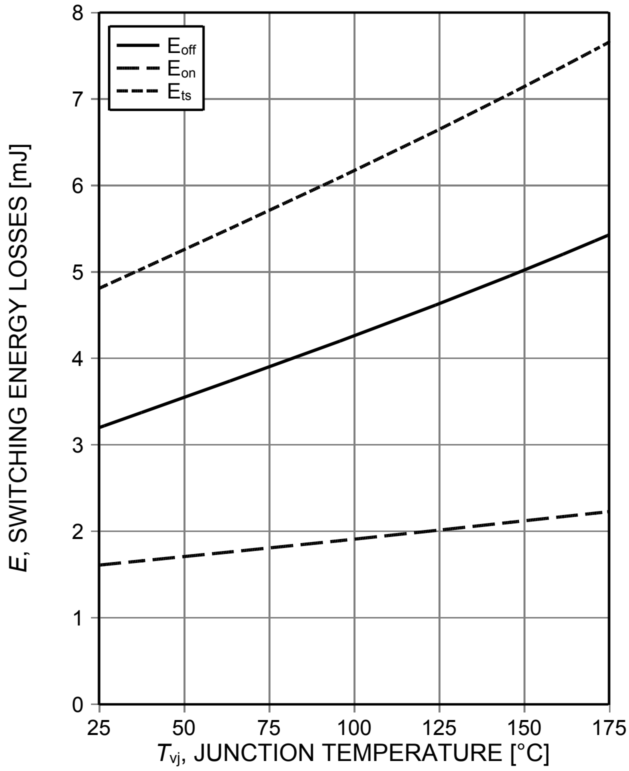


Figure 14. **Typical switching energy losses as a function of junction temperature**
(inductive load, V_{CE}=400V, V_{GE}=0/15V, I_C=75A, $R_{G(on)}$=4Ω, $R_{G(off)}$=4Ω, dynamic test circuit in Figure E)

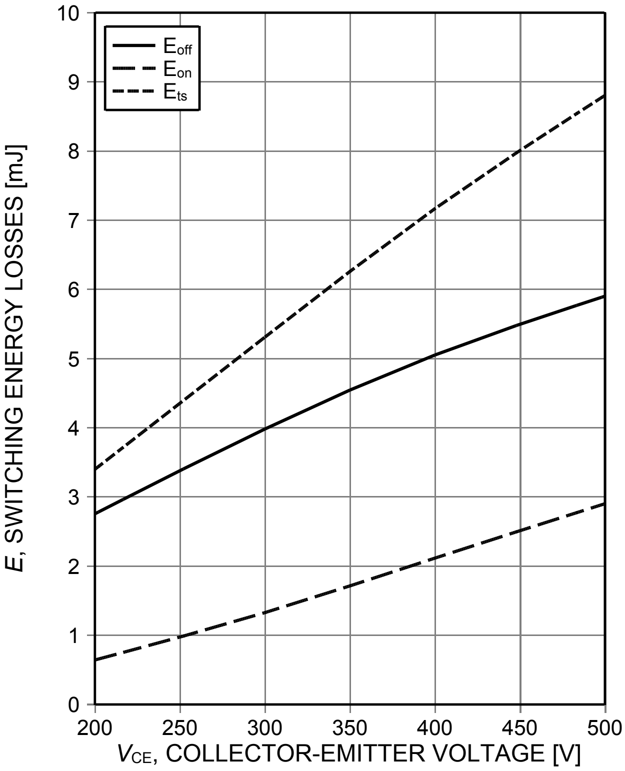


Figure 15. **Typical switching energy losses as a function of collector emitter voltage**
(inductive load, T_{vj}=150°C, V_{GE}=0/15V, I_C=75A, $R_{G(on)}$=4Ω, $R_{G(off)}$=4Ω, dynamic test circuit in Figure E)

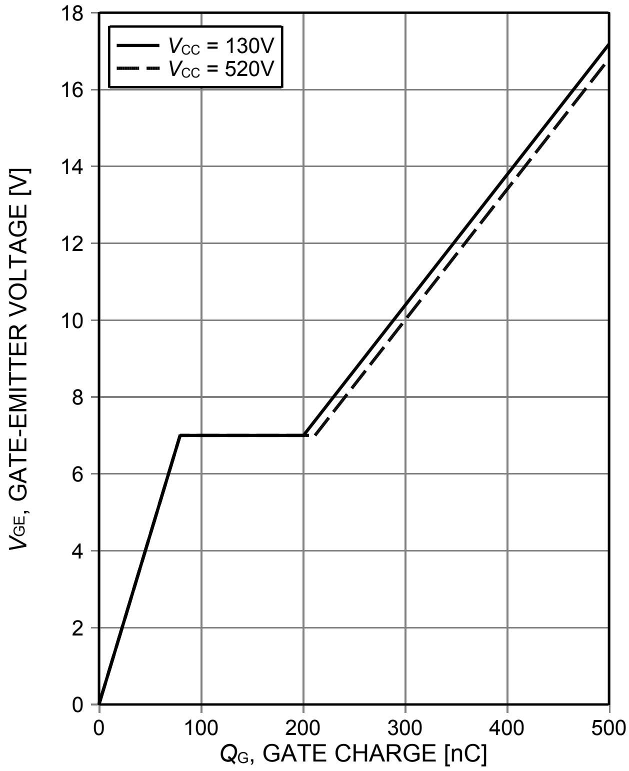


Figure 16. **Typical gate charge**
(I_C=75A)

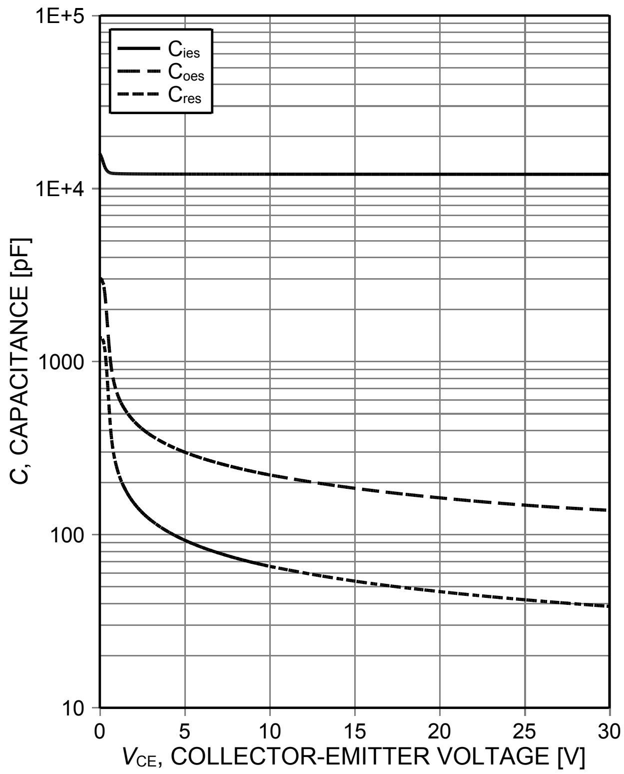


Figure 17. **Typical capacitance as a function of collector-emitter voltage**
(V_{GE}=0V, f=1MHz)

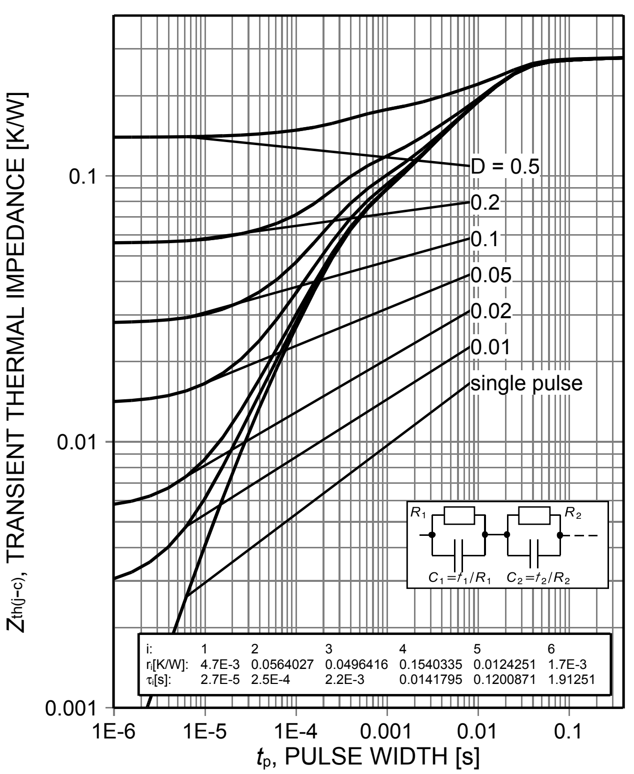


Figure 18. **IGBT transient thermal impedance**
(D=t_p/T)

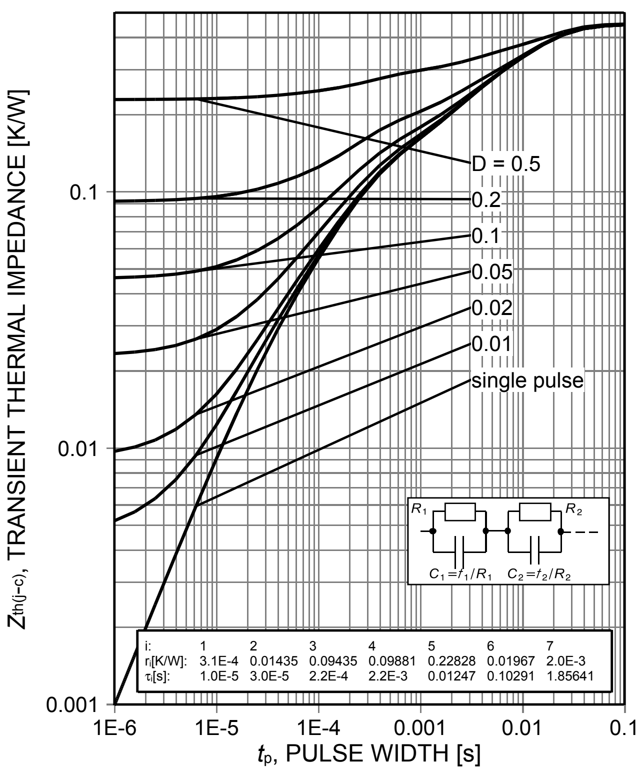


Figure 19. **Diode transient thermal impedance as a function of pulse width**
(D=t_p/T)

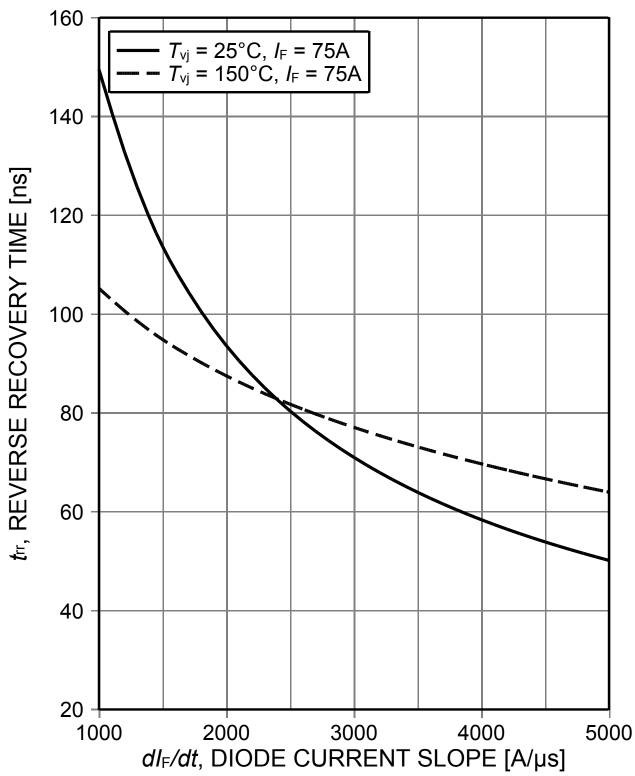


Figure 20. **Typical reverse recovery time as a function of diode current slope**
(V_R=400V)

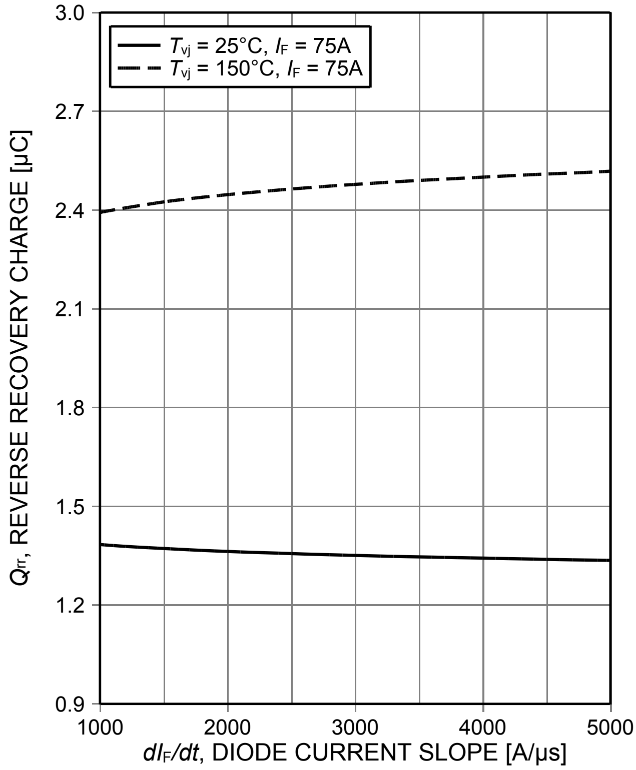


Figure 21. **Typical reverse recovery charge as a function of diode current slope**
(V_R=400V)

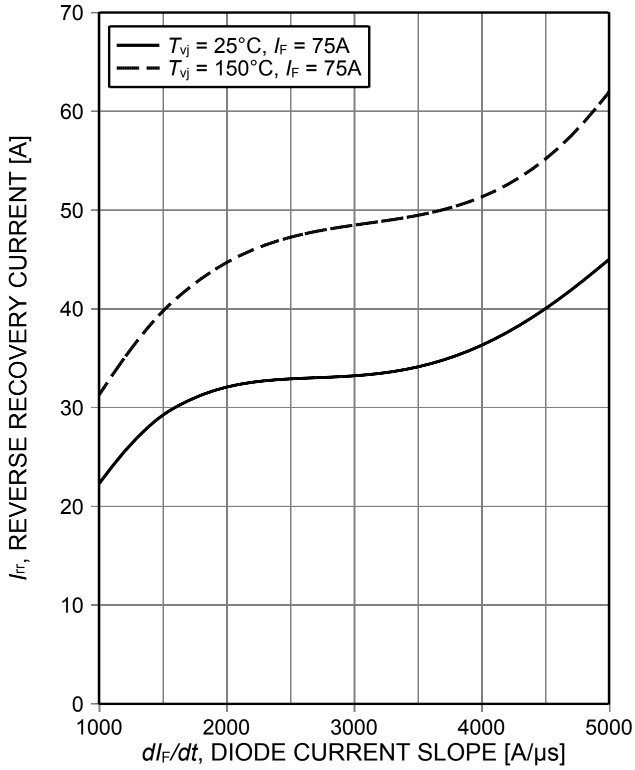


Figure 22. **Typical reverse recovery current as a function of diode current slope**
(V_R=400V)

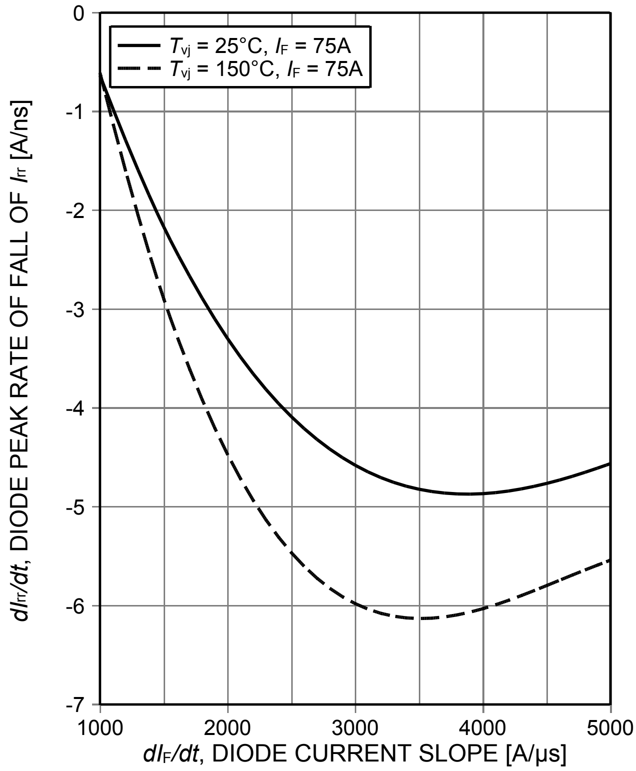


Figure 23. **Typical diode peak rate of fall of reverse recovery current as a function of diode current slope**
(V_R=400V)

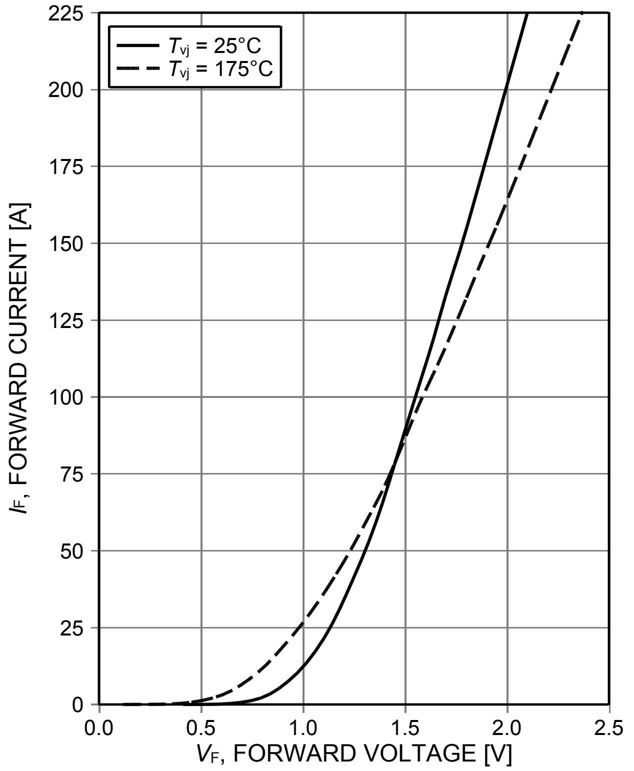


Figure 24. **Typical diode forward current as a function of forward voltage**

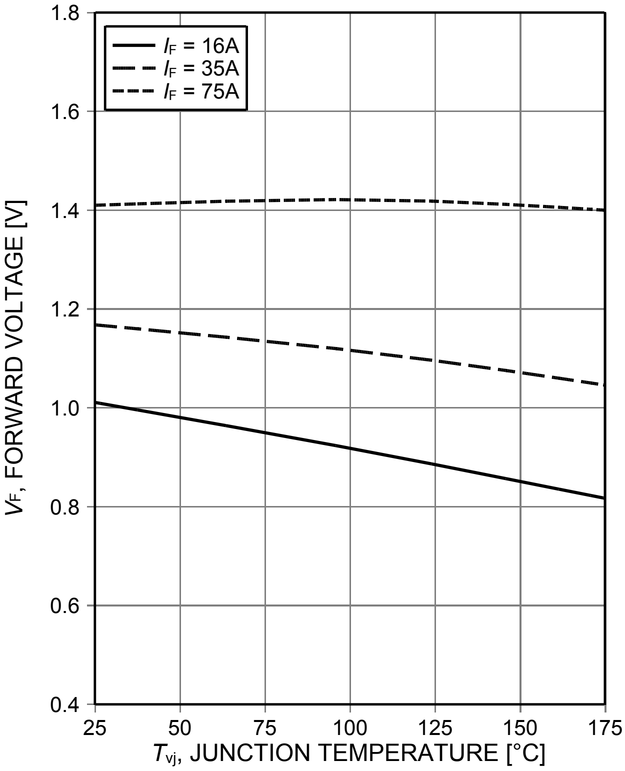
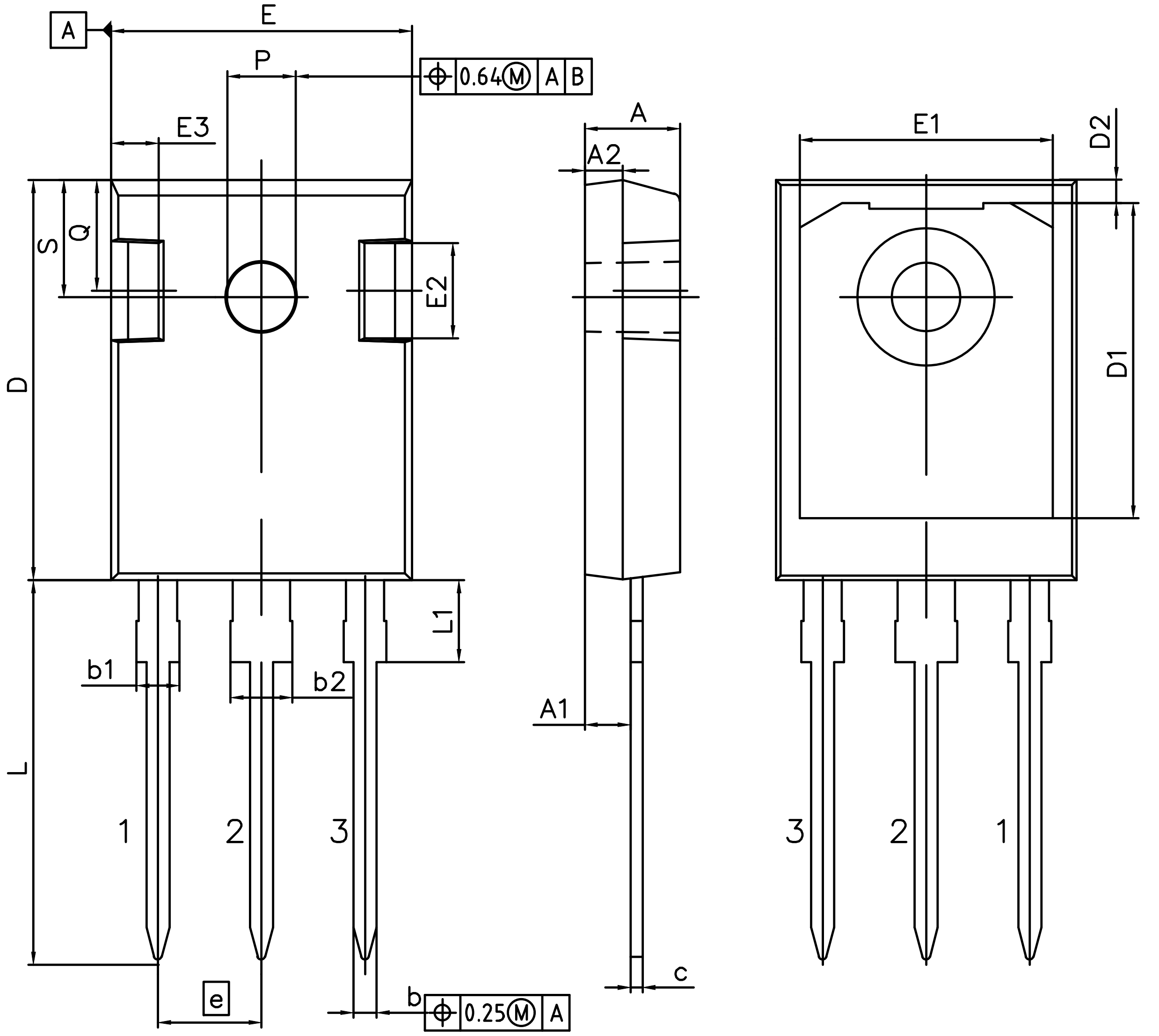


Figure 25. **Typical diode forward voltage as a function of junction temperature**

Package Drawing PG-TO247-3



DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.70	5.30
A1	2.20	2.60
A2	1.50	2.50
b	1.00	1.40
b1	1.60	2.41
b2	2.57	3.43
c	0.38	0.89
D	20.70	21.50
D1	13.08	17.65
D2	0.51	1.35
E	15.50	16.30
E1	12.38	14.15
E2	3.40	5.10
E3	1.00	2.60
e	5.44	
L	19.80	20.40
L1	3.85	4.50
P	3.50	3.70
Q	5.35	6.25
S	6.04	6.30

DOCUMENT NO.
Z8B00003327

REVISION
06

SCALE 3:1
0 1 2 3 4 5mm

EUROPEAN PROJECTION

ISSUE DATE
25.07.2018

Testing Conditions

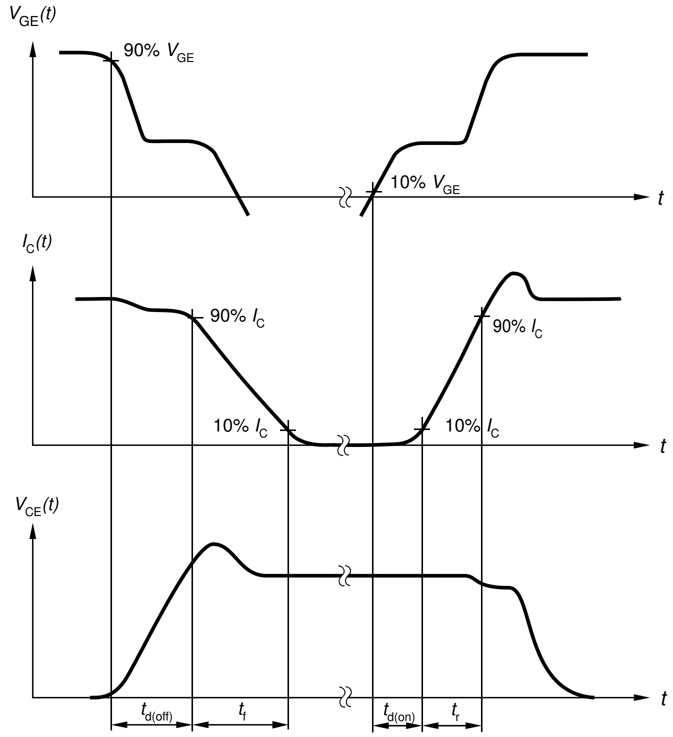


Figure A. **Definition of switching times**

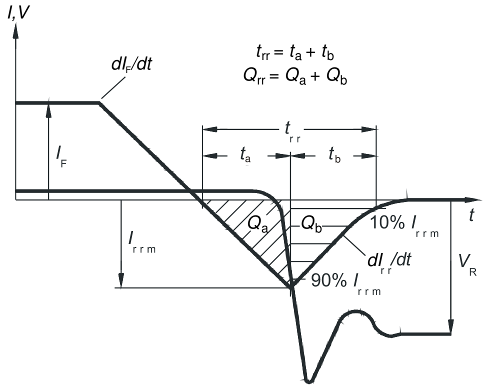


Figure C. **Definition of diode switching characteristics**

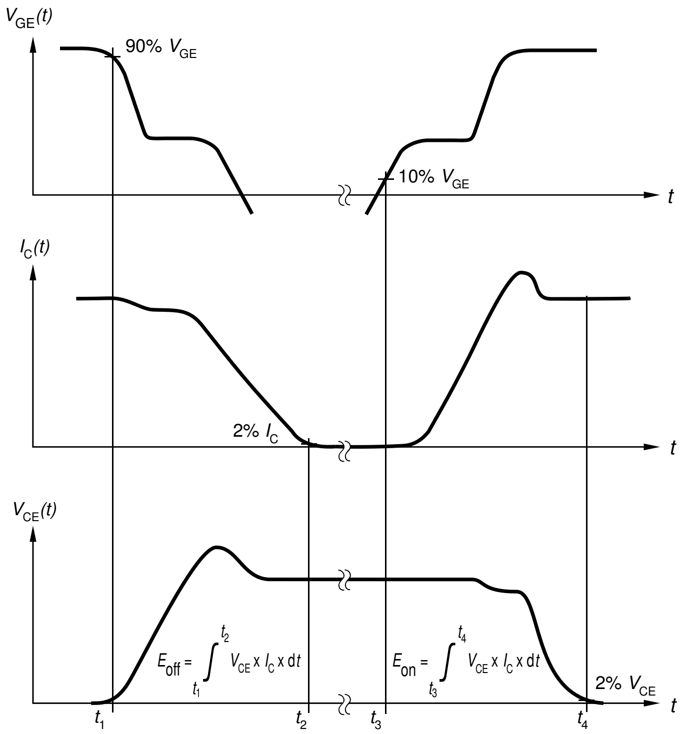


Figure B. **Definition of switching losses**

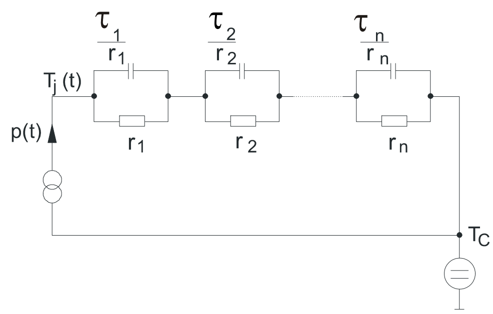


Figure D. **Thermal equivalent circuit**

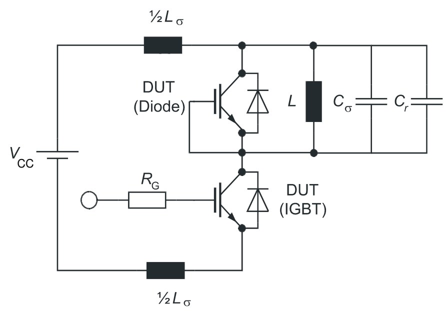


Figure E. **Dynamic test circuit**
Parasitic inductance L_{σ},
parasitic capacitor C_{σ},
relief capacitor C_r,
(only for ZVT switching)

Revision History

IKW75N65EL5

Revision: 2020-10-07, Rev. 2.2

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.1	2014-12-10	Final data sheet
2.2	2020-10-07	VGE(th): test condition update

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Published by
Infineon Technologies AG
81726 München, Germany

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