PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES MAY 6, 2017

General Description

The 87973I-147 is a LVCMOS/LVTTL clock generator. The 87973I-147 has three selectable inputs and provides 14 LVCMOS/LVTTL outputs.

The 87973I-147 is a highly flexible device. The three selectable inputs (1 differential and 2 single ended inputs) are often used in systems requiring redundant clock sources. Up to three different output frequencies can be generated among the three output banks.

The three output banks and feedback output each have their own output dividers which allows the device to generate a multitude of different bank frequency ratios and output-to-input frequency ratios. In addition, 2 outputs in Bank C (QC2, QC3) can be selected to be inverting or non-inverting. The output frequency range is 10MHz to 150MHz. The input frequency range is 6MHz to 120MHz.

The 87973I-147 also has a QSYNC output which can be used for system synchronization purposes. It monitors Bank A and Bank C outputs and goes low one period prior to coincident rising edges of Bank A and Bank C clocks. QSYNC then goes high again when the coincident rising edges of Bank A and Bank C occur. This feature is used primarily in applications where Bank A and Bank C are running at different frequencies, and is particularly useful when they are running at non-integer multiples of one another.

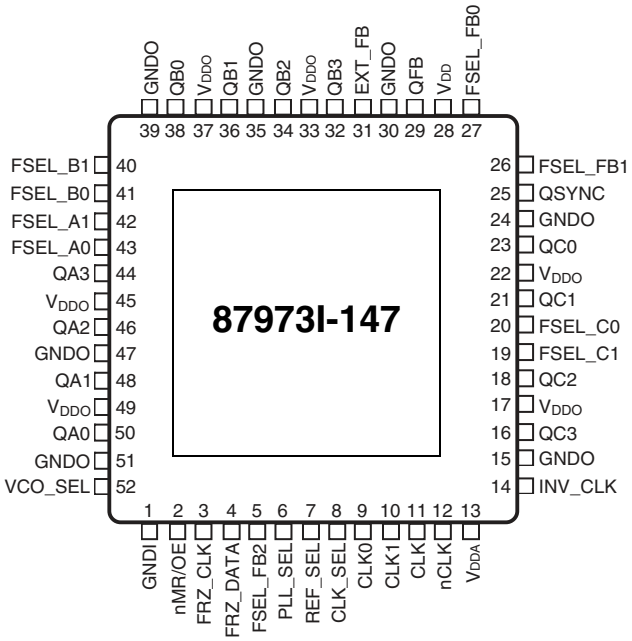
Example Applications:

1. *System Clock generator:* Use a 16.66MHz reference clock to generate eight 33.33MHz copies for PCI and four 100MHz copies for the CPU or PCI-X.
2. *Line Card Multiplier:* Multiply differential 62.5MHz from a back plane to single-ended 125MHz for the line Card ASICs and Gigabit Ethernet Serdes.
3. *Zero Delay buffer for Synchronous memory:* Fanout up to twelve 100MHz copies from a memory controller reference clock to the memory chips on a memory module with zero delay.

Features

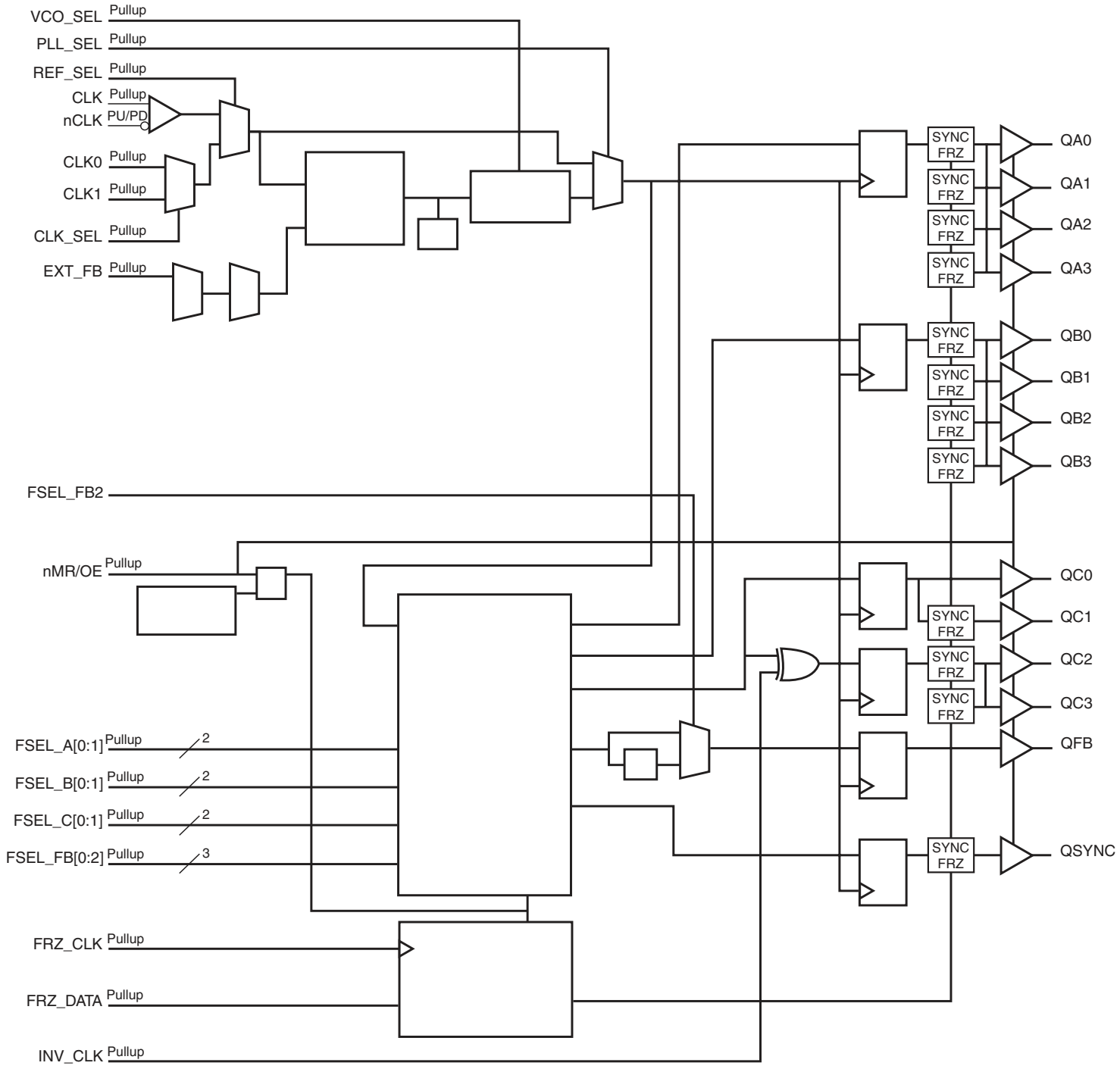
- Fully integrated PLL
- Fourteen LVCMOS/LVTTL outputs to include: twelve clocks, one feedback, one sync
- Selectable differential CLK, nCLK inputs or LVCMOS/LVTTL reference clock inputs
- CLK0, CLK1 can accept the following input levels: LVCMOS or LVTTL
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency range: 10MHz to 150MHz
- VCO range: 240MHz to 500MHz
- Output skew: 200ps (maximum)
- Cycle-to-cycle jitter, (all banks ÷4): 55ps (maximum)
- Full 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Compatible with PowerPC™and Pentium™Microprocessors
- Available in lead-free packages
- For drop-in replacement use 87973i

Pin Assignment

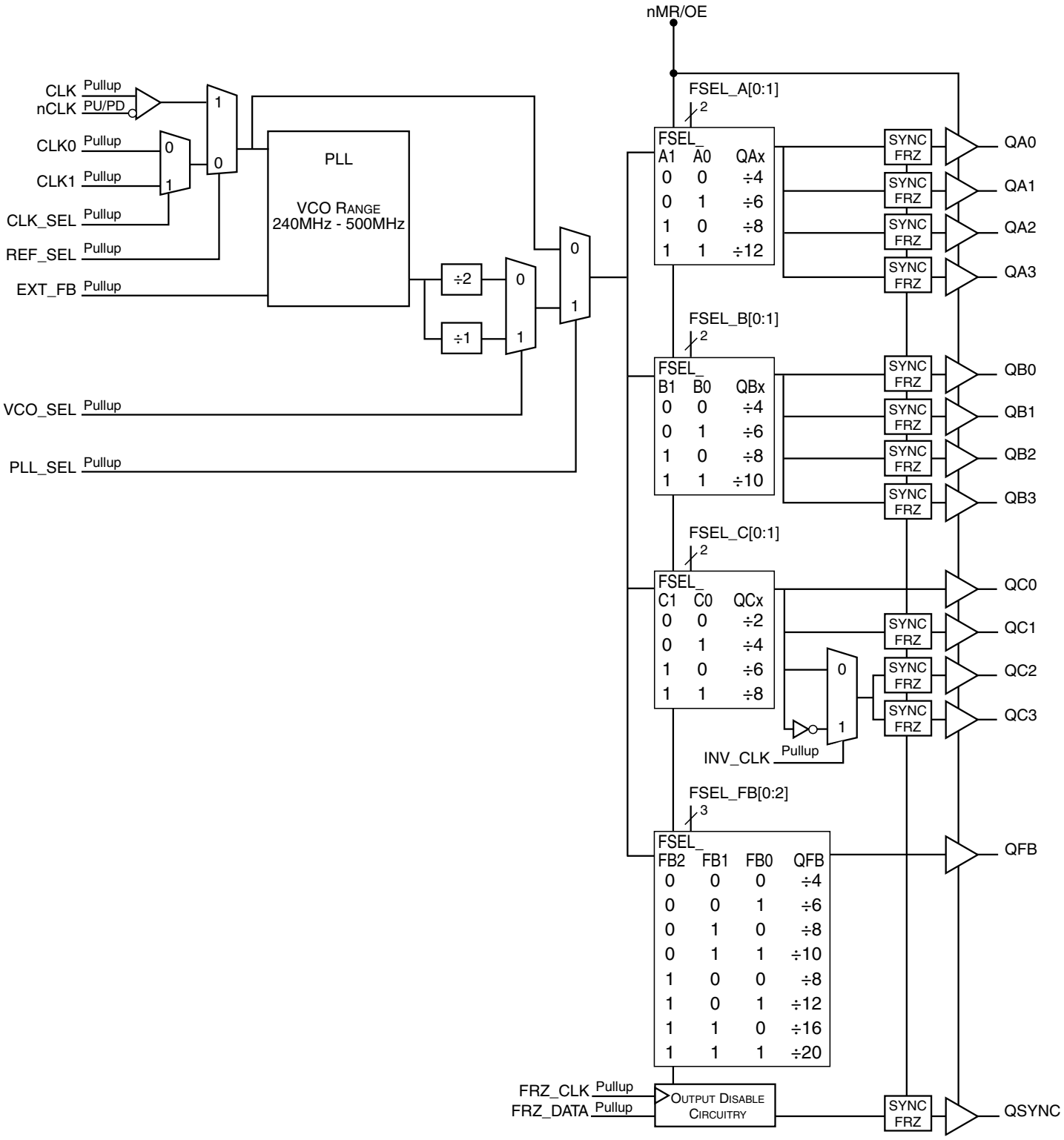


52-Lead, 10mm x 10mm LQFP

Block Diagram



Simplified Block Diagram



Pin Descriptions and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1	GNDI	Power		Power supply ground.
2	nMR/OE	Input	Pullup	Master reset and output enable. When HIGH, enables the outputs. When LOW, resets the outputs in a high-impedance state and resets output divide circuitry. Enables and disables all outputs. LVCMOS / LVTTL interface levels.
3	FRZ_CLK	Input	Pullup	Clock input for freeze circuitry. LVCMOS / LVTTL interface levels.
4	FRZ_DATA	Input	Pullup	Configuration data input for freeze circuitry. LVCMOS / LVTTL interface levels.
5, 26, 27	FSEL_FB2, FSEL_FB1, FSEL_FB0	Input	Pullup	Select pins control Feedback Divide value. LVCMOS / LVTTL interface levels. See Table 3B.
6	PLL_SEL	Input	Pullup	Selects between the PLL and reference clocks as the input to the output dividers. When HIGH, selects PLL. When LOW, bypasses the PLL and reference clocks. LVCMOS / LVTTL interface levels.
7	REF_SEL	Input	Pullup	Selects between CLK0 or CLK1 and CLK, nCLK inputs. When LOW, selects CLK0 or CLK1. When HIGH, CLK, nCLK inputs. LVCMOS / LVTTL interface levels.
8	CLK_SEL	Input	Pullup	Clock select input. When LOW, selects CLK0. When HIGH, selects CLK1. LVCMOS / LVTTL interface levels.
9, 10	CLK0, CLK1	Input	Pullup	Single-ended reference clock inputs. LVCMOS/LVTTL interface levels.
11	CLK	Input	Pullup	Non-inverting differential clock input.
12	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
13	V_{DDA}	Power		Analog supply pin.
14	INV_CLK	Input	Pullup	Inverted clock select for QC2 and QC3 outputs. LVCMOS / LVTTL interface levels.
15, 24, 30, 35, 39, 47, 51	GNDO	Power		Power supply ground.
16, 18, 21, 23	QC3, QC2, QC1, QC0	Output		Single-ended Bank C clock outputs. LVCMOS/ LVTTL interface levels.
17, 22, 33, 37, 45, 49	V_{DDO}	Power		Output power supply pins.
19, 20	FSEL_C1, FSEL_C0	Input	Pullup	Select pins for Bank C outputs. LVCMOS / LVTTL interface levels. See Table 3A.
25	QYSNC	Output		Synchronization output for Bank A and Bank C. Refer to Figure 1, Timing Diagrams. LVCMOS / LVTTL interface levels.
28	V_{DD}	Power		Power supply pin.
29	QFB	Output		Single-ended feedback clock output. LVCMOS / LVTTL interface levels.
31	EXT_FB	Input	Pullup	External feedback. LVCMOS / LVTTL interface levels.
32, 34, 36, 38	QB3, QB2, QB1, QB0	Output		Single-ended Bank B clock outputs. LVCMOS/ LVTTL interface levels.
40, 41	FSEL_B1, FSEL_B0	Input	Pullup	Select pins for Bank B outputs. LVCMOS / LVTTL interface levels. See Table 3A.
42, 43	FSEL_A1, FSEL_A0	Input	Pullup	Select pins for Bank A outputs. LVCMOS / LVTTL interface levels. See Table 3A.
44, 46 48, 50	QA3, QA2, QA1, QA0	Output		Single-ended Bank A clock outputs. LVCMOS/ LVTTL interface levels.
52	VCO_SEL	Input	Pullup	Selects VCO. When HIGH, selects VCO ÷ 1. When LOW, selects VCO ÷ 2. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDA}, V_{DDO} = 3.465V			18	pF
R_{OUT}	Output Impedance		5	7	12	Ω

Function Tables

Table 3A. Output Bank Configuration Select Function Table

Inputs		Outputs	Inputs		Outputs	Inputs		Outputs
FSEL_A1	FSEL_A0	QA	FSEL_B1	FSEL_B0	QB	FSEL_C1	FSEL_C0	QC
0	0	÷4	0	0	÷4	0	0	÷2
0	1	÷6	0	1	÷6	0	1	÷4
1	0	÷8	1	0	÷8	1	0	÷6
1	1	÷12	1	1	÷10	1	1	÷8

Table 3B. Feedback Configuration Select Function Table

Inputs			Outputs
FSEL_FB2	FSEL_FB1	FSEL_FB0	QFB
0	0	0	÷4
0	0	1	÷6
0	1	0	÷8
0	1	1	÷10
1	0	0	÷8
1	0	1	÷12
1	1	0	÷16
1	1	1	÷20

Table 3C. Control Input Select Function Table

Control Pin	Logic 0	Logic 1
VCO_SEL	VCO/2	VCO
REF_SEL	CLK0 or CLK1	XTAL
CLK_SEL	CLK0	CLK1
PLL_SEL	BYPASS PLL	Enable PLL
nMR/OE	Master Reset/Output High-Impedance	Enable Outputs
INV_CLK	Non-Inverted QC2, QC3	Inverted QC2, QC3

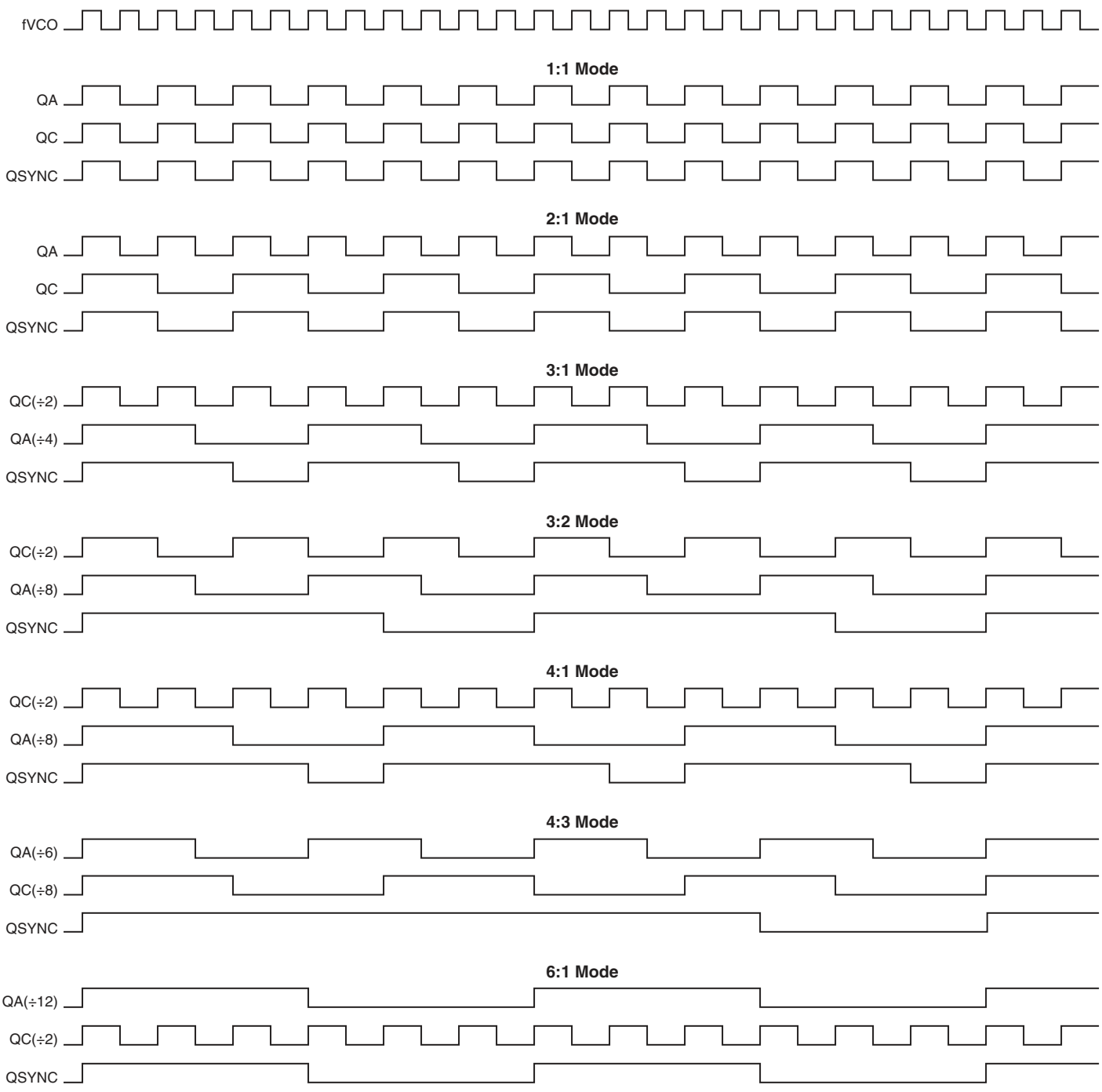


Figure 1. Timing Diagrams

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	42.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				225	mA
I_{DDA}	Analog Supply Current				20	mA

Table 4B. DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IN}	Input Current					±120	µA
V_{OH}	Output High Voltage; NOTE 1		I_{OH} = -20mA	2.4			V
V_{OL}	Output Low Voltage; NOTE 1		I_{OL} = 20mA			0.5	V
V_{PP}	Peak-to-Peak Input Voltage; NOTE 2, 3	CLK, nCLK		0.3		1	V
V_{CMRP}	Common Mode Input Voltage; NOTE 2, 3	CLK, nCLK		V_{DD} - 2		V_{DD} - 0.6	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information section. *Load Test Circuit diagram.*
NOTE 2: V_{IL} should not be less than -0.3V.
NOTE 3: Common mode input voltage is defined as V_{IH}.

Table 5. Input Frequency Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{IN}	Input Frequency	CLK0, CLK1; NOTE 1				120	MHz
		FRZ_CLK				20	MHz

NOTE 1: Input frequency depends on the feedback divide ratio to ensure "clock * feedback divide" is in the VCO range of 240MHz to 500MHz.

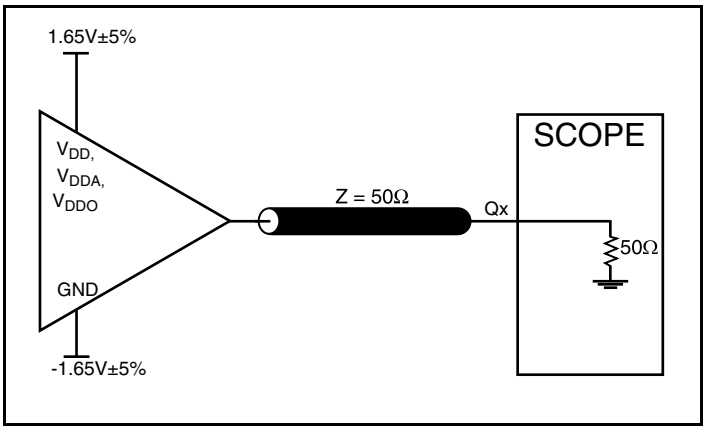
AC Electrical Characteristics

Table 6. AC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

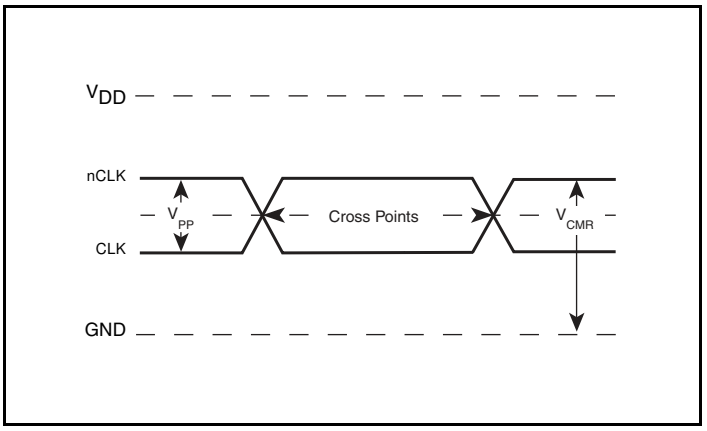
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		÷2			250	MHz
			÷4			125	MHz
			÷6			83.33	MHz
			÷8			62.5	MHz
			÷10			50	MHz
			÷12			41.66	MHz
t(Ø)	Static Phase Offset; NOTE 1	CLK0	QFB ÷ 8, In Frequency = 50MHz	-10	145	300	ps
		CLK1		-65	90	245	ps
		CLK, nCLK		-130	18	165	ps
*t*sk(o)	Output Skew; NOTE 2, 3					200	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 3		All Banks ÷ 4			55	ps
f_{VCO}	PLL VCO Lock Range			240		500	MHz
t_{LOCK}	PLL Lock Time; NOTE 4					10	ms
t_R / t_F	Output Rise/Fall Time		0.8V to 2V	150		700	ps
odc	Output Duty Cycle			45		55	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 4					10	ns
t_{PLZL}, t_{PHZ}	Output Disable Time; NOTE 4					8	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

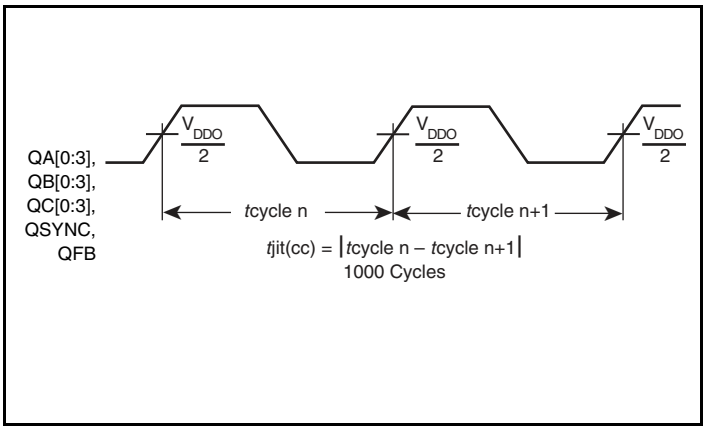
Parameter Measurement Information



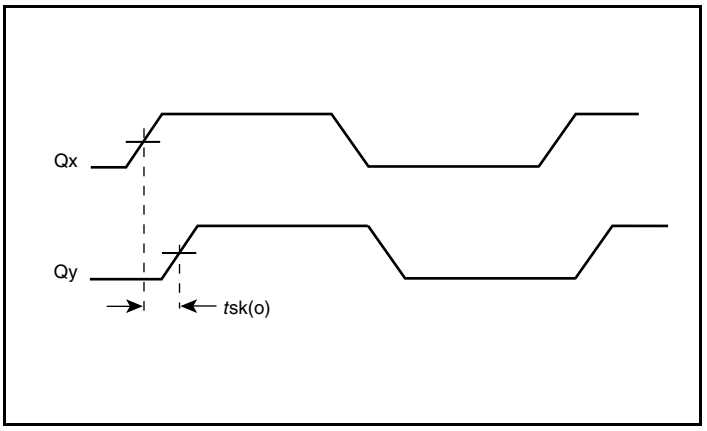
LVCMOS Output Load AC Test Circuit



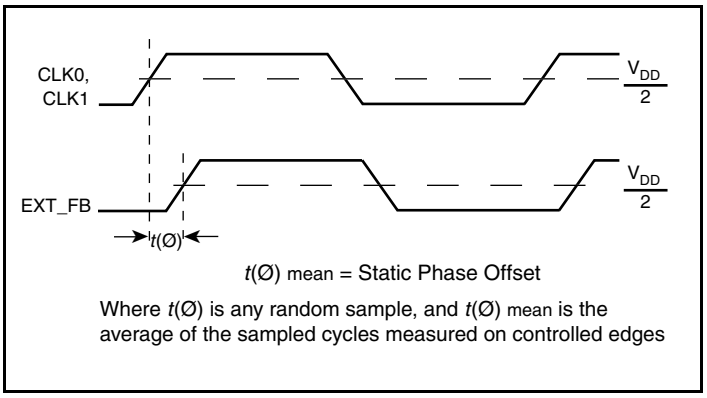
Differential Input Level



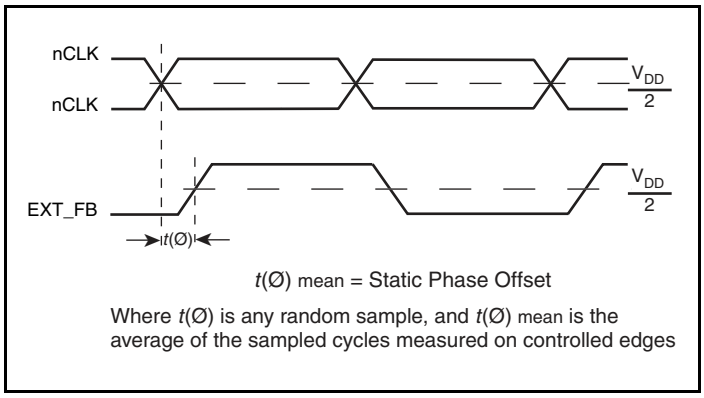
Cycle-to-Cycle Jitter



Output Skew

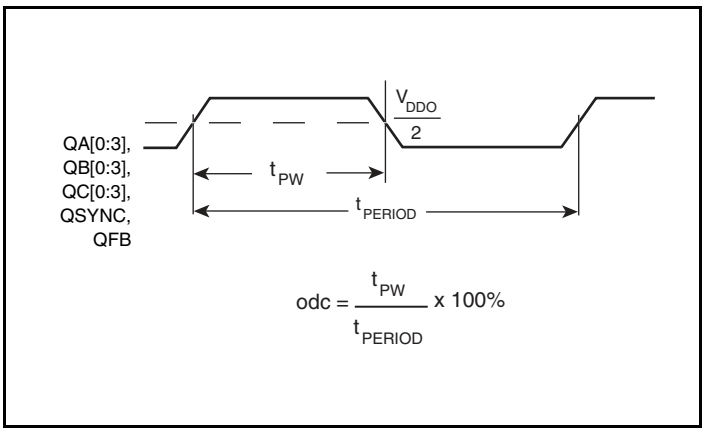


LVCMOS Static Phase Offset

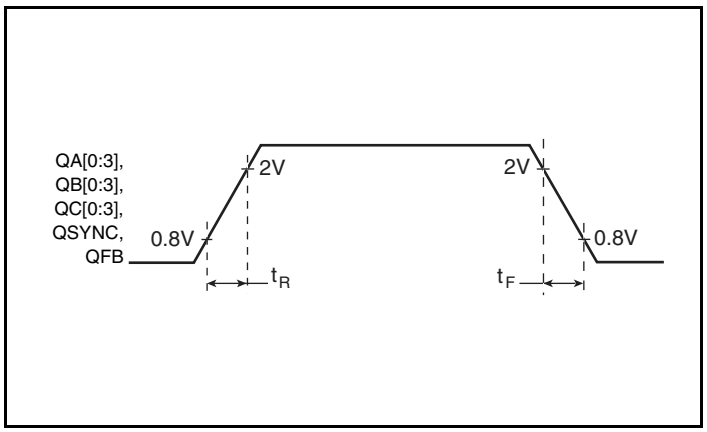


Differential Static Phase Offset

Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width Period



Output Rise/Fall Time

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

CLK Inputs

For applications not requiring the use of the clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK to ground.

LVCMOS Control Pins

All control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 87973I-147 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 2* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

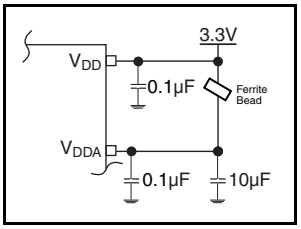


Figure 2. Power Supply Filtering

Wiring the Differential Input to Accept Single-Ended Levels

Figure 3 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

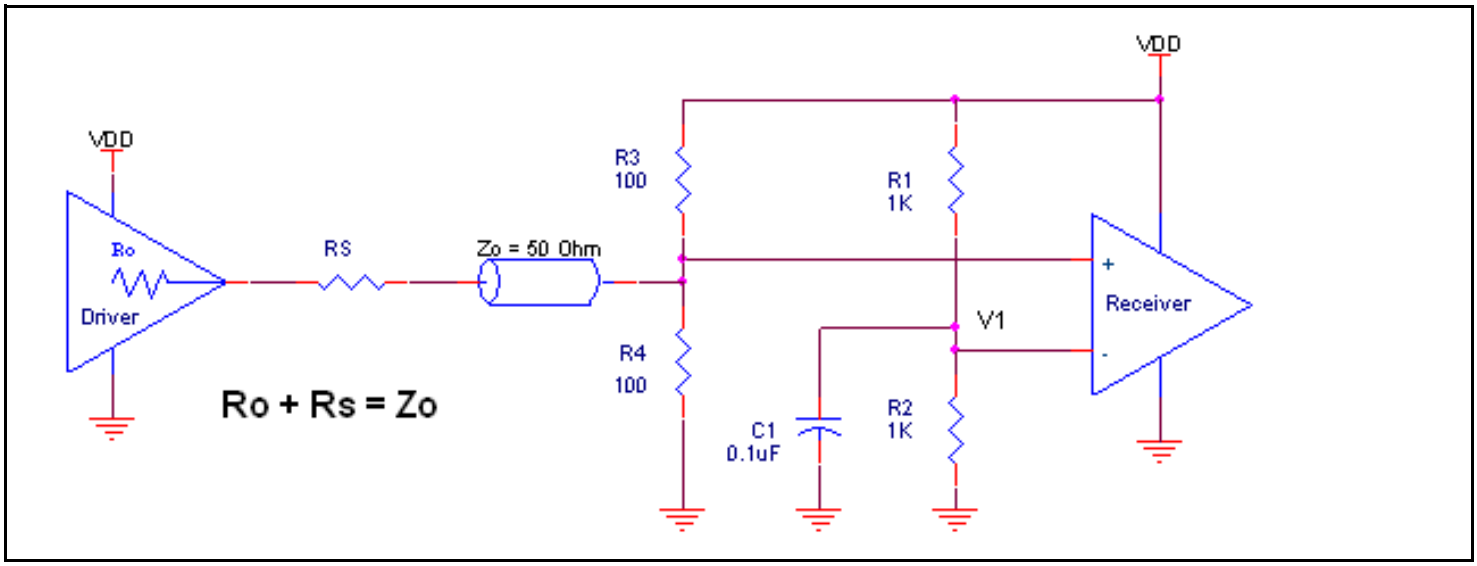


Figure 3. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 4A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

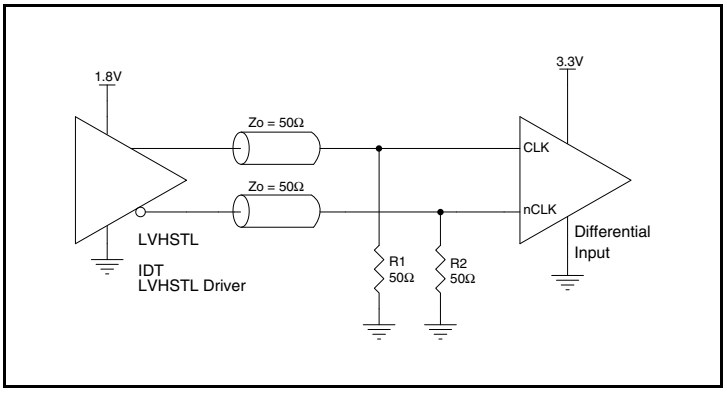


Figure 4A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

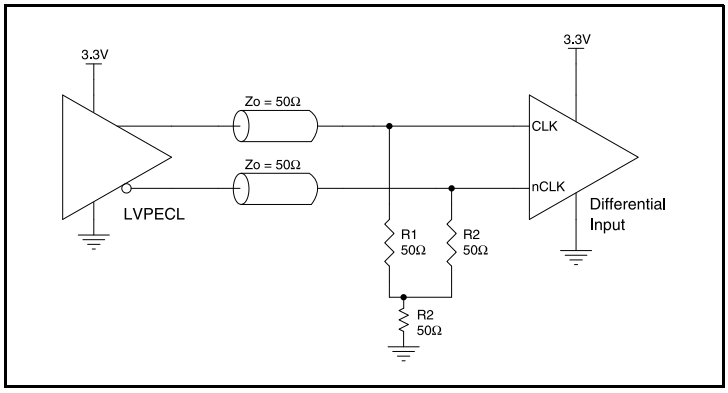


Figure 4B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

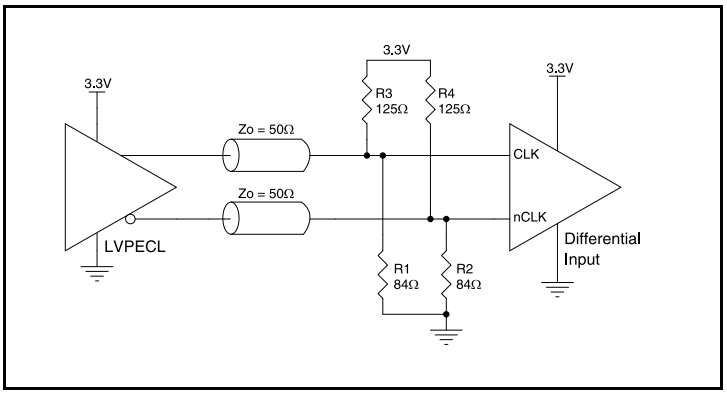


Figure 4C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

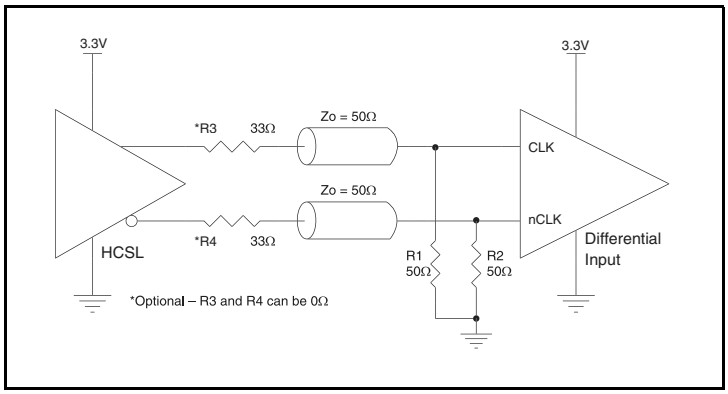


Figure 4D. CLK/nCLK Input Driven by a 3.3V HCSL Driver

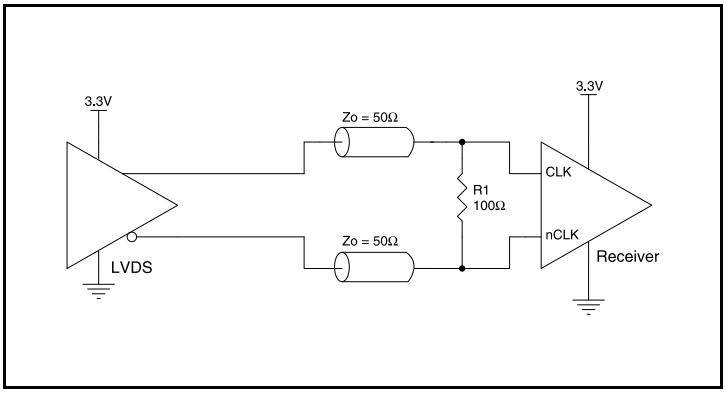


Figure 4E. CLK/nCLK Input Driven by a 3.3V LVDS Driver

Using the Output Freeze Circuitry

OVERVIEW

To enable low power states within a system, each output of 87973I-147 (Except QC0 and QFB) can be individually frozen (stopped in the logic “0” state) using a simple serial interface to a 12 bit shift register. A serial interface was chosen to eliminate the need for each output to have its own Output Enable pin, which would dramatically increase pin count and package cost. Common sources in a system that can be used to drive the 87973I-147 serial interface are FPGA’s and ASICs.

PROTOCOL

The Serial interface consists of two pins, FRZ_Data (Freeze Data) and FRZ_CLK (Freeze Clock). Each of the outputs which can be frozen has its own freeze enable bit in the 12 bit shift register. The sequence is started by supplying a logic “0” start bit followed by 12NRZ freeze enable bits. The period of each FRZ_DATA bit equals the period of the FRZ_CLK signal. The FRZ_DATA serial transmission should be timed so the 87973I-147 can sample each FRZ_DATA bit with the rising edge of the FRZ_CLK signal. To place an output in the freeze state, a logic “0” must be written to the respective freeze enable bit in the shift register. To unfreeze an output, a logic “1” must be written to the respective freeze enable bit. Outputs will not become enabled/disabled until all 12 data bits are shifted into the shift register. When all 12 data bits are shifted in the register, the next rising edge of FRZ_CLK will enable or disable the outputs. If the bit that is following the 12th bit in the register is a logic “0”, it is used for the start bit of the next cycle; otherwise, the device will wait and won’t start the next cycle until it sees a logic “0” bit. Freezing and unfreezing of the output clock is synchronous (see the timing diagram below). When going into a frozen state, the output clock will go LOW at the time it would normally go LOW, and the freeze logic will keep the output low until unfrozen. Likewise, when coming out of the frozen state, the output will go HIGH only when it would normally go HIGH. This logic, therefore, prevents runt pulses when going into and out of the frozen state.

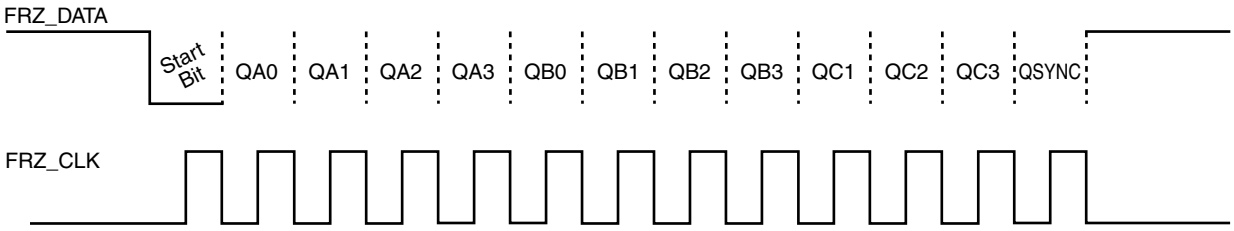


Figure 5A. Freeze Data Input Protocol

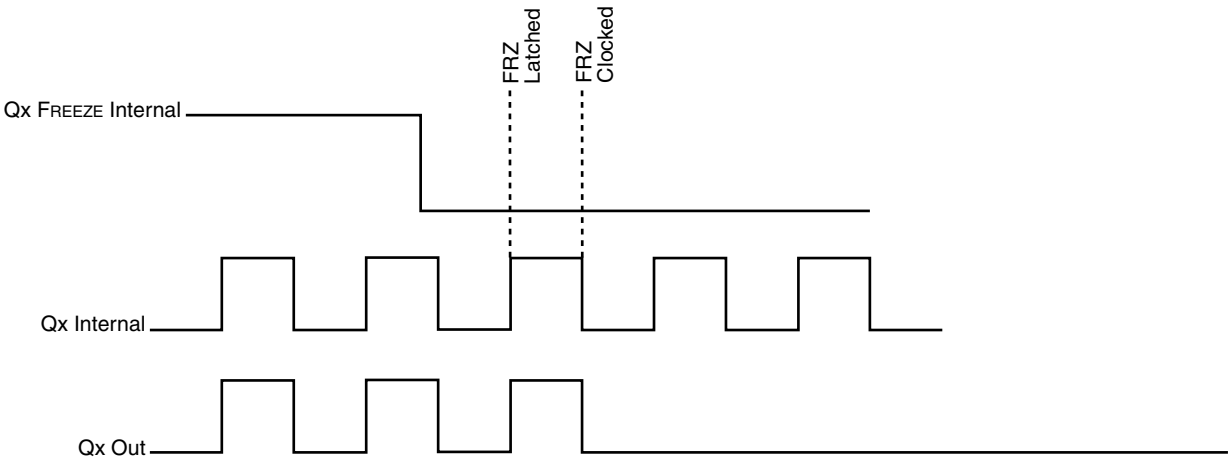


Figure 5. Output Disable Timing Diagram

Schmatic Example

Figure 6 shows a schematic example of using 87973I-147. This example shows general design of input, output termination, logic control input pull up/down and power supply filtering. In this example, the clock input is driven by an LVCMOS driver.

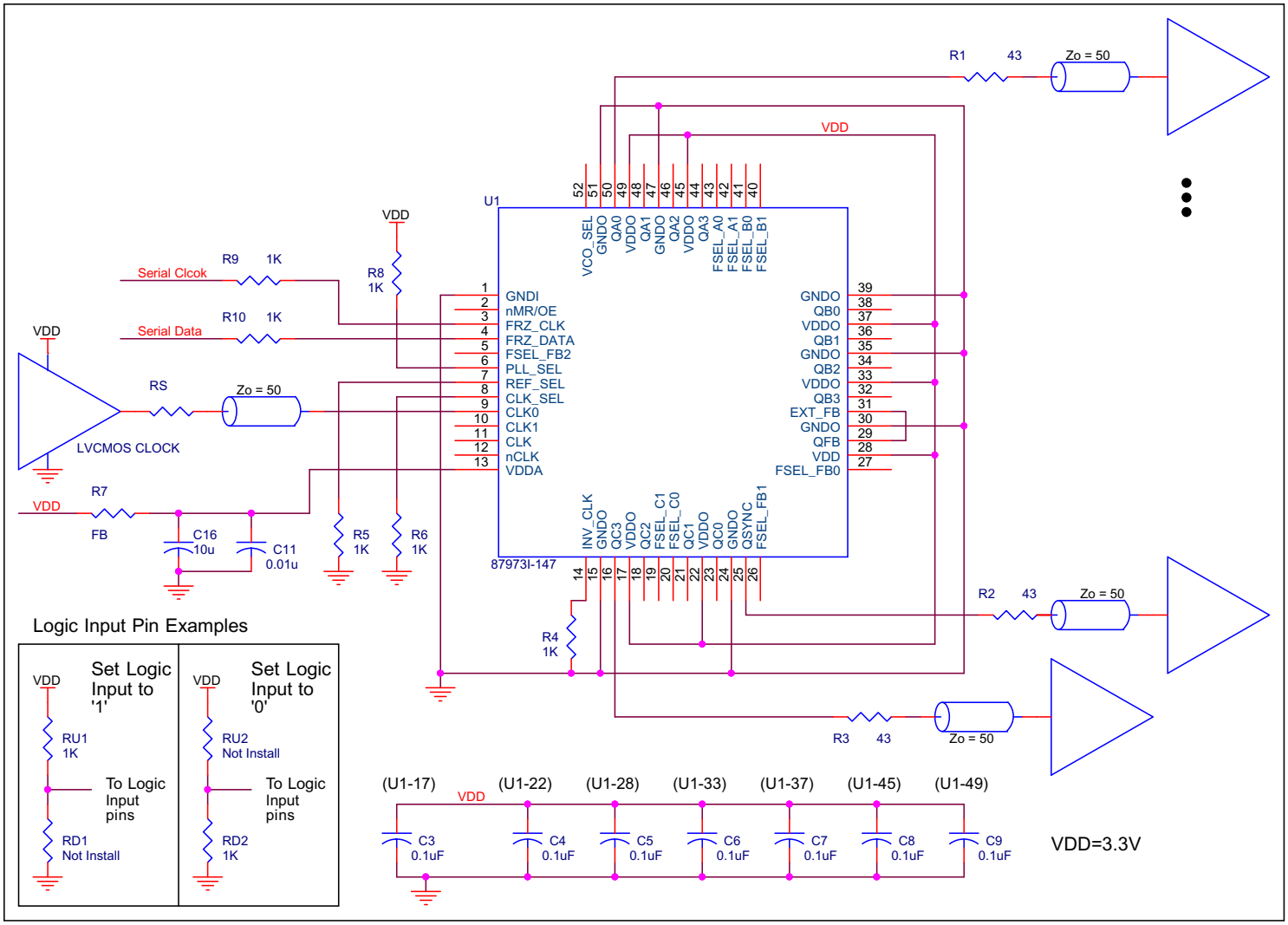


Figure 6. 87973I-147 Schematic Layout

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 52 Lead LQFP

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	58.0°C/W	47.1°C/W	42.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	42.3°C/W	36.4°C/W	34.0°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

Transistor Count

The transistor count for 87973I-147: 8364

Pin Compatible with MPC973

Package Outline and Package Dimensions

Package Outline - Y Suffix for 52 Lead LQFP

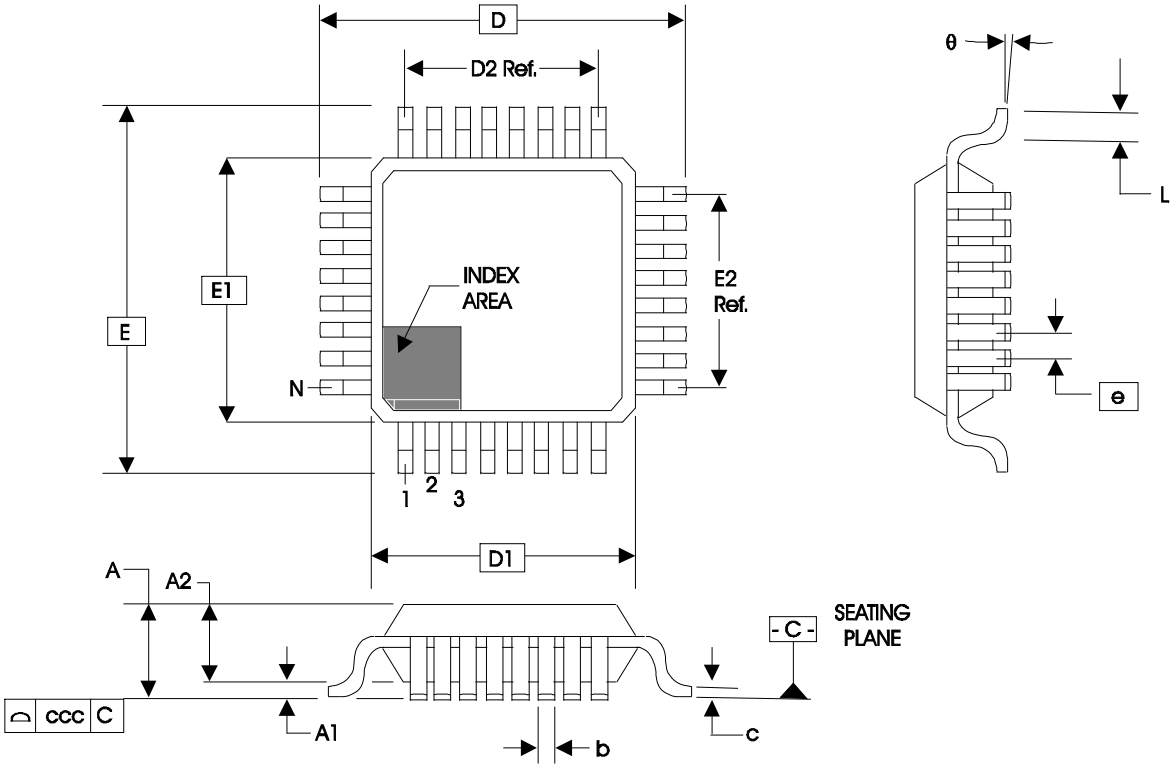


Table 8. Package Dimensions for 52 Lead LQFP

JEDEC Variation: BCC All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		52	
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.22		0.38
c	0.09		0.20
D & E		12.00 Basic	
D1 & E1		10.00 Basic	
D2 & E2		7.80 Ref.	
e		0.65 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87973DYI-147LF	ICS87973DI147L	“Lead-Free” 52 Lead LQFP	Tray	-40°C to 85°C
87973DYI-147LFT	ICS87973DI147L	“Lead-Free” 52 Lead LQFP	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B		2 -3	Updated Block Diagrams - added “PU/PD” to nCLK clock input.	7/27/15
	T1	4	Pin Description Table - pin number 12, nCLK - added “Pullup/Pulldown” in *Type column.*	
	T6	8	AC Characteristics Table - f_{OUT} Frequency - added ÷10 and ÷12 rows. ÷2 row, corrected typo: maximum value from 150MHz to 250MHz.	
		11	*Power Supply Filtering Technique* - corrected Figure 2 drawing. Updated *Wiring the Differential Inputs to Accept Single-ended Levels* application note.	
		14	Schematic Example - corrected Schematic Layout drawing. Deleted “ICS” prefix in part number throughout the datasheet. Updated headers/footers.	
B	T9	17	Ordering Information - removed quantity from tape and reel. Deleted LF note below table. Product Discontinuation Notice - Last time buy expires May 6, 2017. PDN CQ-16-01. Updated header and footer.	6/28/16

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

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