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# FCD7N60

## N-Channel SuperFET® MOSFET 600 V, 7 A, 600 mΩ

### Features

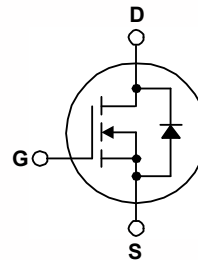
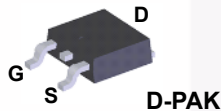
- 650 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 530\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 23\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 60\text{ pF}$ )
- 100% Avalanche Tested
- RoHS Compliant

### Application

- LCD / LED TV and Monitor
- Lighting
- Solar Inverter
- AC-DC Power Supply

### Description

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance,  $dv/dt$  rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCD7N60TM / FCD7N60TM_WS	Unit
$V_{DSS}$	Drain to Source Voltage	600	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	7
		- Continuous ( $T_C = 100^\circ\text{C}$ )	4.4
$I_{DM}$	Drain Current	- Pulsed (Note 1)	21
$V_{GSS}$	Gate to Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	230	mJ
$I_{AR}$	Avalanche Current (Note 1)	7	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	8.3	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	20	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	83
		- Derate Above $25^\circ\text{C}$	0.67
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FCD7N60TM / FCD7N60TM_WS	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	83	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCD7N60TM	FCD7N60	D-PAK	Tape and Reel	330 mm	16 mm	2500 units
FCD7N60TM_WS	FCD7N60	D-PAK	Tape and Reel	330 mm	16 mm	2500 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 $\mu$ A, T <sub>C</sub> = 25 $^\circ$ C	600	-	-	V
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 $\mu$ A, T <sub>C</sub> = 150 $^\circ$ C	-	650	-	V
$\Delta$ BV <sub>DSS</sub> / $\Delta$ T <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 $\mu$ A, Referenced to 25 $^\circ$ C	-	0.6	-	V/ $^\circ$ C
BV <sub>DS</sub>	Drain to Source Avalanche Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 7.0 A	-	700	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	-	-	1	$\mu$ A
		V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125 $^\circ$ C	-	-	10	
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = $\pm$ 30 V, V <sub>DS</sub> = 0 V	-	-	$\pm$ 100	nA

### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 $\mu$ A	3.0	-	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.5 A	-	0.53	0.6	$\Omega$
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 3.5 A	-	6	-	S

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	710	920	pF
C <sub>oss</sub>	Output Capacitance		-	380	500	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	34	-	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	22	29	pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	-	60	-	pF

### Switching Characteristics

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 7.0 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 25 $\Omega$	-	35	80	ns
t <sub>r</sub>	Turn-On Rise Time		-	55	120	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	75	160	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4)	-	32	75
Q <sub>g(tot)</sub>	Total Gate Charge at 10V	V <sub>DS</sub> = 480 V, I <sub>D</sub> = 7.0 A, V <sub>GS</sub> = 10 V	-	23	30	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		-	4.2	5.5	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		(Note 4)	-	11.5	-

### Drain-Source Diode Characteristics

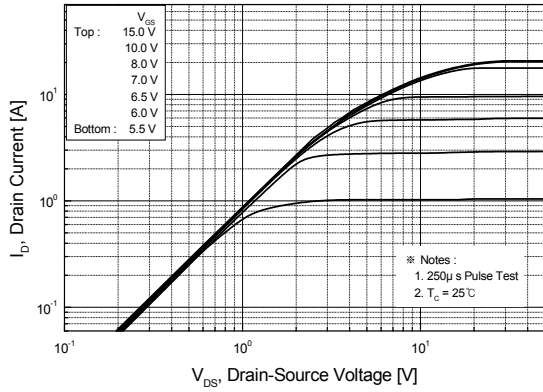
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current	-	-	7	A	
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current	-	-	21	A	
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 7.0 A	-	-	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 7.0 A, di <sub>F</sub> /dt = 100 A/ $\mu$ s	-	360	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	4.5	-	$\mu$ C

#### Notes:

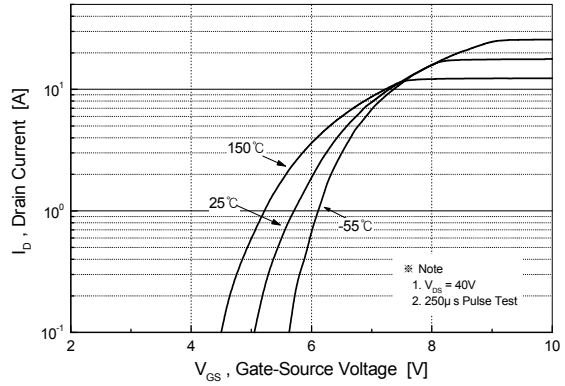
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I<sub>AS</sub> = 3.5 A, V<sub>DD</sub> = 50 V, R<sub>G</sub> = 25  $\Omega$ , starting T<sub>J</sub> = 25 $^\circ$ C.
3. I<sub>SD</sub>  $\leq$  7 A, di<sub>F</sub>/dt  $\leq$  200 A/ $\mu$ s, V<sub>DD</sub>  $\leq$  BV<sub>DSS</sub>, starting T<sub>J</sub> = 25 $^\circ$ C.
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

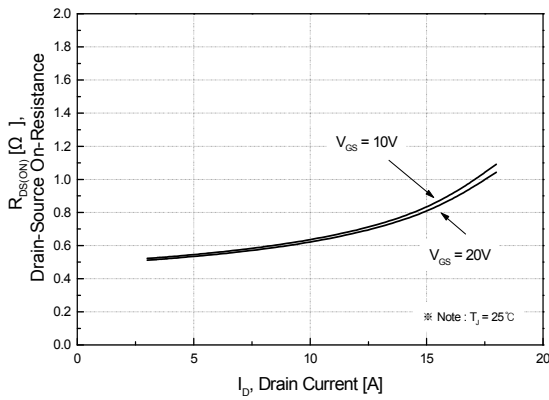
**Figure 1. On-Region Characteristics**



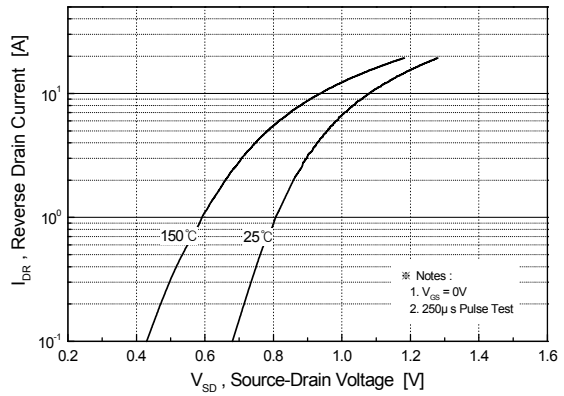
**Figure 2. Transfer Characteristics**



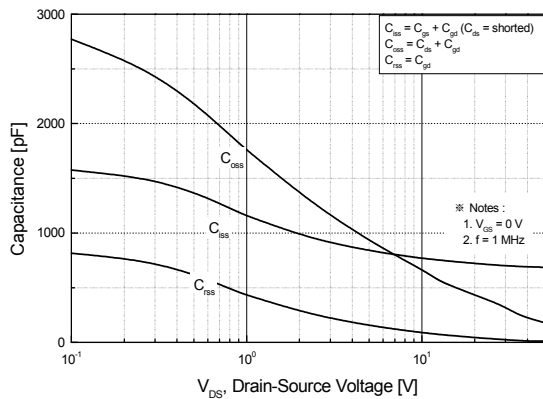
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



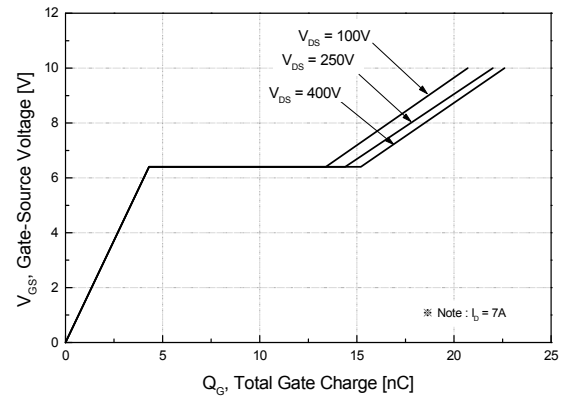
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**



**Figure 6. Gate Charge Characteristics**



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

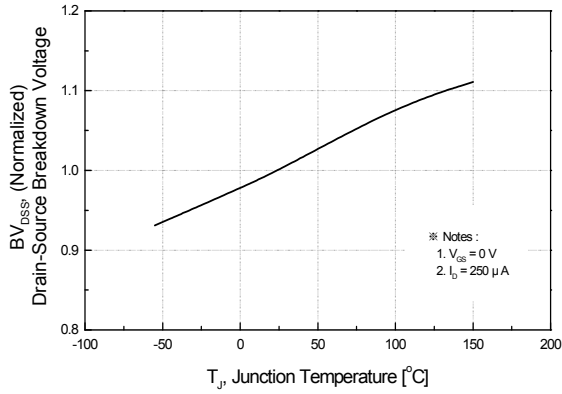


Figure 8. On-Resistance Variation vs. Temperature

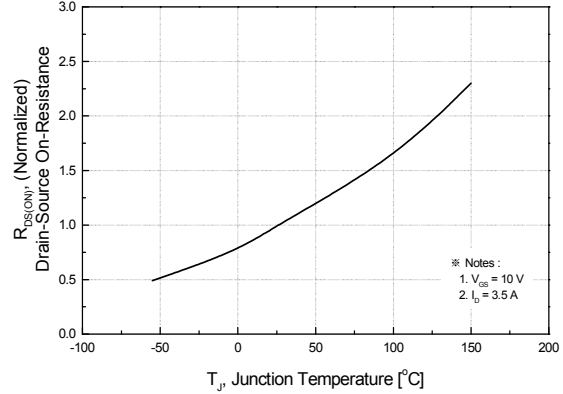


Figure 9. Maximum Safe Operating Area

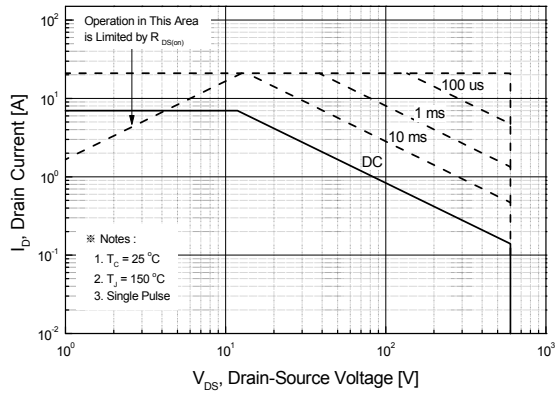


Figure 10. Maximum Drain Current vs. Case Temperature

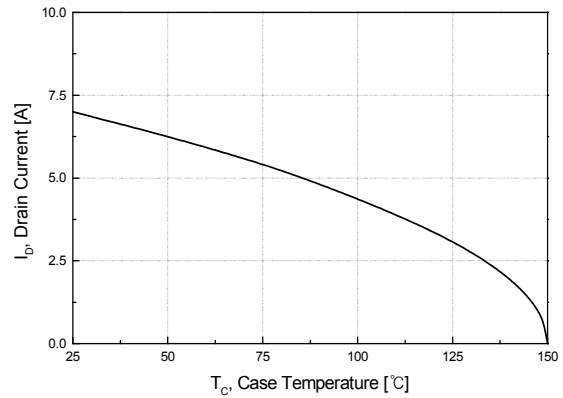
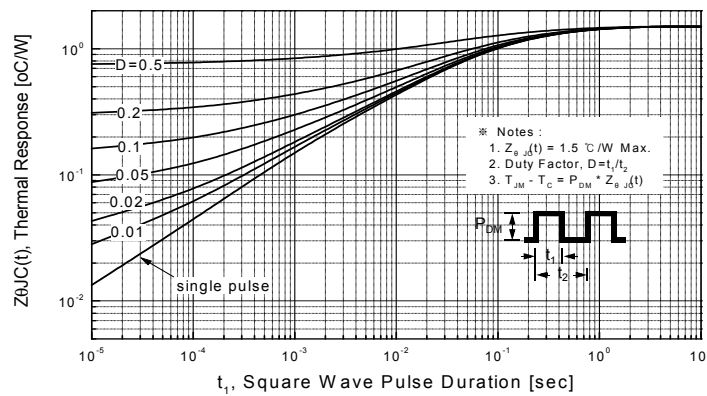


Figure 11. Transient Thermal Response Curve



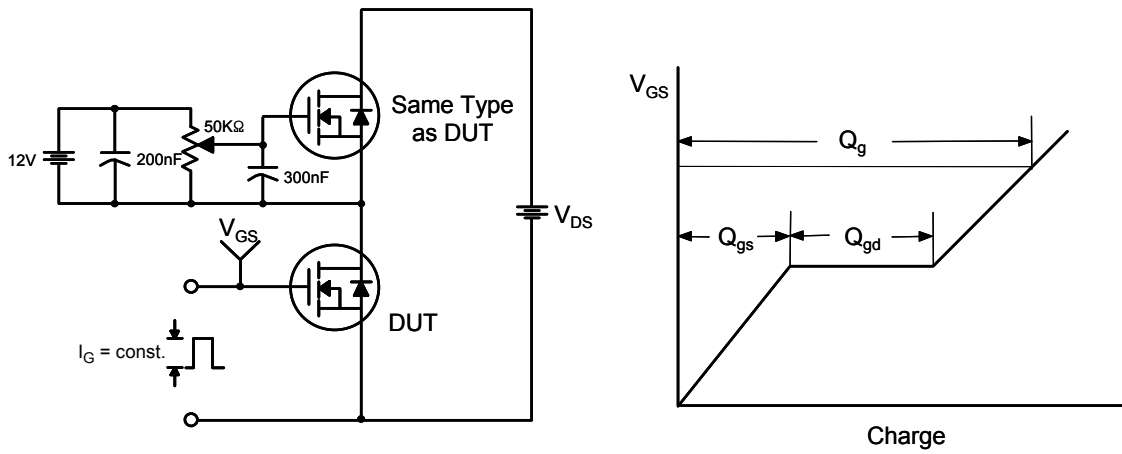


Figure 12. Gate Charge Test Circuit & Waveform

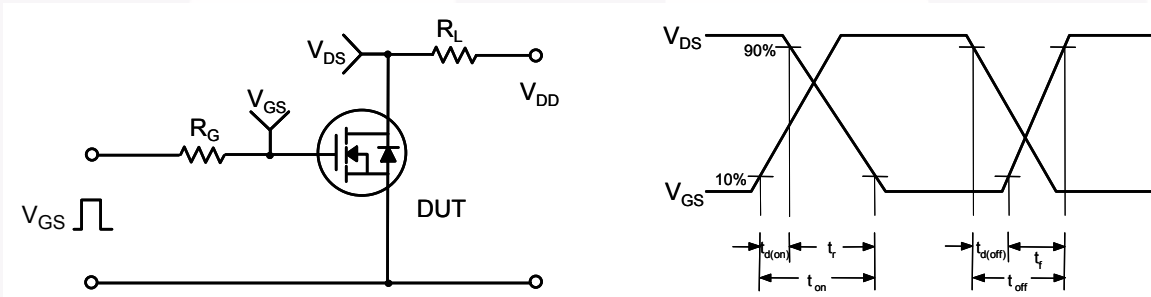


Figure 13. Resistive Switching Test Circuit & Waveforms

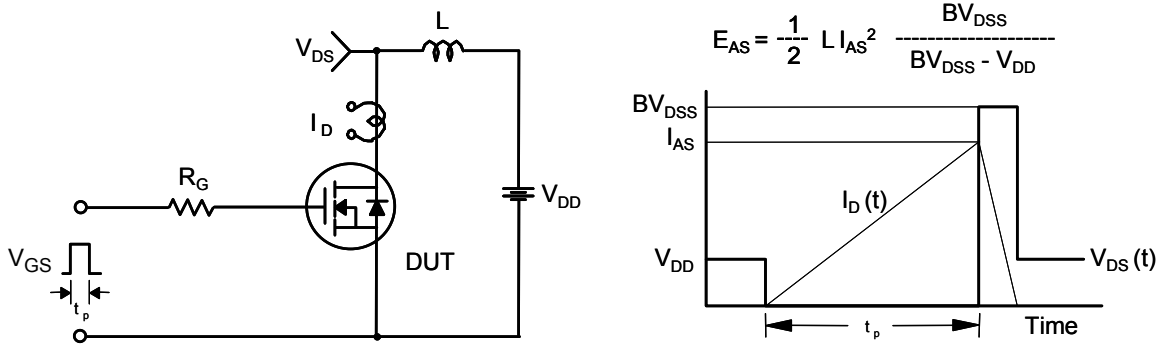


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

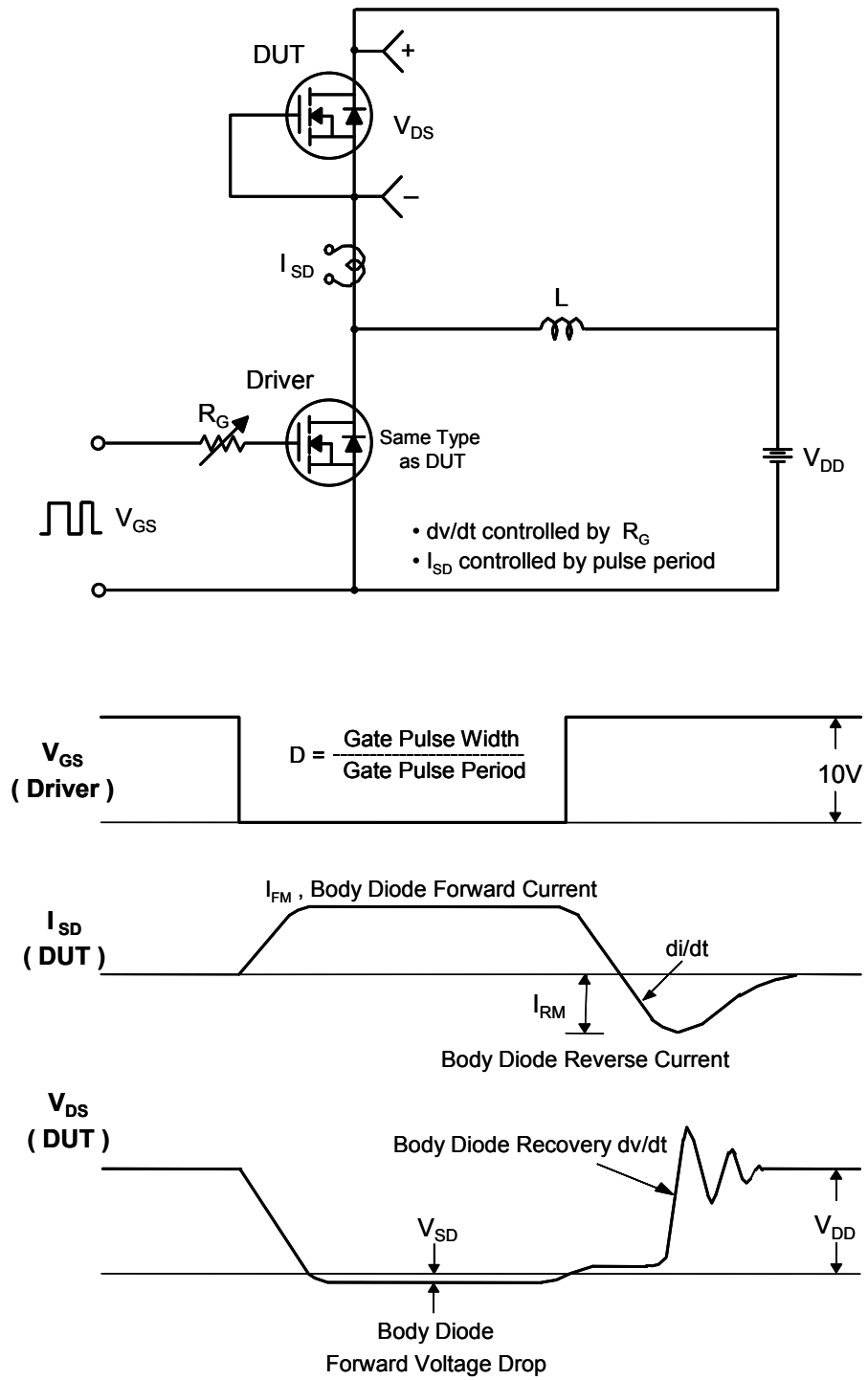
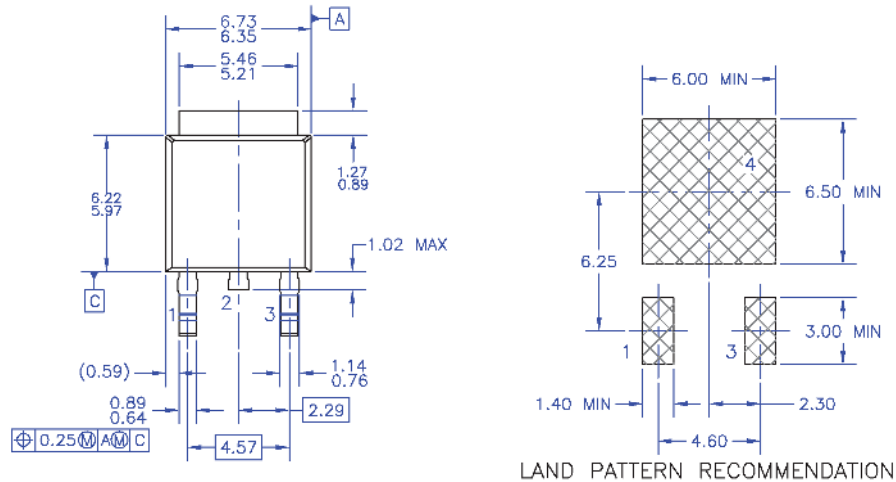


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
  - F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
  - G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
  - H) DRAWING NUMBER AND REVISION: MKT-T0252A03REV8

**Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB**

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