SAMA5D2-PTC-EK

SAMA5D2-PTC-EK User's Guide

Scope

This user's guide describes how to use the SAMA5D2 PTC Evaluation Kit (SAMA5D2-PTC-EK).

The SAMA5D2-PTC-EK is used to evaluate the capabilities of the Peripheral Touch Controller (PTC) designed for the SAMA5D2 series of embedded MPUs. Refer to the Configuration Summary table in the SAMA5D2 Series Datasheet for the list of MPUs featuring PTC.

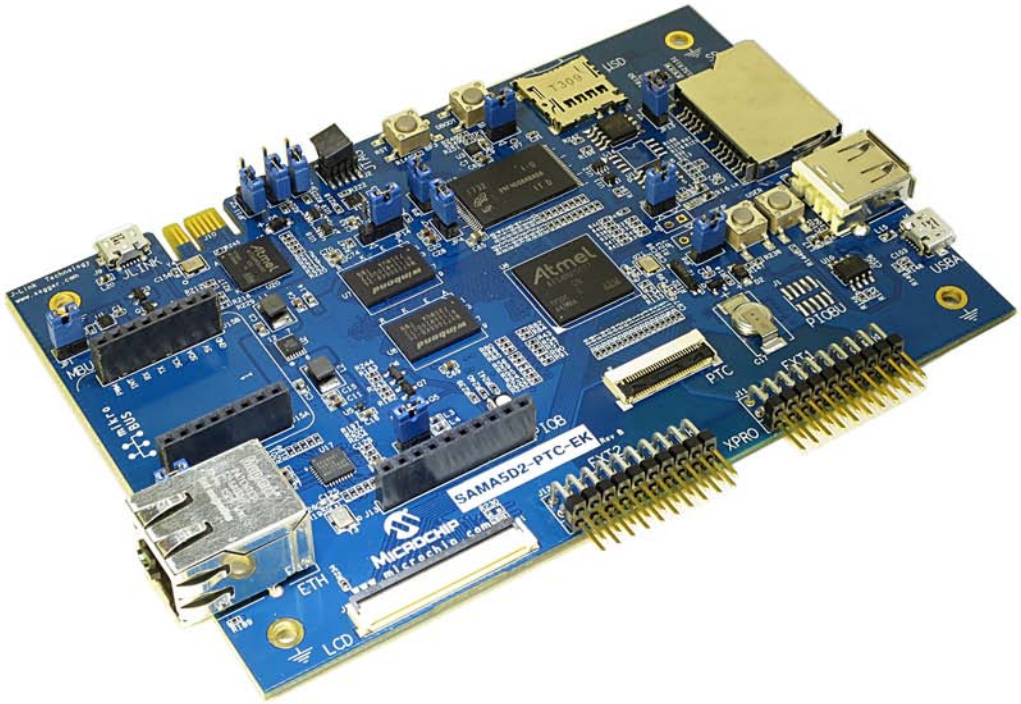


Table of Contents

1. Introduction

1.1 Document Layout

The document is organized as follows:

- Chapter 1. "Introduction"
- Chapter 2. "Product Overview" – Important information about the SAMA5D2-PTC-EK board
- Chapter 3. "Board Components" – Specifications of the SAMA5D2-PTC-EK and high-level description of the major components and interfaces
- Chapter 4. "Installation and Operation" – Instructions on how to get started with the SAMA5D2-PTC-EK
- Appendix A. "Schematics and Layouts" – SAMA5D2-PTC-EK schematics and layout diagrams

1.2 Recommended Reading

The following Microchip document is available and recommended as a supplemental reference resource:

- SAMA5D2 Series Datasheet. Lit. Number DS60001476

2. Product Overview

2.1 SAMA5D2-PTC-EK Features

The SAMA5D2-PTC-EK follows the Microchip MPU strategy for low cost evaluation kits with maximum reuse capability, and is built on the SAMA5D2 Xplained Ultra (XULT) hardware and software ecosystem. This board is mainly dedicated to evaluating the Peripheral Touch Controller capabilities.

Table 2-1. SAMA5D2-PTC-EK Features

Characteristics	Specifications	Components
Processor	SAMA5D27-CU (289-ball BGA) 14x14mm body, 0.8mm pitch	–
Clock speed	MPU: 24 MHz, 32.768 KHz PHY: Crystal 25 MHz	–
Memory	Two 16-bit, 2-Gbit DDR2 One 4-Gbit Nand Flash One QSPI Flash One Serial Data Flash (optional) One EEPROM	Winbond W972GG6KB-25 Micron MT29F4G08 Microchip SST26VF064B Microchip SST26VF032B Microchip 24AA02E48
Display	One LCD interface connector	RGB, 18 bits
SD/MMC	One standard SD card interface One microSD card interface	With 3.3V/1.8V power switch –
USB	One USB host type A One USB device type MicroAB One USB HSIC	With 5V power switch – Connector not mounted
Ethernet	One ETH PHY	Micrel KSZ8081RN
Debug Port	One JLINK-OB/ JLINK-CDC One JTAG interface	Embedded JLINK-OB and JLINK-CDC (ATSAM3U4C TFBGA100)
Board Monitor	One RGB (Red, Green, Blue) LED Four push button switches	– DisableBoot, Reset, WakeUp, User Free
Expansion	One set of XPRO WINGS connectors One ITO FLEX connector One Port B connector One PIOBU connector One mikroBUS connector	Dedicated PTC QTouch Optional Optional Optional –

Characteristics	Specifications	Components
Board Supply	From USB A and USB JLINK-OB	5VDC
Backup Power Supply	SuperCap	ELNA DSK-3R3H204T614-H2L

2.2 SAMA5D2-PTC-EK Content

The SAMA5D2-PTC-EK evaluation kit includes the following:

- The SAMA5D2-PTC-EK board
- A USB cable

2.3 Evaluation Kit Specifications

Table 2-2. Evaluation Kit Specifications

Characteristic	Specification
Board	SAMA5D2-PTC-EK
Board supply voltage	USB-powered
Temperature	Operating: 0°C to +70°C Storage: –40°C to +85°C
Relative humidity	0 to 90% (non-condensing)
Main board dimensions	135 × 90 × 20 mm
RoHS status	Compliant
Board identification	SAMA5D2 Peripheral Touch Controller Evaluation Kit

2.4 Power Sources

Several options are available to power up the SAMA5D2-PTC-EK board:

- USB powering through the USB Micro-AB connector (J4 - default configuration)
- Powering through the USB Micro-AB connector on the JLink-OB Embedded Debugger interface (J9)

Table 2-3. Electrical Characteristics

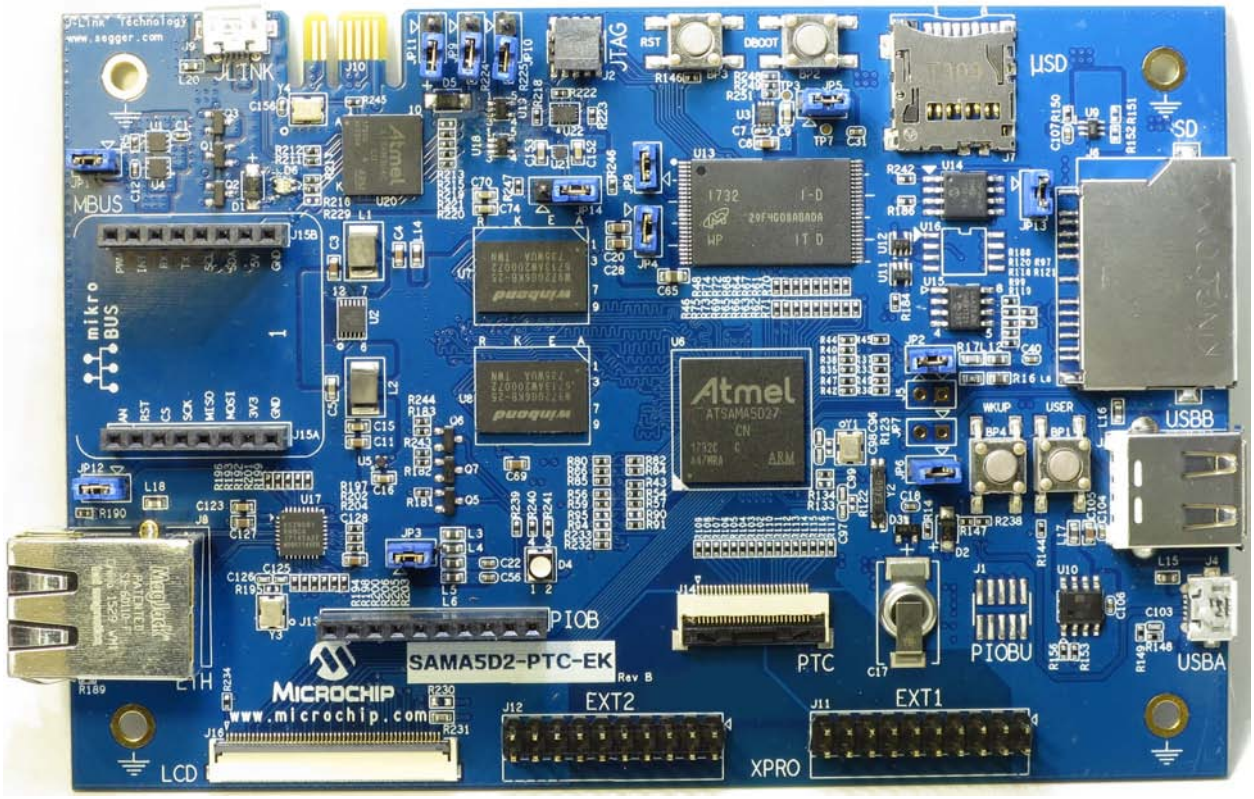
Electrical Parameter	Value
Input voltage	5VCC
Maximum input voltage	6VCC
Maximum 3.3VDC current available	1.2A
I/O voltage	3.3V only

3. Board Components

This section covers the specifications of the SAMA5D2-PTC-EK and provides a high-level description of the board's major components and interfaces. This document is not intended to provide a detailed documentation about the processor or about any other component used on the board. It is expected that the user will refer to the appropriate documents of these devices to access detailed information.

3.1 Board Overview

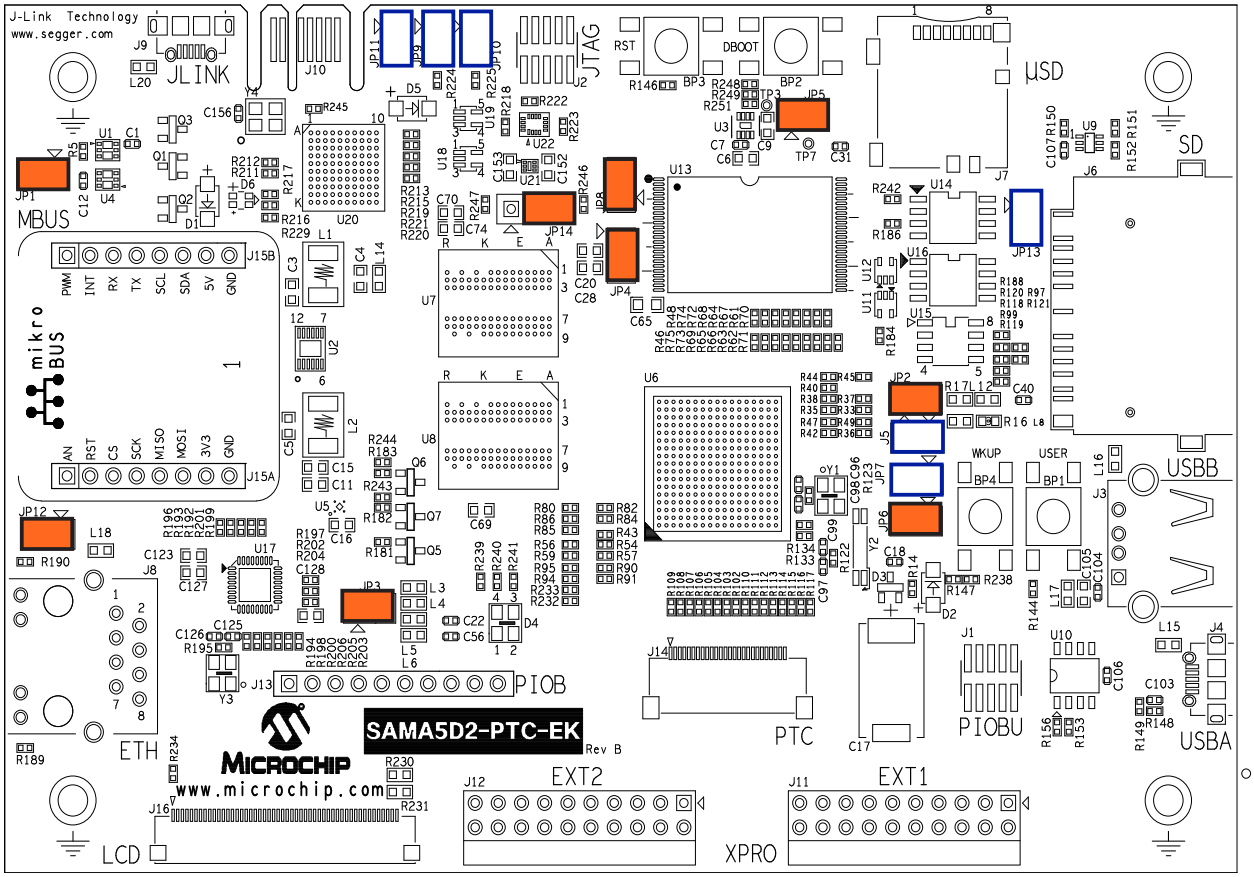
The fully-featured SAMA5D2-PTC-EK board integrates multiple peripherals and interface connectors, as shown in the figure below.



3.1.1 Default Jumper Settings

The figure below shows the default jumper settings. Jumpers in red are configuration items and current measurement points. Jumpers in blue are not populated.

Figure 3-1. Default Jumper Settings



The following table describes the functionality of the jumpers.

Table 3-1. SAMA5D2-PTC-EK Jumper Settings

Jumper	Default	Function
JP1	Closed	VDD_MAIN_5V current measurement
JP2	Closed	VDDOSC, VDDUTMII, VDDANA, VDDAUDIOPLL current measurement
JP3	Closed	VDDISC + VDDIOP0/1/2 current measurement
JP4	Closed	VDDIODDR_MPU current measurement
JP5	Closed	VDDCORE current measurement
JP6	Closed	VDDBU current measurement
JP7	Open	PIOBU1, PIOBU7
JP8	Closed	Disables NAND_CS (open=disable)
JP9	Open	Enables JTAG-CDC (closed=disable)
JP10	Open	Enables JTAG-OB (closed=disable)
JP11	Open	Erases SAM3U Flash Code (closed = erase)

Jumper	Default	Function
		WARNING **Warning:** This jumper is reserved for factory configuration and should never be used by the end user.
JP12	Closed	Powers mikroBUS extension (3.3V)
JP13	Open	Disables QSPI
JP14	1-2	Enables 3.3V JLINK-OB, connected to shutdown circuitry
	2-3	Enables 3.3V JLINK-OB, always ON

3.1.2 Connectors on Board

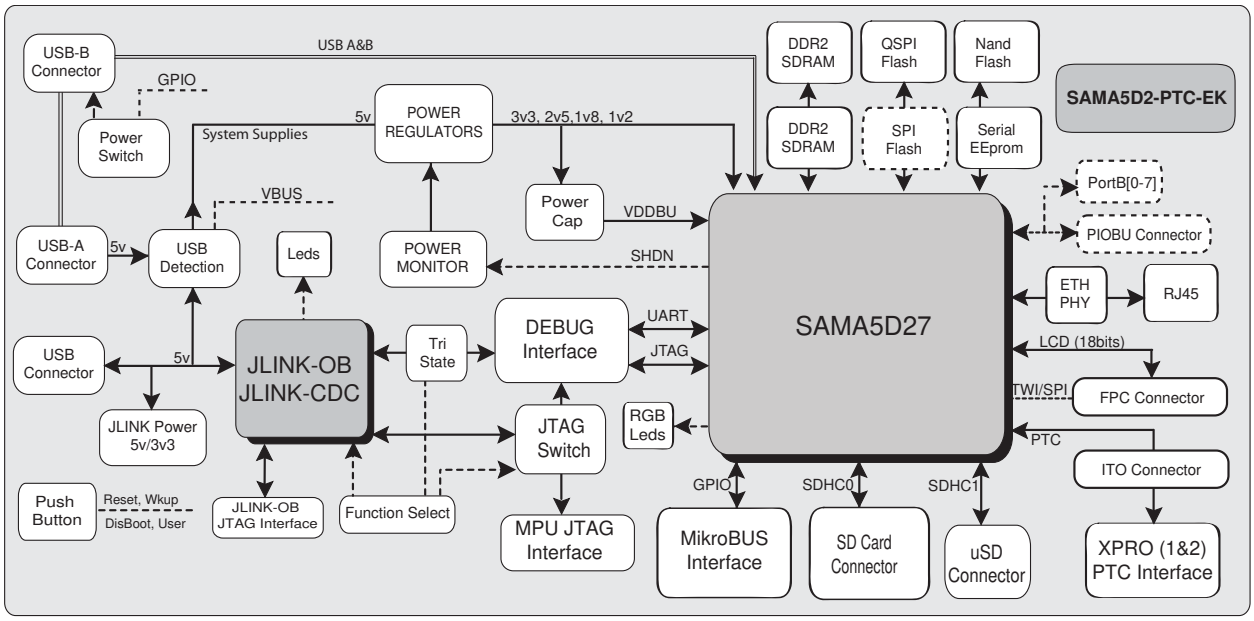
The following table describes the interface connectors on the SAMA5D2-PTC-EK.

Table 3-2. SAMA5D2-PTC-EK Board Interface Connectors

Connector	Interfaces to
J1	PIOBU, tamper and analog comparator connector (not populated)
J2	JTAG, 10-pin IDC connector
J3	USB Host B. Supports USB host using a type A connector
J4	USB A Device. Supports USB device using a type Micro-AB connector
J5	USB-C HSIC header (not populated)
J6	Standard SDMMC connector
J7	microSD connector
J8	Ethernet 10/100 RJ45
J9	USB-A MicroAB, JLink-OB port
J10	PCB connector for factory-programming the JLINK-OB/SAM3U
J11, J12	Xplained Pro expansion connectors (PTC-dedicated add-on boards)
J13	PIOs PortB connector
J14	ITO connector
J15 A&B	mikroBUS connector
J16	Expansion TFT LCD connector for display module

3.2 Function Blocks

Figure 3-2. SAMA5D2-PTC-EK Block Diagram



3.2.1 Processor

The SAMA5D2 Series is a high-performance, power-efficient embedded MPU based on the ARM® Cortex®-A5 processor.

Please refer to the SAMA5D2 Series datasheet for more information.

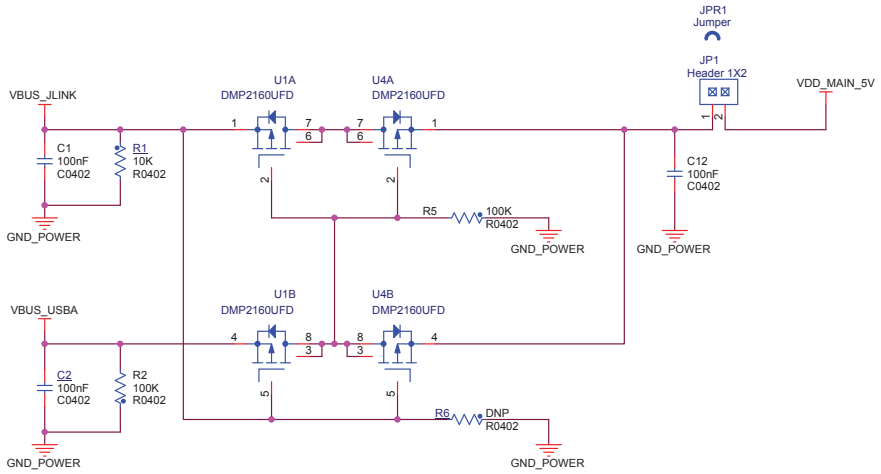
3.2.2 Power Supply Topology and Power Distribution

3.2.2.1 Input Power Options

Two options are available to power the SAMA5D2-PTC-EK board. The USB-powered operation is the default configuration and comes from the USB device ports (J4-J9) connected to a PC or a 5VDC supply. Such USB power source is sufficient to supply the board in most applications. It is important to note that when the USB-powered operation is used, the USB port down the way has a limited powering capability. If the USB-B Host port (J3) is required to provide full powering capabilities to the target application, it is recommended to use an external DC supply instead of a USB power source.

The following figure is a schematic of the power options.

Figure 3-3. Input Powering



Note: USB-powered operation eliminates additional wires and batteries. It is the preferred mode of operation for any project that requires only a 5V source at up to 500 mA.

Jumper JP1 is used to perform MAIN_5V current measurements on the SAMA5D2-PTC-EK board.

3.2.2.2 Power Supply Requirements and Restrictions

Detailed information on the device power supplies is provided in tables “SAMA5D2 Power Supplies” and “Power Supply Connections” in the SAMA5D2 Series datasheet.

3.2.2.3 Power-up and Power-down Considerations

Power-up and power-down considerations are described in section “Power Considerations” of the SAMA5D2 Series datasheet.

⚠ CAUTION **Caution:** The power-up and power-down sequences provided in the SAMA5D2 Series datasheet must be respected for reliable operation of the device.

3.2.2.4 Power Management

The board power management uses three types of regulators:

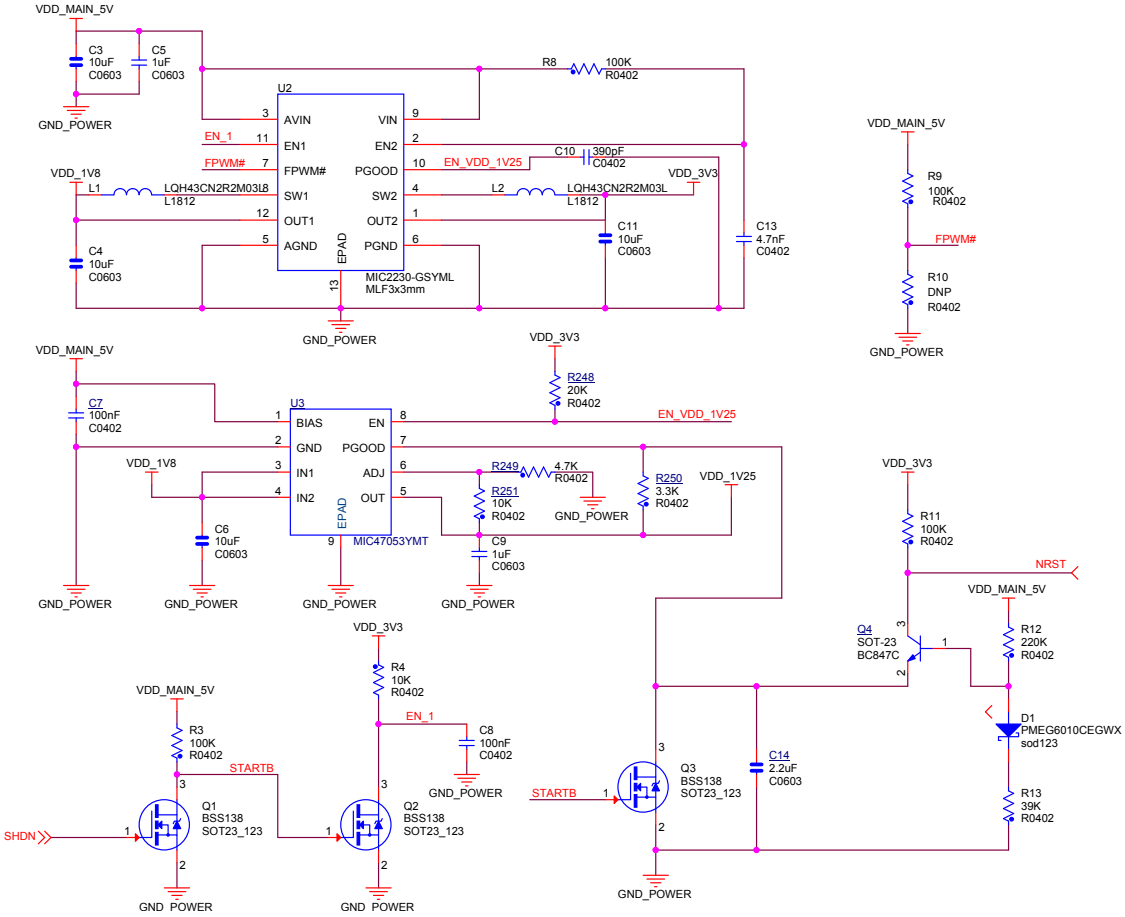
- One dual synchronous step-down DC-DC regulator (U2 MIC2230) generates the 3.3V/800mA and 1.8V/800mA power lines and utilizes a high-efficiency, fixed-frequency (2.5 MHz), current-mode PWM control architecture that requires a minimum number of external components.
- One ultra low-dropout linear regulator (U3 MIC47053) generates the 1.25V/500mA from the 1.8V source.
- One high-performance single 2.5V/150mA is used as a VDDFUSE generator (U5 MIC5366).

The main regulators are enabled through a Field Effect Transistor (FET) scheme. The processor can assert SHDN (a VDDBU-powered I/O) to shut down the regulators to enter Backup mode. All regulators on the board are also shut down by the action of the SHDN signal.

A 3.3V battery (supercap) is implemented to permanently maintain VDDBU voltage (note: jumper JP6 must be in place). The board can be woken up by action on the PB4 button, which drives the WKUP signal (also a VDDBU-powered I/O).

The figure below shows the power management scheme.

Figure 3-4. Board Power Management



3.2.2.5 Supply Group Configuration

The main regulators provide all power supplies required by the SAMA5D2 device:

- 1.25V VDDCORE, VDDPLLA, VDDUTMIC, VDDHSIC
- 1.8V VDDIODDR, VDDSDHC1V8
- 2.5V VDDFUSE
- 3.3V VDDIOP0, VDDIOP1, VDDIOP2, VDDISC
- 3.3V VDDOSC, VDDUTMI, VDDANA, VDDAUDIOPLL
- 3.3V VDDBU

Figure 3-5. Power Lines Distribution

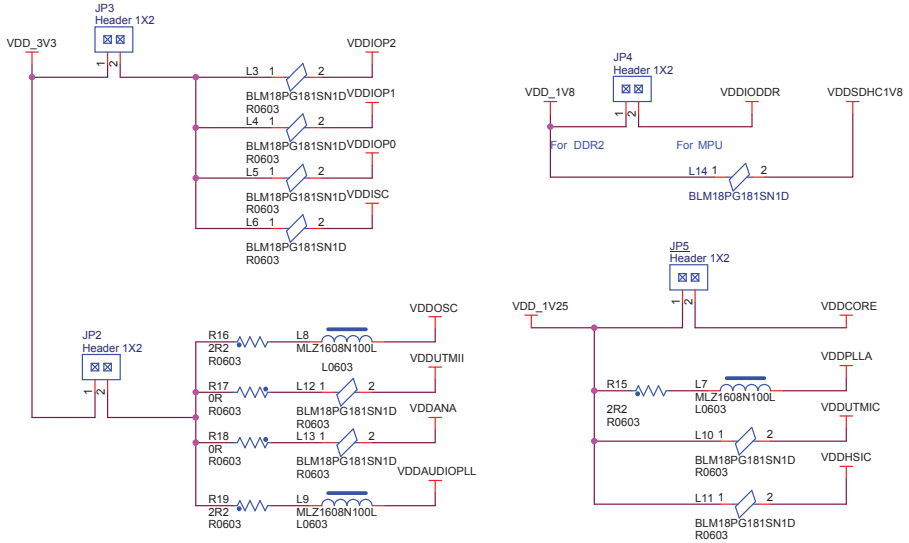
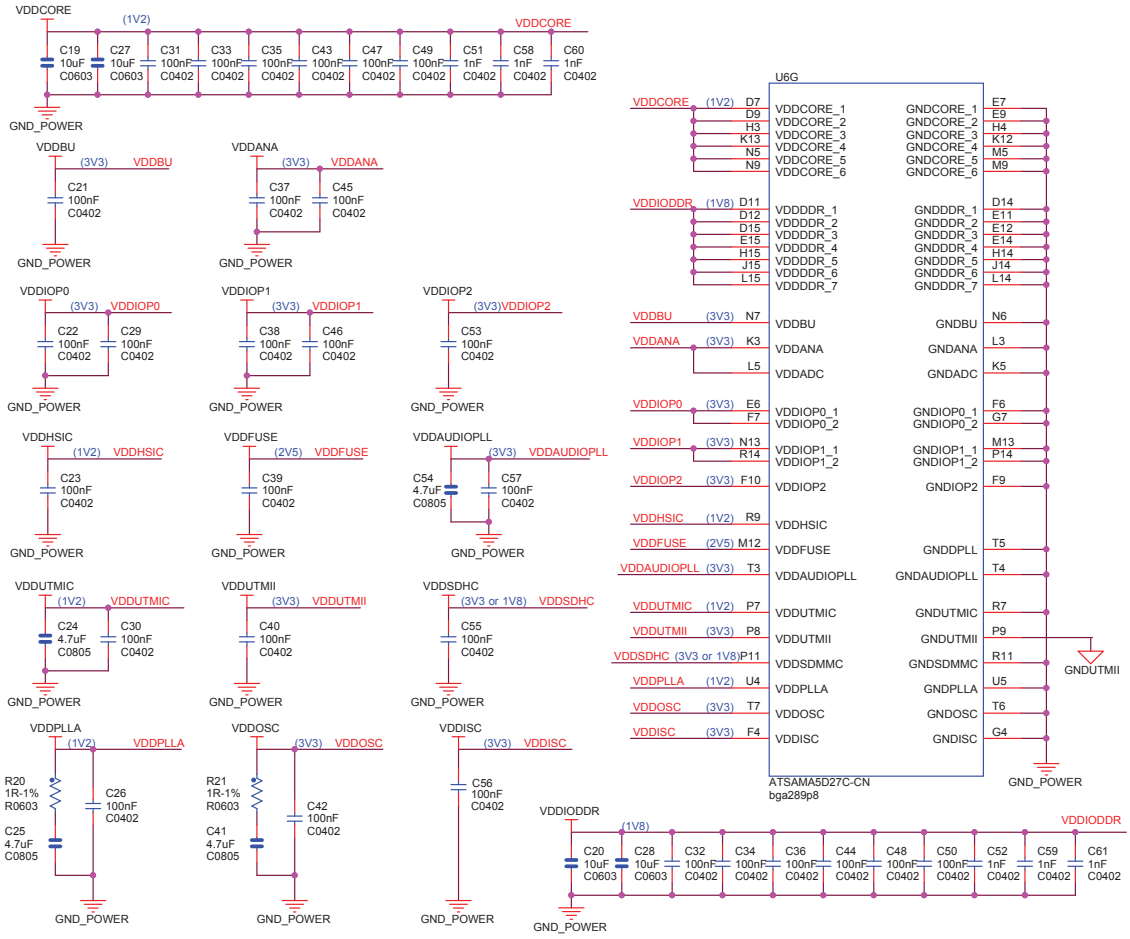


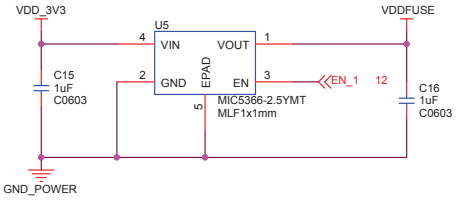
Figure 3-6. Processor Power Lines Supplies



3.2.2.6 VDDFUSE

The SAMA5D2-PTC-EK board embeds a 2.5V regulator for fuse box programming.

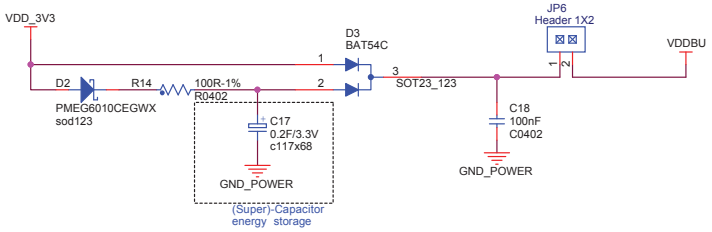
Figure 3-7. VDDFUSE Regulator



3.2.2.7 Backup Power Supply

The SAMA5D2-PTC-EK board requires a power source in order to permanently power the backup part of the SAMA5D2 device (refer to SAMA5D2 Series datasheet). The super capacitor C17 sustains such permanent power to VDDBU when all system power sources are off.

Figure 3-8. VDDBU Powering Options

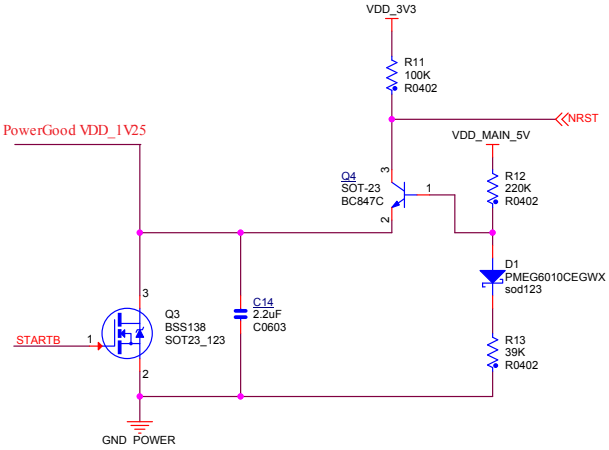


3.2.3 Reset Circuitry

The reset sources for the SAMA5D2-PTC-EK board are:

- Power-on reset from the power management unit,
- Push button reset BP3,
- JTAG or JLINK-OB reset from an in-circuit emulator.

Figure 3-9. Main Reset Control

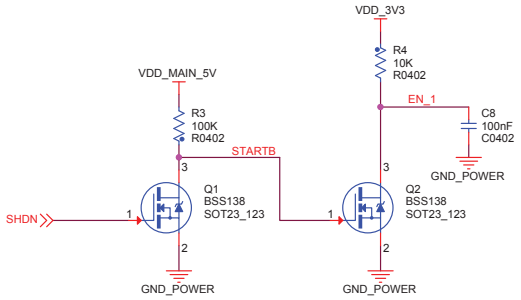


3.2.4 Shutdown Circuitry

The SHDN signal, output of Shutdown Controller (SHDN), drives the shutdown request to the power supply. This output signal is supplied by VDDBU, which is present in Backup mode.

The Shutdown Controller manages the main power supply and is connected to the ENABLE input pin of the DC/DC converter providing the main power supplies of the system.

Figure 3-10. Shutdown Controller

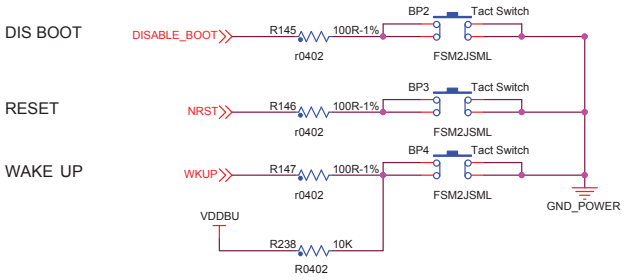


3.2.5 Push Button Switches

The SAMA5D2-PTC-EK features four push buttons:

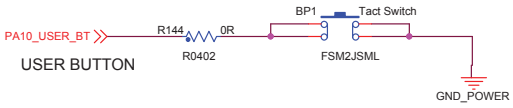
- One board reset push button (BP3). When pressed and released, it causes a power-on reset of the board.
- One wakeup push button (BP4) connected to the SAMA5D2 WKUP pin, used to exit the processor from low-power mode.
- One disable boot push button (BP2) used to devalidate the boot memories (refer to CS Disable).

Figure 3-11. System Push Buttons



- One user push button (BP1) connected to PIO PB10.

Figure 3-12. User Push Button



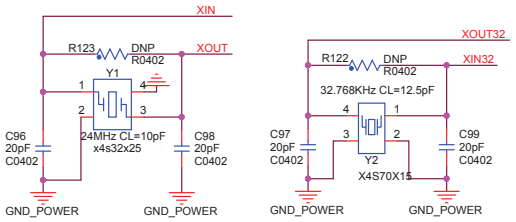
3.2.6 Clock Circuitry

The embedded microcontroller generates its necessary clocks based on two crystal oscillators: one slow clock (SLCK) oscillator running at 32.768 KHz and one main clock oscillator running at 24 MHz.

The SAMA5D2-PTC-EK board includes four clock sources:

- The two clocks mentioned above are alternatives for the SAMA5D2 processor (24 MHz, 32.768 kHz)
- One crystal oscillator for the Ethernet RMII chip (25 MHz)
- One crystal oscillator for the JLink-OB microcontroller (12 MHz)

Figure 3-13. MPU Clock Circuitry



3.2.7 Memory

3.2.7.1 Memory Organization

The SAMA5D2 features a DDR/SDR memory interface and an External Bus Interface (EBI) to enable interfacing to a wide range of external memories and to almost any kind of parallel peripheral.

This section describes the memory devices mounted on the SAMA5D2-PTC-EK board:

- Two DDR2 SDRAMs
- One NAND Flash
- One QSPI Flash
- One SPI Flash (optional)
- One serial EEPROM

Additional memory can be added to the board by:

- Installing an SD or MMC card in the SD/MMC0 or SD/MMC1 slot,
- Using the USB-B port.

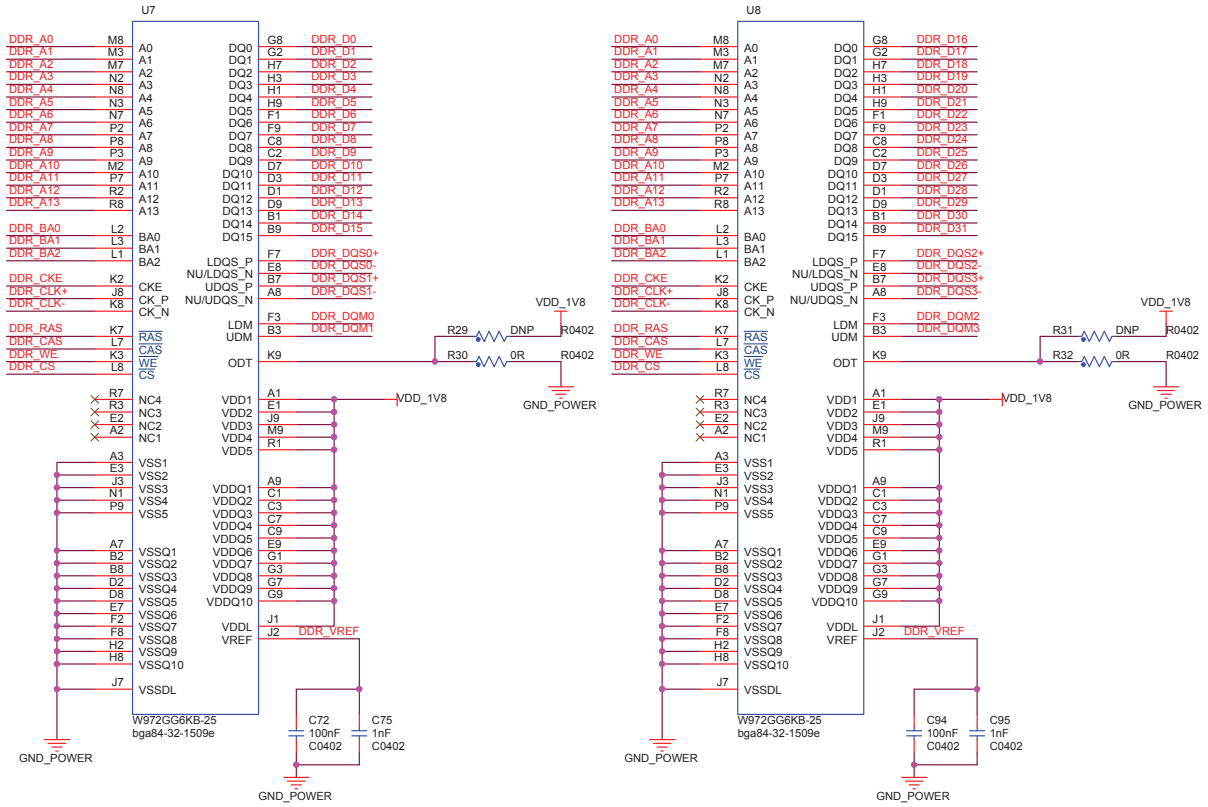
Support is dependent upon driver support in the OS.

3.2.7.2 DDR2/SDRAMs

Two DDR2/SDRAMs (W972GG6KB-25-2 Gbits = 16 Mbits x 16 x 8 banks) are used as main system memory, totalling 4 Gbits of SDRAM on the board. The memory bus is 32 bits wide and operates with a frequency of up to 166 MHz.

The figure below illustrates the implementation for the DDR2 memories.

Figure 3-14. DDR2 SDRAMs



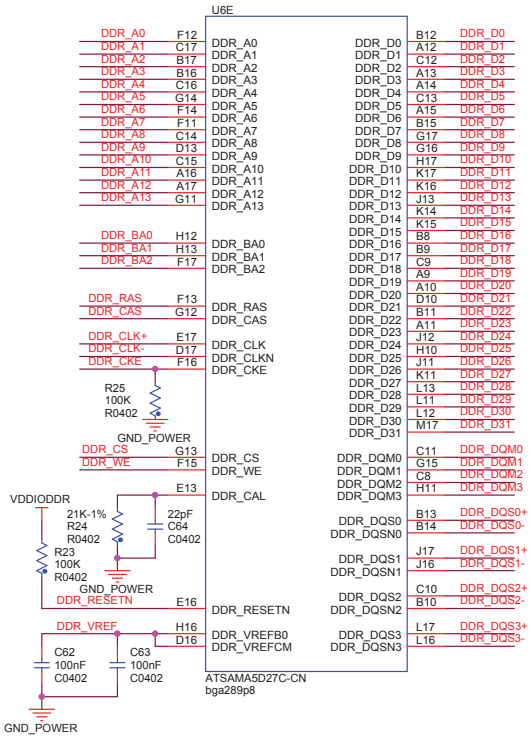
3.2.7.3 DDR_CAL Analog Input

One specific analog input, DDR_CAL, is used to calibrate all DDR I/Os.

Table 3-3. Calibration Cell DDR_CAL Value

Memory	Resistor value
LPDDR2/LPDDR3	24K
DDR3L	23K
DDR3	22K
DDR2/LPDDR1	21K

Figure 3-15. DDR Signals and CAL Analog Input



3.2.7.4 NAND FLASH

The SAMA5D2-PTC-EK has native support for NAND Flash memory through its NAND Flash Controller. The board implements one MT29F4G08ABA 4Gb x 16 NAND Flash connected to chip select three (NCS3) of the microcontroller.

⚠ CAUTION **Caution:** The NAND Flash interface is shared with the SDMMC1 and QSPI interfaces.

The figure below illustrates the NAND Flash memory implementation.

Figure 3-16. NAND Flash

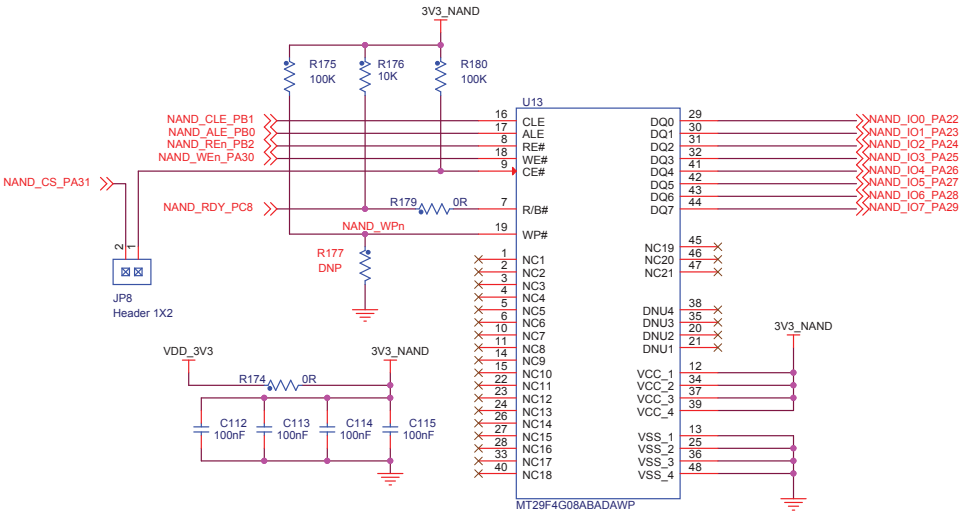


Table 3-4. NAND Flash Signal Descriptions

PIO	Mnemonic	Shared PIO	Signal Description
PA22	NAND_D0	SDMMC1-QSPI	Data 0
PA23	NAND_D1	QSPI	Data 1
PA24	NAND_D2	QSPI	Data 2
PA25	NAND_D3	QSPI	Data 3
PA26	NAND_D4	QSPI	Data 4
PA27	NAND_D5	QSPI	Data 5
PA28	NAND_D6	SDMMC1	Data 6
PA29	NAND_D7	–	Data 7
PA30	NANDWE	SDMMC1	–
PA31	NCS3	–	Chip Select
PB00	NANDALE	–	–
PB01	NANDCLE	–	–
PB02	NANDOE	–	–
PC08	NANRDY	–	–

3.2.7.5 NAND Flash CS Disable

On-board jumper JP8 controls the selection (CS#) of the NAND Flash memory.

3.2.8 Additional Memories

3.2.8.1 Serial Flash

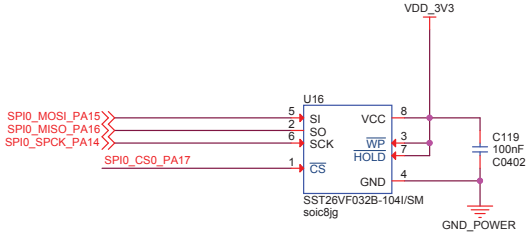
The SAMA5D2 includes two high-speed Serial Peripheral Interface (SPI) controllers. The SPI is a full duplex synchronous bus supporting a single master and multiple slave devices. The SPI bus consists of the following items:

- a serial clock line (generated by the master)
- a data output line from the master
- a data input line to the master
- one or more active low chip select signals (output from the master)

One SPI port is used to interface with the on-board serial Flash.

The following figure illustrates the implementation of an SPI Flash memory.

Figure 3-17. Serial Flash



Note: The serial Flash is optional and not mounted on board.

3.2.8.2 QSPI Serial Flash

The SAMA5D2 provides two Quad Serial Peripheral Interfaces (QSPI).

A QSPI is a synchronous serial data link that provides communication with external devices in Master mode.

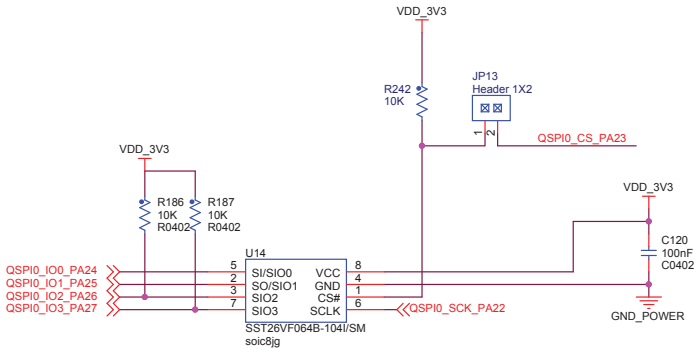
The QSPI can be used in SPI mode to interface with serial peripherals (such as ADCs, DACs, LCD controllers, CAN controllers and sensors), or in Serial Memory mode to interface with serial Flash memories.

The QSPI allows the system to execute code directly from a serial Flash memory (XIP, or Execute In place, technology) without code shadowing to RAM. The serial Flash memory mapping is seen in the system as other memories (ROM, SRAM, DRAM, etc.).

With the support of the Quad SPI protocol, the QSPI allows the system to use high-performance serial Flash memories which are small and inexpensive, instead of larger and more expensive parallel Flash memories.

The figure below illustrates the implementation of a QSPI Flash memory.

Figure 3-18. QSPI Serial Flash



A jumper (JP13) is used to disable the QSPI Flash.

Table 3-5. SPI and QSPI Signal Descriptions

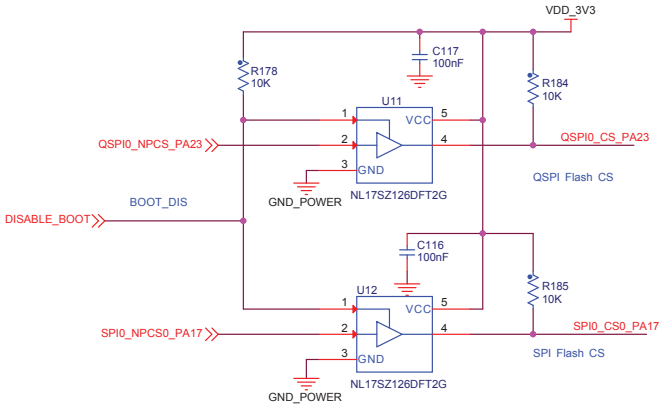
PIO	Mnemonic	PIO Shared	Signal Description
PA14	SPI0_SPCK	_	SPI clock
PA15	SPI0_MOSI	_	Master out - Slave in
PA16	SPI0_MISO	_	Master in - Slave out
PA17	SPI0_NPCS0	_	Chip select
_	_	_	_
PA22	QSPI0_SCK	SDMMC1-Nand Flash	QSPI clock
PA23	QSPI0_CS	Nand Flash	Chip select
PA24	QSPI0_IO0	Nand Flash	Data0
PA25	QSPI0_IO1	Nand Flash	Data1

PIO	Mnemonic	PIO Shared	Signal Description
PA26	QSPI0_IO2	Nand Flash	Data2
PA27	QSPI0_IO3	Nand Flash	Data3

3.2.8.3 CS Disable

On-board push button PB2 controls the selection (CS#) of the bootable memory components (QSPI and serial Flash) using a non-inverting 3-state buffer.

Figure 3-19. CS Disable



The rule of operation is:

- PB2 (DISABLE_BOOT) and PB3 (RESET) pressed = booting from QSPI or optional serial Flash is disabled.

Refer to the SAMA5D2 Series datasheet for more information on standard boot strategies and sequencing.

3.2.8.4 Serial EEPROM with Unique MAC Address

The SAMA5D2-PTC-EK board embeds one Microchip 24AA02E48 I²C serial EEPROM connected on the TWI1 interface.

The TWI interface is I^2C-compatible and similarly uses only two lines, namely serial data (SDA) and serial clock (SCL). According to the standard, the TWI clock rate is limited to 400 kHz in Fast mode and 100 kHz in Normal mode, but configurable baud rate generator permits the output data rate to be adapted to a wide range of core clock frequencies. The TWI is used in Master mode.

The 24AA02E48 features 2048 bits of Serial Electrically-Erasable Programmable Read-Only Memory (EEPROM) organized as 256 words of eight bits each and is accessed via an I^2C-compatible (2-wire) serial interface. In addition, the 24AA02E48 incorporates an easy and inexpensive method to obtain a globally unique MAC or EUI address (EUI-48).

The EUI-48 addresses can be assigned as the actual physical address of a system hardware device or node, or it can be assigned to a software instance. These addresses are factory-programmed by Microchip and guaranteed unique. They are permanently write-protected in an extended memory block located outside the standard 2-Kbit memory array.

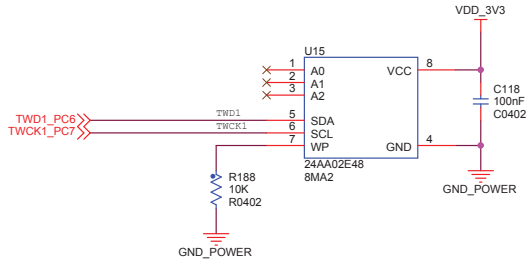
⚠ CAUTION **Caution:** The EEPROM device is used as a “software label” to store board information such as chip type, manufacturer name and production date, using the last two 16-byte blocks in memory. The information contained in these blocks should not be modified.

Table 3-6. EEPROM PIOs Signal Descriptions

PIO	Mnemonic	Shared	Signal Description
PC6	TWD1	XPRO	TWI Data
PC7	TWCL1	XPRO	TWI Clock

The figure below illustrates the implementation for the EEPROM.

Figure 3-20. EEPROM 24AA02E48



3.2.9 Secure Digital Multimedia Card (SDMMC) Interface

The SD (Secure Digital) Card is a non-volatile memory card format used as a mass storage memory in mobile devices.

3.2.9.1 Secure Digital Multimedia Card (SDMMC) Controller

The SAMA5D2-PTC-EK board has two Secure Digital Multimedia Card (SDMMC) interfaces that support the MultiMedia Card (e.MMC) Specification V4.41, the SD Memory Card Specification V3.0, and the SDIO V3.0 specification. It is compliant with the SD Host Controller Standard V3.0 Specification.

- The SDMMC0 interface is connected to a standard SD card interface.
- The SDMMC1 interface is connected to a microSD card interface.

3.2.9.2 SDMMC0 Card Connector

A standard MMC/SD card connector, connected to SDMMC0, is mounted on the top side of the board. The SDMMC0 communication is based on a 12-pin interface (clock, command, data (8) and power lines (2)). A card detection switch is included.

The figure below illustrates the implementation for the SDMMC0 interface.

Figure 3-21. SDMMC0 Standard SD Socket

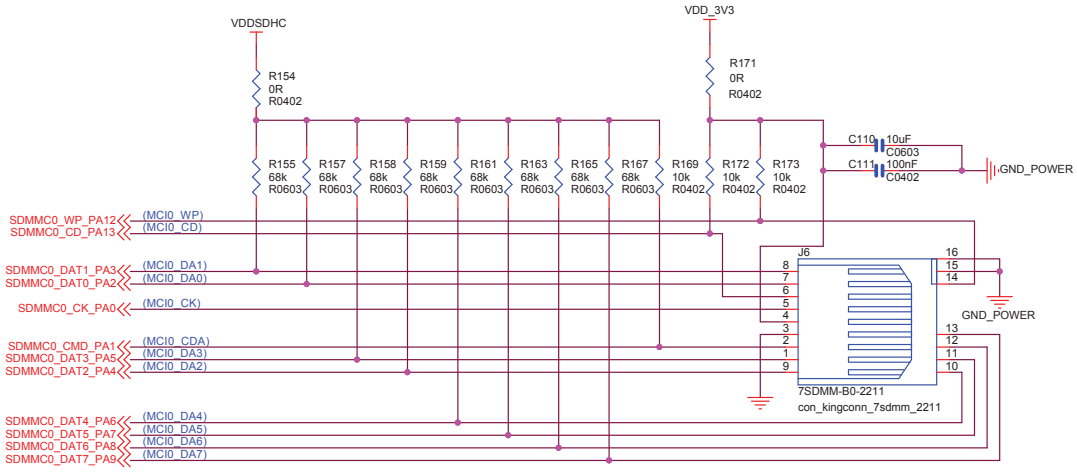
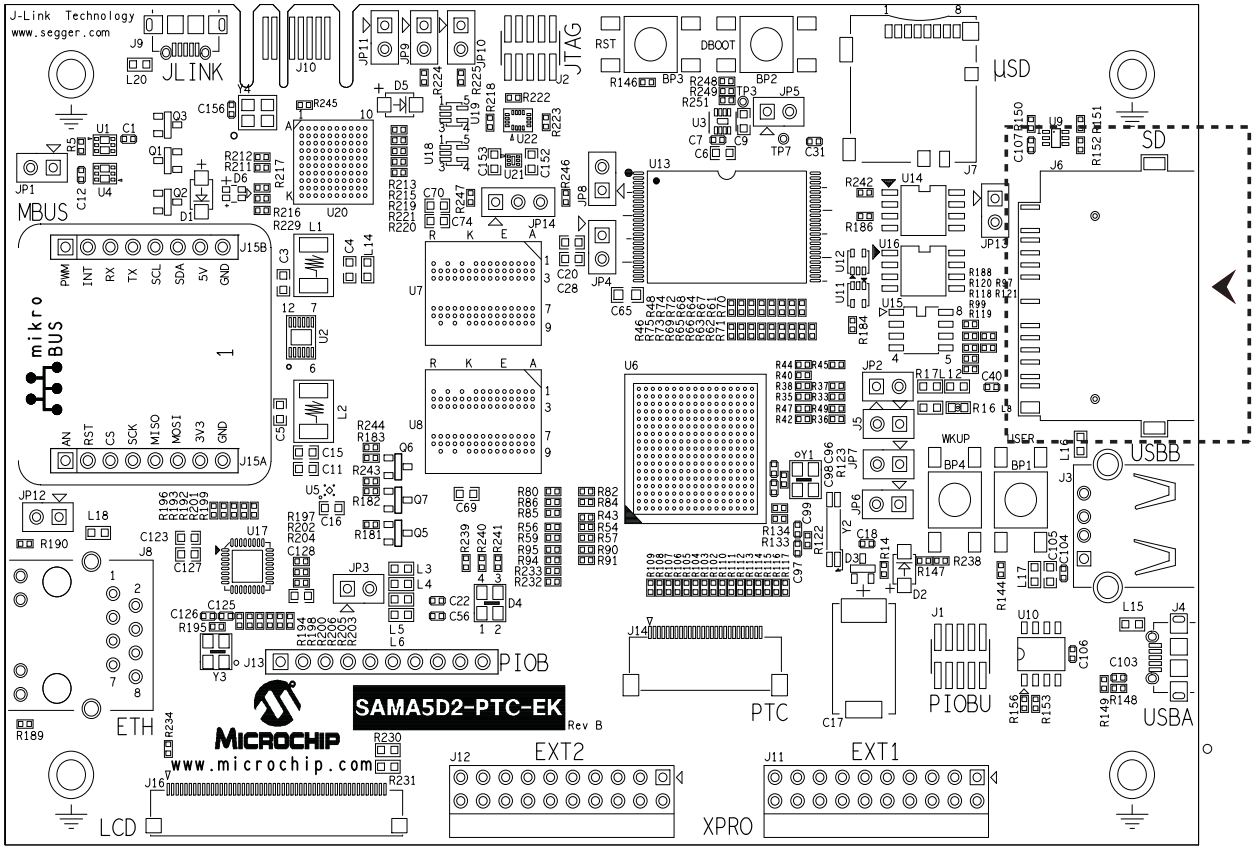


Figure 3-22. Standard SD Socket J6 Location



The table below describes the pin assignment of SD/MMC connector J6.

Table 3-7. Standard SD Socket J6 Pin Assignment

Pin No	Mnemonic	Signal Description
1	MCI0_DA3	SDMMC0_DAT3_PA5
2	MCI0_CDA	SDMMC0_CMD_PA1
3	GND	GND
4	VCC	VDDSDHC (3.3V or 1.8V)
5	MCI0_CK	SDMMC0_CK_PA0
6	MCI0_CD	SDMMC0_CD_PA13 (card detect)
7	MCI0_DA0	SDMMC0_DAT0_PA2
8	MCI0_DA1	SDMMC0_DAT1_PA3
9	MCI0_DA2	SDMMC0_DAT2_PA4
10	MCI0_DA4	SDMMC0_DAT4_PA6
11	MCI0_DA5	SDMMC0_DAT5_PA7
12	MCI0_DA6	SDMMC0_DAT6_PA8
13	MCI0_DA7	SDMMC0_DAT7_PA9

Pin No	Mnemonic	Signal Description
14	MCI0_WP	SDMMC0_WP_PA12
15	GND	GND
16	GND	GND

3.2.9.3 SDMMC0 VDDHC Voltage Switching

The board uses an ADG849 to switch the power line VDDSDHC_3V3 or VDDSDHC_1V8 through the command line SDMMC0_VDDSEL_PA11.

Figure 3-23. SDMMC0 VDDSDHC Voltage Switching

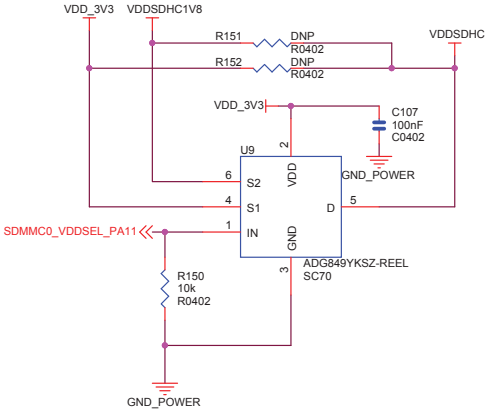


Table 3-8. SDMMC1 Power Command

PIO	Mnemonic	Signal Description
PA11	SDMMC0_VDDSEL	Selects 3.3V or 1.8V

3.2.9.4 SDMMC1 Card Connector

A microSD card connector, connected to SDMMC1, is mounted on the top side of the board. The SDMMC1 communication is based on a 9-pin interface (clock, command, card detect, four data and power lines). A card detection switch is included. The microSD connector can be used to connect any microSD card for mass storage.

Figure 3-24. SDMMC1 microSD Socket

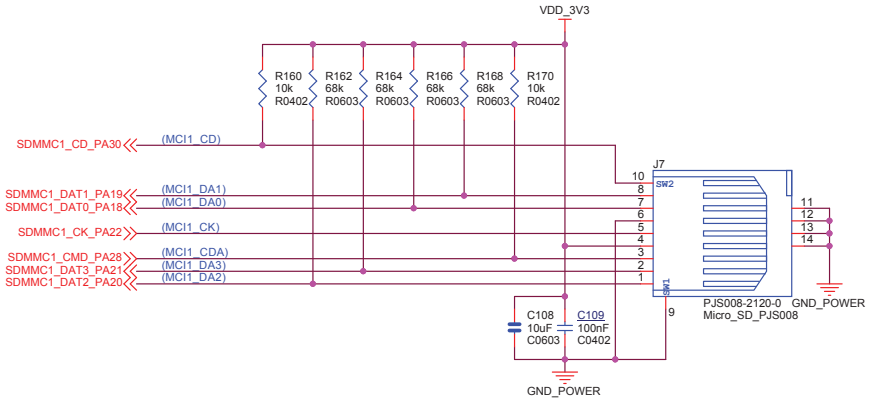
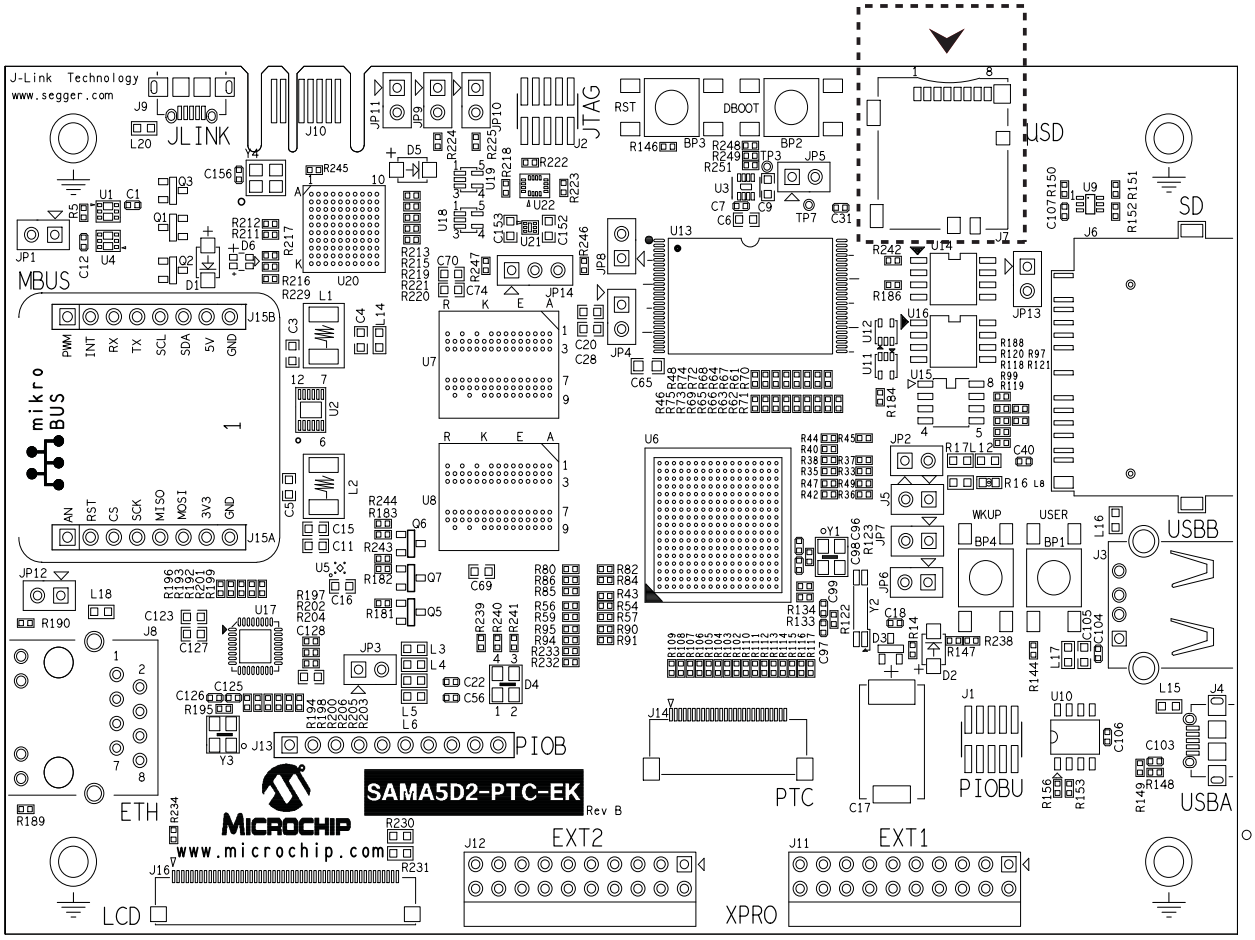


Figure 3-25. microSD Socket J7 Location



The table below describes the pin assignment of microSD connector J7.

Table 3-9. microSD Socket J7 Pin Assignment

Pin No	Mnemonic	PIO	Shared	Signal Description
1	SDMMC1_DAT2	PA20	–	Data bit 2
2	SDMMC1_DAT3	PA21	–	Data bit 3
3	SDMMC1_CDA	PA28	–	Command
4	VCC	–	–	3.3V supply voltage
5	SDMMC1_CK	PA22	–	Clock
6	GND	–	–	Common ground
7	SDMMC1_DAT0	PA18	–	Data bit 0
8	SDMMC1_DAT1	PA19	–	Data bit 1
9	SW1	GND	–	Not used
10	SDMMC1_CD	PA30	–	Card detection switch
11	GND	–	–	Common ground

Pin No	Mnemonic	PIO	Shared	Signal Description
12	GND	–	–	Common ground
13	GND	–	–	Common ground
14	GND	–	–	Common ground

3.2.10 Communication Interfaces

The SAMA5D2-PTC-EK board is equipped with Ethernet and USB host/device communication interfaces. This section describes the signals and connectors related to the ETH and USB communication interfaces.

3.2.10.1 Ethernet 10/100 (GMAC) Port

The SAMA5D2-PTC-EK board features a Micrel PHY device (KSZ8081) operating at 10/100 Mb/s. The board supports RMII interface modes. The Ethernet interface consists of two pairs of low-voltage differential pair signals designated from GRX± and GTX± plus control signals for link activity indicators. These signals can be used to connect to a 10/100 Base-T RJ45 connector integrated on the SAMA5D2-PTC-EK board.

An individual 48-bit MAC address (Ethernet hardware address) is allocated to each product. This number is stored in the Microchip 24AA02E48 I2C serial EEPROM (refer to Serial EEPROM with Unique MAC Address).

Additionally, for monitoring and control purposes, a LED functionality is carried on the RJ45 connectors to indicate activity, link, and speed status.

For more information about the Ethernet controller device, refer to the Micrel KSZ8081RN controller manufacturer's datasheet.

Figure 3-26. Ethernet Interface

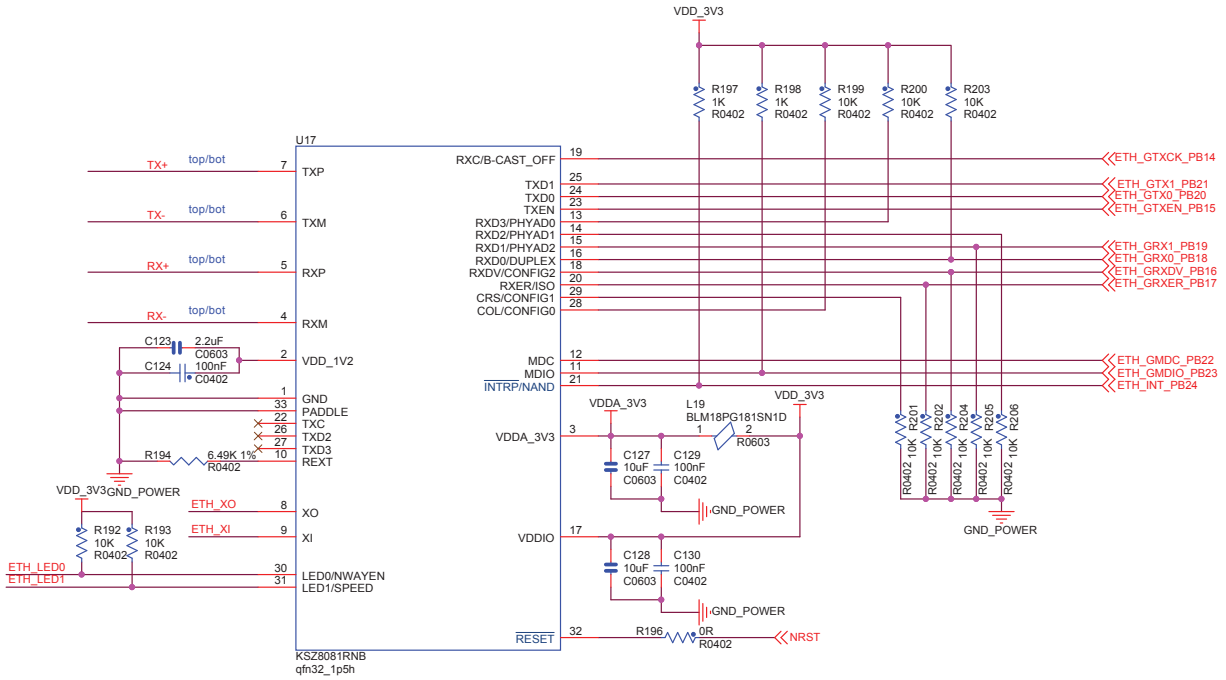


Table 3-10. Ethernet PHY 10/100 Signal Descriptions

PIO	Mnemonic	Shared	Signal Description
PB14	ETH_GTXCK	_	Transmit clock
PB15	ETH_GTXEN	_	Transmit enable
PB16	ETH_GRXDV	_	Receive data valid
PB17	ETH_GRXER	_	Receive error
PB18	ETH_GRX0	_	Receive data 0
PB19	ETH_GRX1	_	Receive data 1
PB20	ETH_GTX0	_	Transmit data 0
PB21	ETH_GTX1	_	Transmit data 1
PB22	ETH_GMDC	_	Management data clock
PB23	ETH_GMDIO	_	Management data in/out
PB24	ETH_GTX_INT	_	Interrupt (open drain)

Figure 3-27. Ethernet PHY Connector J8

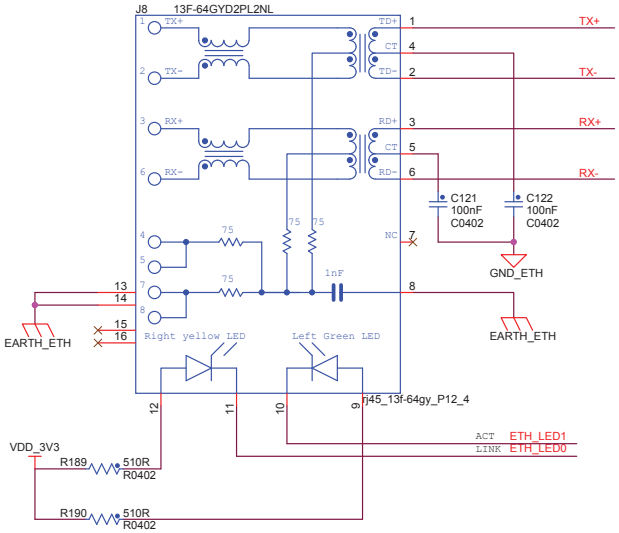
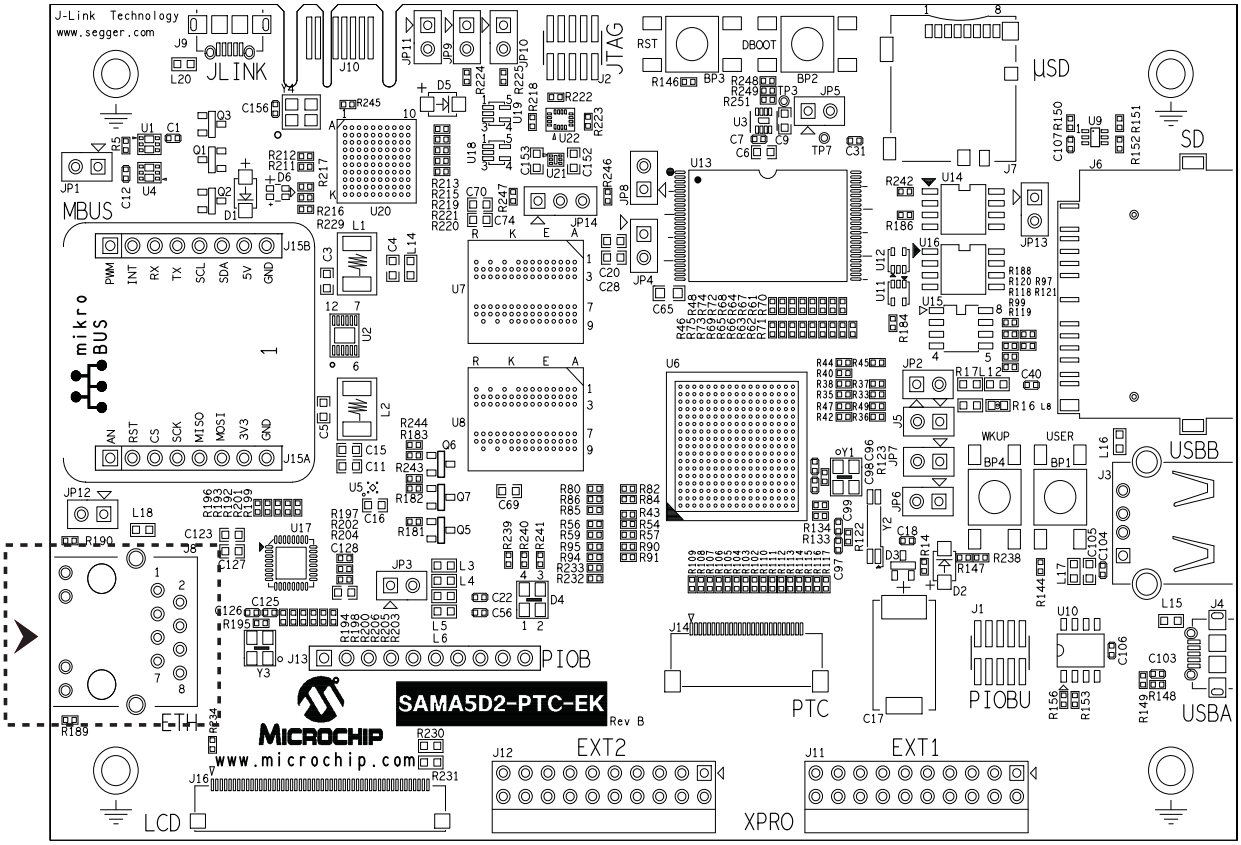


Figure 3-28. Ethernet RJ45 Connector J8 Location



The table below describes the pin assignment of Ethernet connector J8.

Table 3-11. Ethernet RJ45 Connector J8 Pin Assignment

Pin No	Mnemonic	Signal Description
1	TX+	Transmit
2	TX-	Transmit
3	RX+	Receive
4	Decoupling capacitor	–
5	Decoupling capacitor	–
6	RX-	Receive
7	NC	–
8	EARTH / GND	Common ground
9	ACT LED	LED activity
10	ACT LED	LED activity
11	LINK LED	LED link connection
12	LINK LED	LED link connection
13	EARTH / GND	Common ground

Pin No	Mnemonic	Signal Description
14	EARTH / GND	Common ground
15	NC	–
16	NC	–

3.2.10.2 USB Host/Device A, B

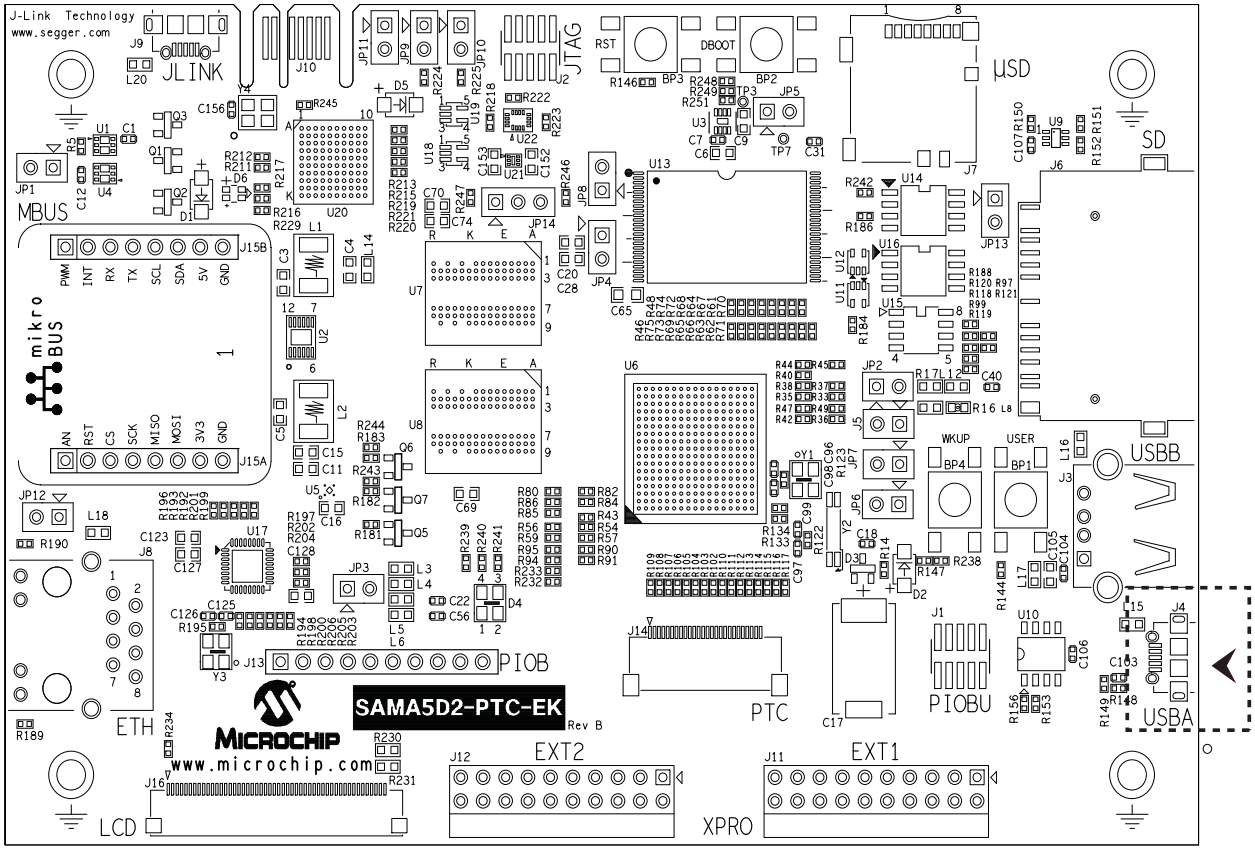
The USB (Universal Serial Bus) is a hot-pluggable general-purpose high-speed I/O standard for computer peripherals. The standard defines connector types, cabling, and communication protocols for interconnecting a wide variety of electronic devices. The USB 2.0 Specification defines data transfer rates as high as 480 Mbps (also known as High Speed USB). A USB host bus connector uses 4 pins: a power supply pin (5V), a differential pair (D+ and D- pins) and a ground pin.

The SAMA5D2-PTC-EK board features three USB communication ports named USB-A to USB-C:

- USB-A device interface
  - One USB device standard micro-AB connector.
  - This port has a VBUS detection function made through the R148-R149 resistor bridge.
  - The USB-A port is used as a primary power source and as a communication link for the board, and derives power from the PC over the USB cable. In most cases, this port is limited to 500 mA.
- USB-B (host port B high- and full-speed interface)
  - One USB host type A connector.
  - The USB-B host port is equipped with a 500 mA high-side power switch to enable powering devices connected to it.
- UBC-C (High-Speed Inter-Chip/HSIC port)
  - One USB high-speed host port with an HSIC interface.
  - The port is connected to a single 2-pin jumper.

3.2.10.3 USB-A Interface

Figure 3-29. USB-A Type microAB Connector J4 Location



3.2.10.4 USB-A VBUS Detection

The USB-A port (J4) features a VBUS detection function provided by the R148-R149 resistor bridge.

The figure below shows the USB implementation on the USBA port.

Figure 3-30. USB-A Power and VBUS Detection

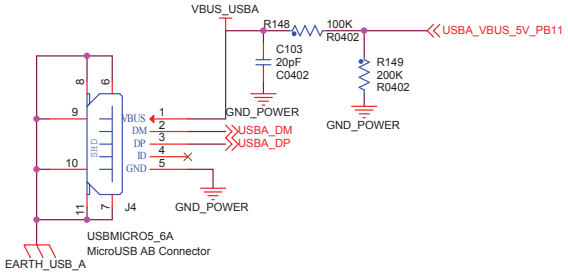


Table 3-12. USB-A PIO Signal Descriptions

PIO	Mnemonic	Shared	Signal Description
PB11	USBA_VBUS_5V	-	VBUS insertion detection

3.2.10.5 USB-B Interface

The figure below shows the USB implementation on the USB-B port.

Figure 3-31. USB-B Interface

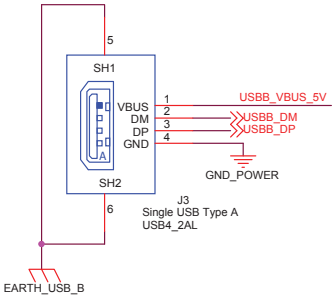


Figure 3-32. USB-B Type A Connector J3 Location

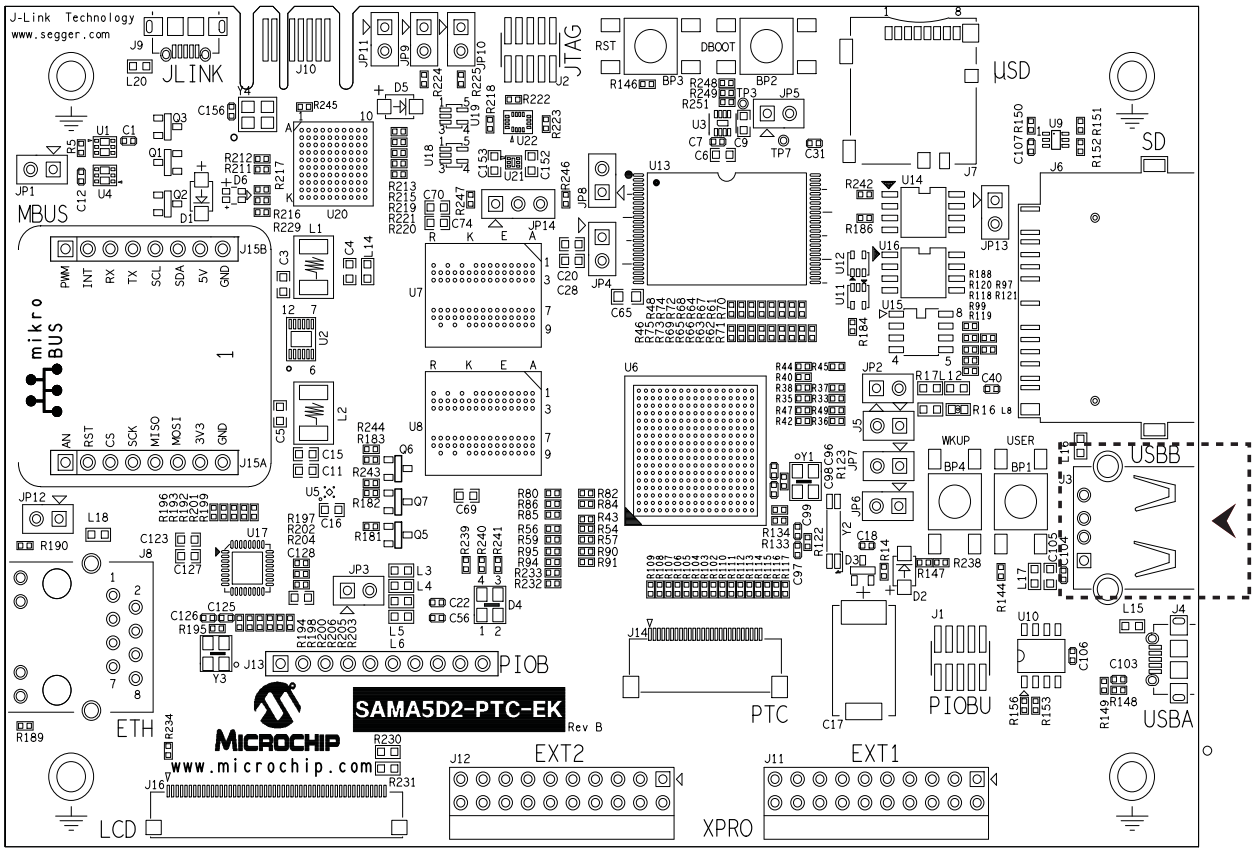


Table 3-13. USB-B PIO Signal Descriptions

PIO	Mnemonic	Shared	Signal Description
PB12	USBB_EN_5V	–	Power switch enable (active high)
PB13	USBB_OVCUR	–	Indicates overcurrent (open drain)

USB-B Power Switch

The USB-B Host port is equipped with a 500 mA high-side power switch for self-powered and bus-powered applications. If the client device is bus-powered, the carrier can supply a 5V, 500mA power to the client device. The USBB_EN_5V_PB12 signal controls the power switch and current limiter, the Micrel MIC2025, which in turn supplies power to a bus-powered client device. Per the USB specification, bus-powered USB 2.0 devices are limited to a maximum of 500 mA. The MIC2025 limits the current and indicates an overcurrent with the USBB_OVCUR_PB13 signal.

The table below describes the pin assignment of the USB-A and USB-B connectors.

Table 3-14. USB-A and USB-B Connector Signal Descriptions

Pin No	Mnemonic	Signal Description
1	VBUS	5V power
2	DM	Data minus
3	DP	Data plus
4	ID	On-the-go identification
5	GND	Common ground

3.2.10.6 HSIC

High-Speed Inter-Chip (HSIC) is a standard for USB chip-to-chip interconnect with a 2-signal (strobe, data) source synchronous serial interface using 240 MHz DDR signaling to provide only high-speed 480 Mbps data rate.

The interface operates at high speed, 480 Mbps, and is fully compatible with existing USB software stacks. It meets all data transfer needs through a single unified USB software stack.

The HSIC interface is not used on the board and is connected to two-point jumper J5 (not mounted).

Figure 3-33. HSIC Interface

3.3 External Interfaces

3.3.1 LCD TFT Interface

This section describes the signals and connectors related to the LCD interface.

3.3.1.1 LCD Interface

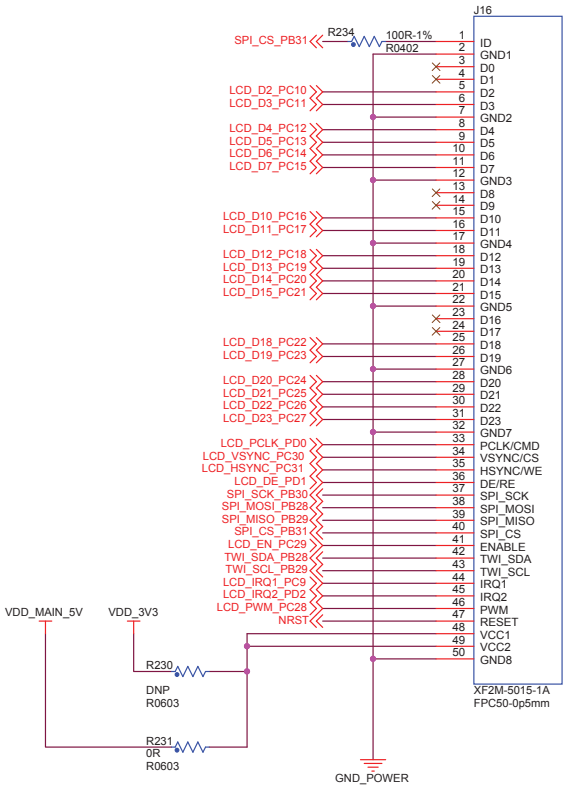
The SAMA5D2-PTC-EK board provides a connector with 18 bits of data and control signals to the LCD interface. Other signals are used to control the LCD and are available on connector J16: TWI, SPI, two GPIOs for interrupt, 1-wire and power supply lines.

This connector is used to connect LCD display series 43xx or 70xx from PDA.

3.3.1.2 LCD Expansion Header

J16 is a 1.27-mm pitch, 50-pin header. It gives access to the LCD signals.

Figure 3-34. LCD Expansion Header Interface

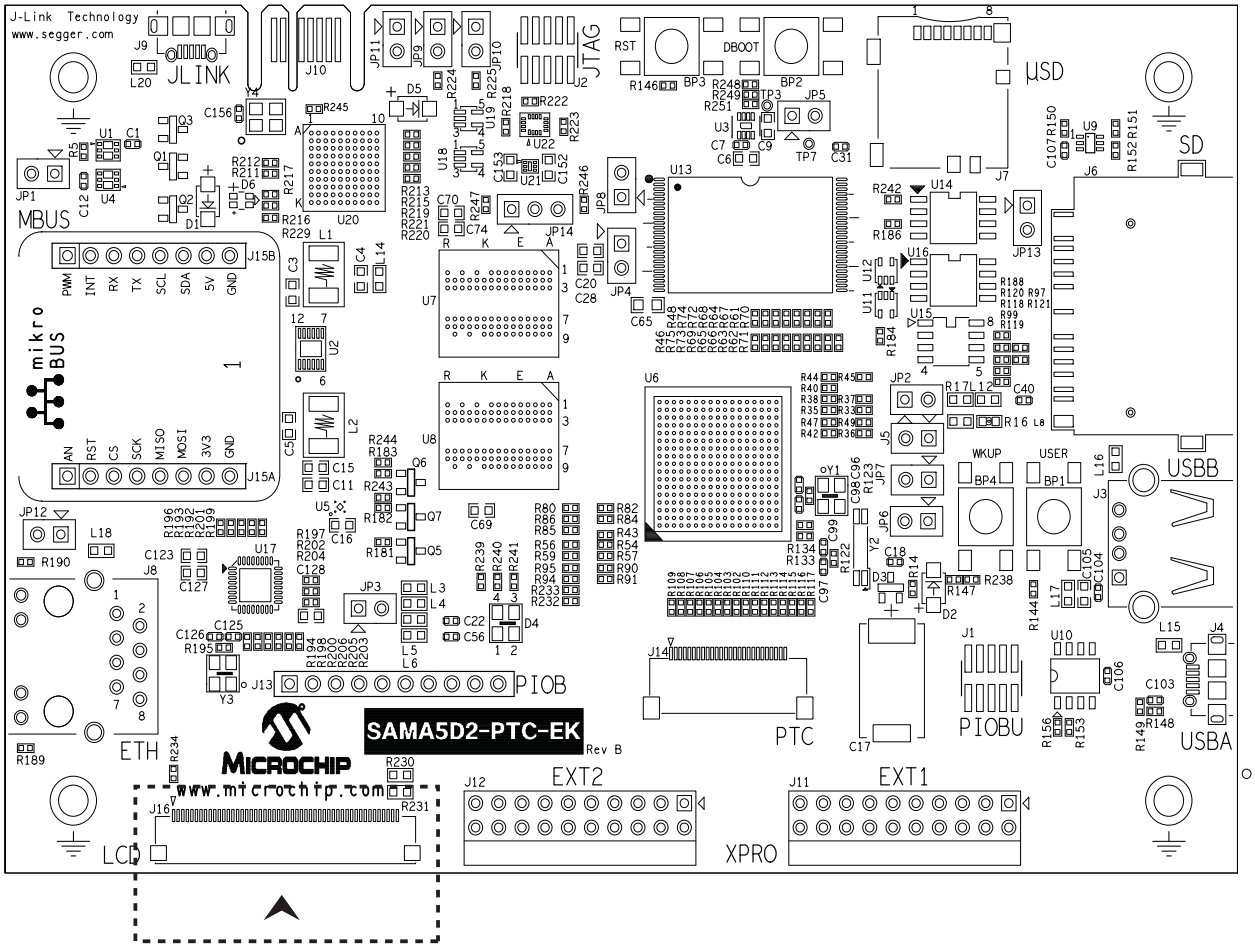


3.3.1.3 LCD Power

In order to operate correctly with various LCD modules, two voltage lines are available: 3.3V and 5VCC (default). The selection is made with 0R resistors R230 and R231.

3.3.1.4 LCD Connector JX

Figure 3-35. LCD Connector J16 Location



The table below describes the pin assignment of LCD FPC connector J16.

Table 3-15. LCD Connector J16 Signal Descriptions

Pin No	Signal	PIO	Signal	RGB Interface Function
1	ID	PB31	_	ID LCD module
2	GND	_	GND	GND
3	LCDDAT0	–	D0	–
4	LCDDAT1	–	D1	–
5	LCDDAT2	PC10	D2	Data line
6	LCDDAT3	PC11	D3	Data line
7	GND	_	GND	GND
8	LCDDAT4	PC12	D4	Data line
9	LCDDAT5	PC13	D5	Data line
10	LCDDAT6	PC14	D6	Data line

Pin No	Signal	PIO	Signal	RGB Interface Function
11	LCDDAT7	PC15	D7	Data line
12	GND	_	GND	GND
13	LCDDAT8	–	D8	–
14	LCDDAT9	–	D9	–
15	LCDDAT10	PC16	D10	Data line
16	LCDDAT11	PC17	D11	Data line
17	GND	GND	GND	GND
18	LCDDAT12	PC18	D12	Data line
19	LCDDAT13	PC19	D13	Data line
20	LCDDAT14	PC20	D14	Data line
21	LCDDAT15	PC21	D15	Data line
22	GND	_	GND	GND
23	LCDDAT16	–	D16	–
24	LCDDAT17	–	D17	–
25	LCDDAT18	PC22	D18	Data line
26	LCDDAT19	PC23	D19	Data line
27	GND	_	GND	GND
28	LCDDAT20	PC24	D20	Data line
29	LCDDAT21	PC25	D21	Data line
30	LCDDAT22	PC26	D22	Data line
31	LCDDAT23	PC27	D23	Data line
32	GND	_	GND	GND
33	LCDPCK	PD0	PCLK	Pixel clock
34	LCDVSYNC	PC30	VSYNC/CS	Vertical sync
35	LCDHSYNC	PC31	HSYNC/WE	Horizontal sync
36	LCDDEN	PD1	DATA_ENABLE	Data enable
37	SPI_SPCK	PB30	SPI_SCK	–
38	SPI_MOSI	PB28	SPI_MOSI	(Shared with TWI)
39	SPI_MISO	PB29	SPI_MISO	(Shared with TWI)
40	SPI_NPCS0	PB31	SPI_CS	–
41	LCDDISP	PC29	ENABLE	Display enable signal
42	TWD	PB28	TWI_SDA	I2C data line (maXTouch)

Pin No	Signal	PIO	Signal	RGB Interface Function
43	TWCK	PB29	TWI_SCL	I2C clock line (maXTouch)
44	GPIO	PC9	IRQ1	maXTouch interrupt line
45	GPIO	PD2	IRQ2	Interrupt line for other I2C devices
46	LCDPWM	PC28	PWM	Backlight control
47	RESET	–	RESET	Reset for both display and maXTouch
48	Main_5V/3V3	VCC	VCC	3.3V or 5V supply (0R)
49	Main_5V/3V3	VCC	VCC	3.3V or 5V supply (0R)
50	GND	_	GND	GND

3.3.2 RGB LED

The SAMA5D2-PTC-EK board features one RGB LED which can be controlled by the user. The three LED cathodes are controlled via GPIO PWM or timer/counter pins.

Figure 3-36. RGB LED Indicators

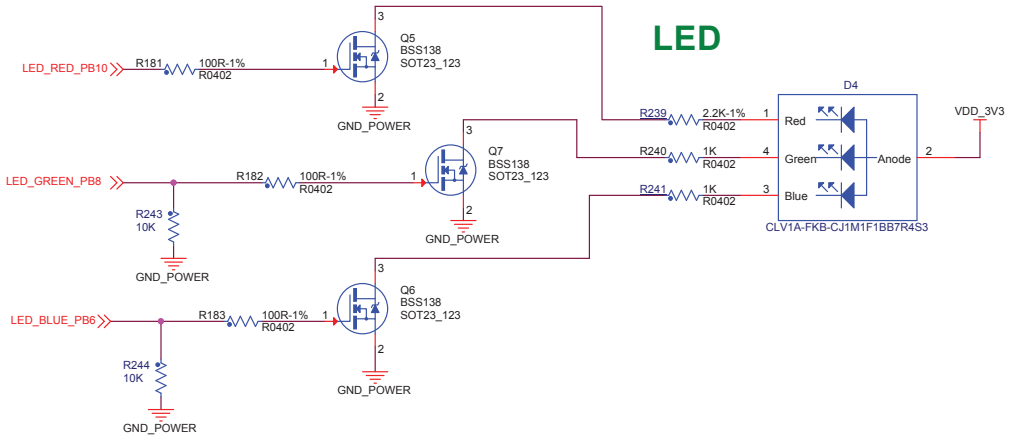


Table 3-16. RGB LED PIOS

Signal	PIO	Function
LED_RED	PB10	TIOB3
LED_GREEN	PB8	PWML3
LED_BLUE	PB6	PWML2

3.4 Debugging Capabilities

The SAMA5D2-PTC-EK includes two main debugging interfaces to provide debug-level access to the SAMA5D2:

- One UART through USB JLINK-CDC
- Two JTAG interfaces, one connected directly to the MPU using connector J2 and one through the JLINK-OB interface USB port J9

3.4.1 Debug JTAG

This section describes the signals and connectors related to the JTAG interface.

A 10-pin JTAG header is provided on the SAMA5D2-PTC-EK board to facilitate software development and debugging using various JTAG emulators. The interface signals have a voltage level of 3.3V.

Figure 3-37. JTAG Interface

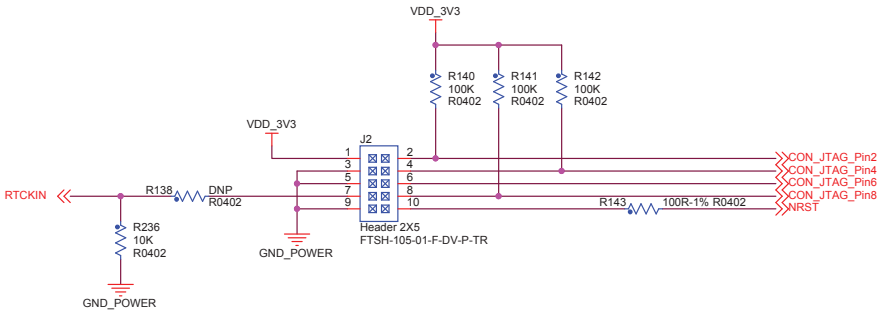
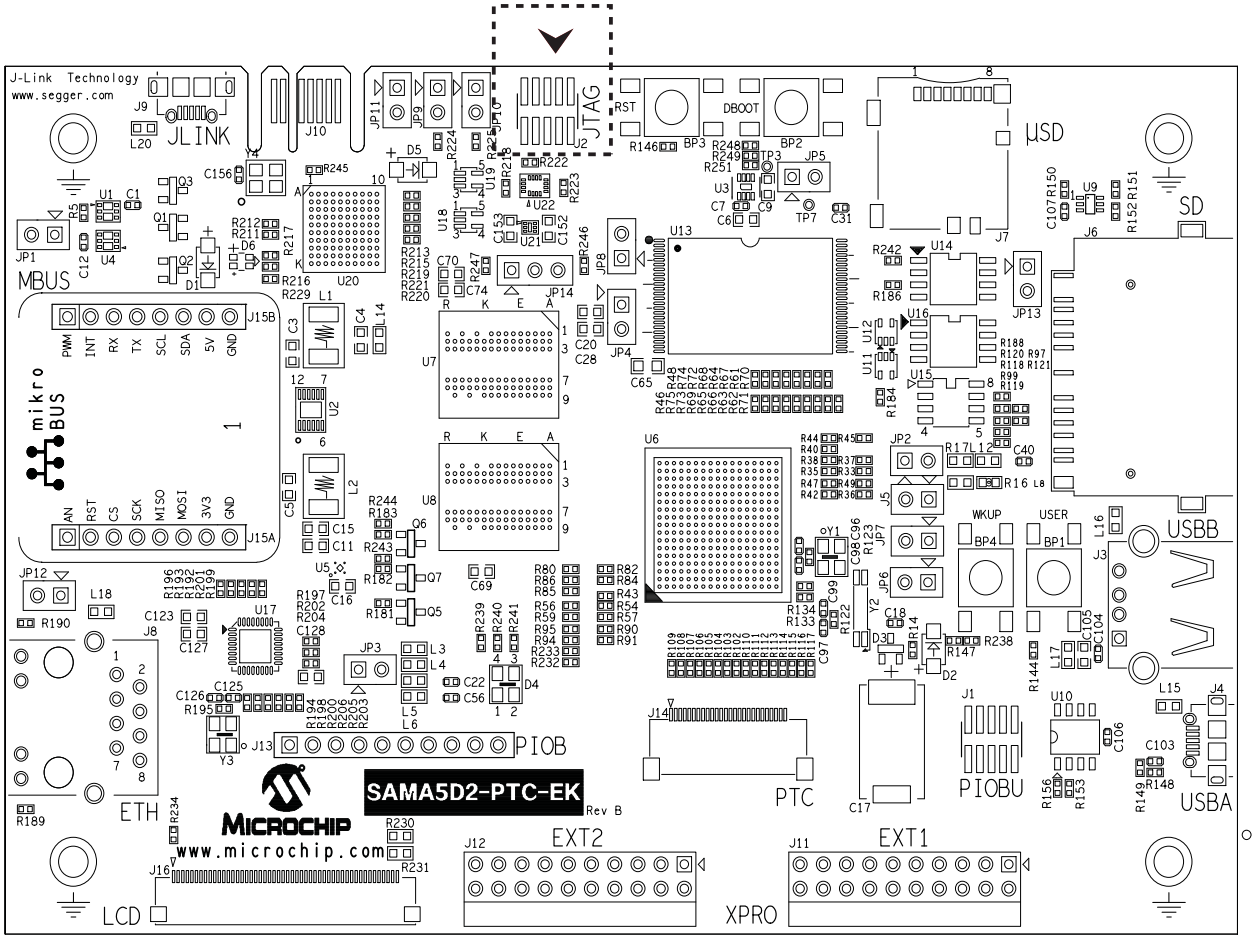


Figure 3-38. JTAG Connector J2 Location



The table below describes the pin assignment of JTAG connector J2.

Table 3-17. JTAG/ICE Connector J2 Pin Assignment

Pin No	Mnemonic	Signal Description
1	VTref. 3.3V power	This is the target reference voltage (main 3.3V).
2	TMS TEST MODE SELECT	JTAG mode set input into target CPU
3	GND	Common ground
4	TCK TEST CLOCK - Output timing signal, for synchronizing test logic and control register access	JTAG clock signal into target CPU
5	GND	Common ground
6	TDO JTAG TEST DATA OUTPUT - Serial data input from the target	JTAG data output from target CPU
7	RTCK - Input return test clock signal from the target	Some targets with a slow system clock must synchronize the JTAG inputs to internal clocks. In the present case, such synchronization is unneeded and TCK is merely looped back into RTCK.
8	TDI TEST DATA INPUT - Serial data output line, sampled on the rising edge of the TCK signal	JTAG data input into target CPU
9	GND	Common ground
10	nRST RESET	Active-low reset signal. Target CPU reset signal.

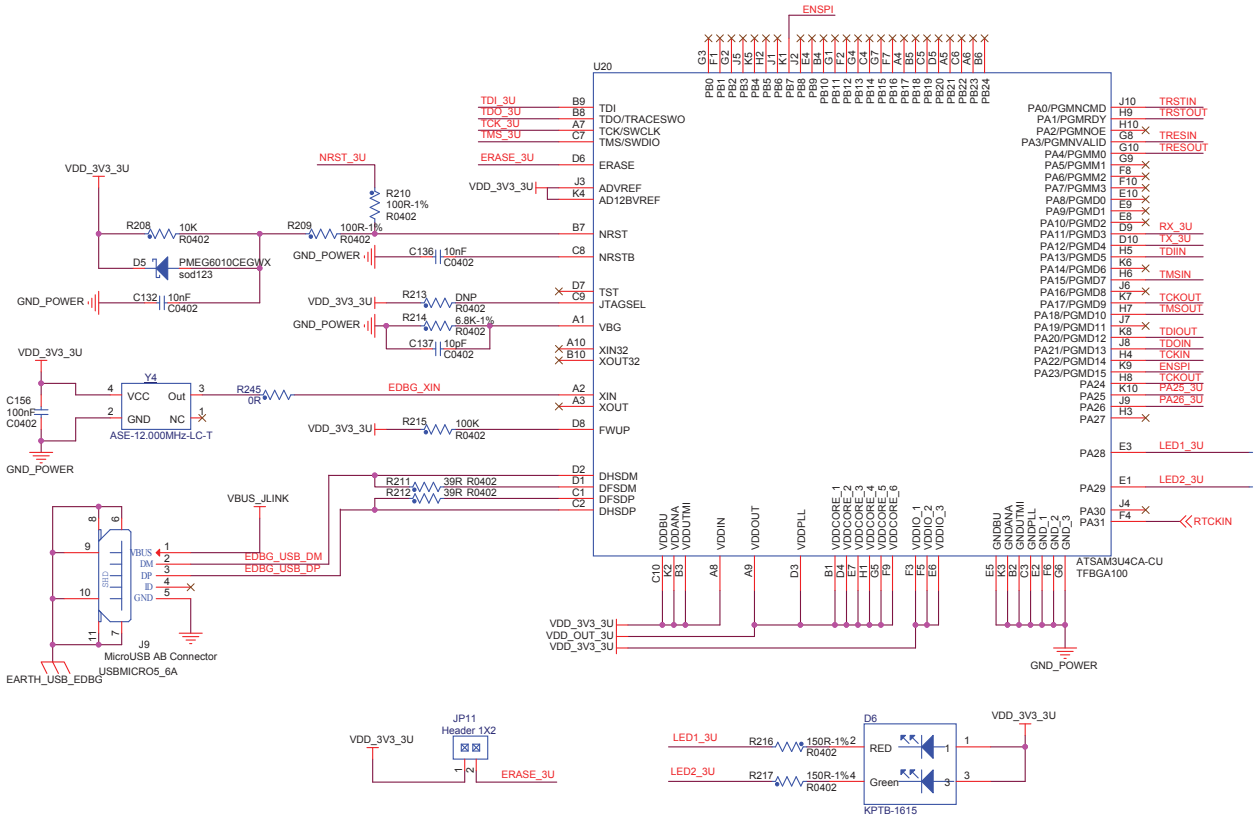
3.4.2 Embedded Debugger (JLINK-OB) Interface

The SAMA5D2-PTC-EK includes a built-in SEGGER J-Link-On-Board device. The functionality is implemented with an ATSAM3U4C microcontroller in an LFBGA100 package. The ATSAM3U4C provides the functions of JTAG and a bridge USB/Serial debug port (CDC). One two-colored LED (D6) mounted near the SAM3 chip (U20) shows the status of the J-Link-On-Board device.

J-Link-OB-ATSAM3U4C was designed in order to provide an efficient, low-cost, on-board alternative to the standard J-Link.

The USB JLINK-OB port is used as a secondary power source and as a communication link for the board, and derives power from the PC over the USB cable. This port is limited in most cases to 500 mA. A single PC USB port is sufficient to power the board.

Figure 3-39. JLINK-OB Interface



3.4.2.1 Disabling JLINK-OB (ATSAM3U4C)

Jumper JP10 disables the J-Link-OB-ATSAM3U4C JTAG functionality. When the jumper is installed, it grounds pin 26 of the ATSAM3U4C that is normally pulled high. A quad analog switch is used to select the JTAG interface.

- Jumper JP10 not installed: J-Link-OB-ATSAM3U4C is enabled and fully functional.
- Jumper JP10 installed: J-Link-OB-ATSAM3U4C is disabled and an external JTAG controller can be used through the 10-pin JTAG port J2.

Jumper JP10 disables only the J-Link functionality. The debug serial com port that is emulated through a Communication Device Class (CDC) of the same USB connector remains operational (if JP9 is open).

Figure 3-40. Enabling/Disabling JLINK-OB and JLINK-CDC

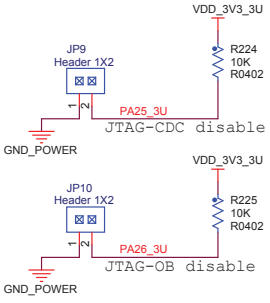
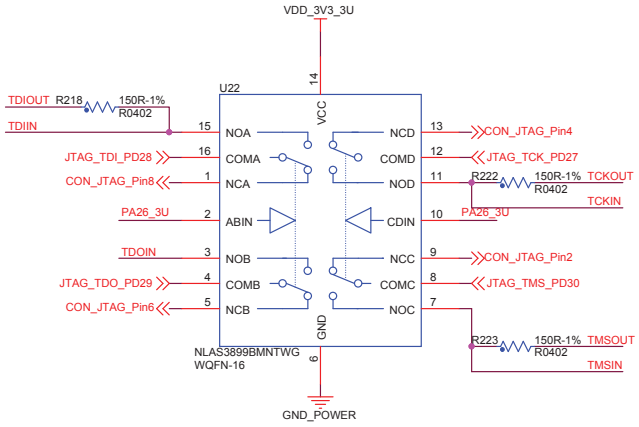


Figure 3-41. JTAG Switch



3.4.3 Hardware UART via CDC

In addition to the J-Link-OB functionality, the ATSAM3U4C microcontroller provides a bridge to a debug serial port (UART DBGU) of the SOM's processor. The port is made accessible over the same USB connection used by JTAG by implementing Communication Device Class (CDC), which allows terminal communication with the target device.

This feature is enabled only if the SAM3U/PA25 (pin K10) is not grounded. The pin is normally pulled high and controlled by jumper JP9.

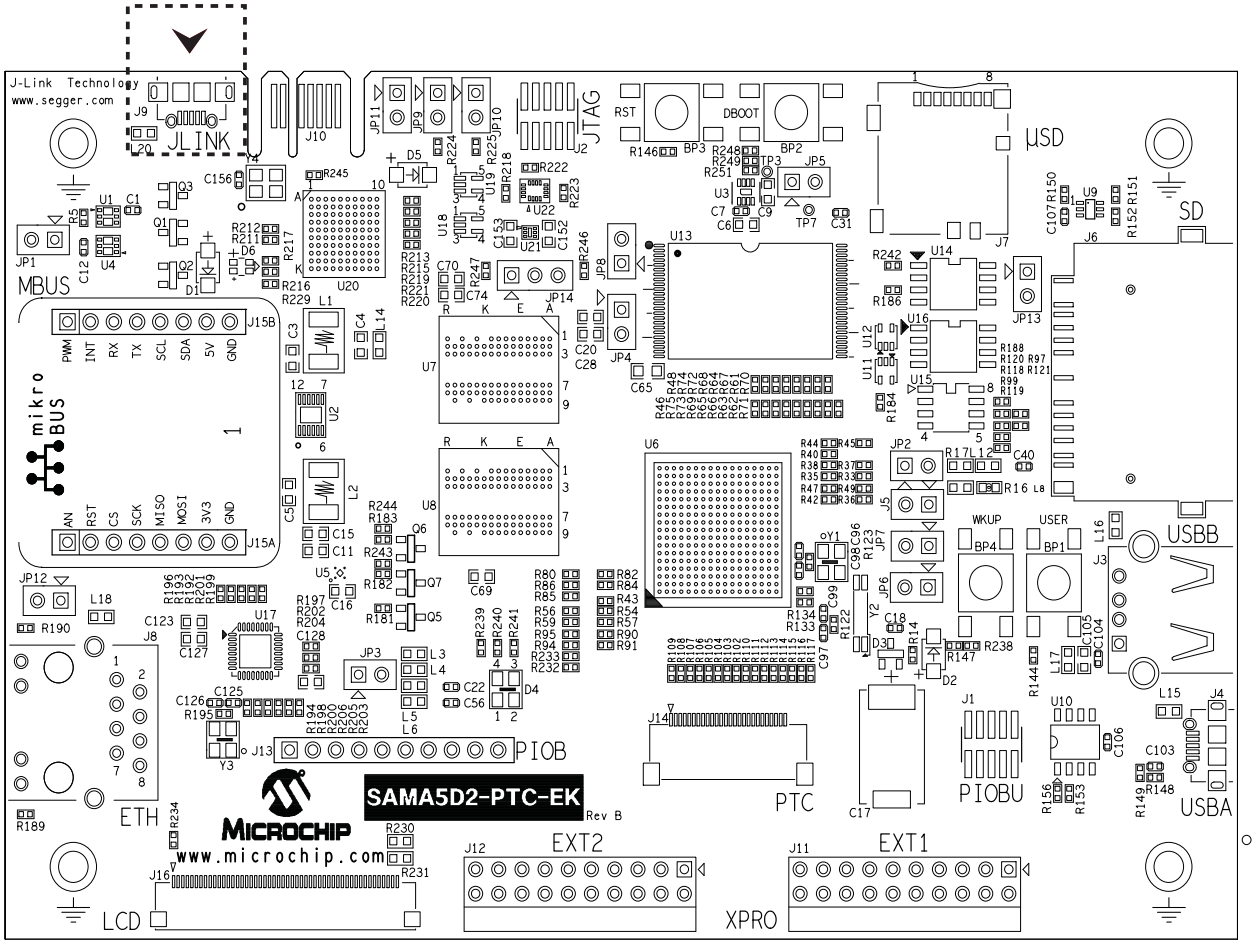
- Jumper JP9 not installed: the J-Link-CDC is enabled and fully functional.
- Jumper JP9 installed: the J-Link-CDC device is disabled.

The USB Communications Device Class (CDC) enables to convert the USB device into a serial communication device. The target device running USB-Device CDC is recognized by the host as a serial interface (USB2COM, virtual COM port) without the need to install a special host driver (since the CDC is standard). All PC software using a COM port work without modifications with this virtual COM port. Under Windows, the device shows up as a COM port; under Linux, as a /dev/ACMx device. This enables the user to use host software which was not designed to be used with USB, such as a terminal program.

Table 3-18. Debug COM Port PIOs Signal Descriptions

PIO	Mnemonic	Shared	Signal Description
PB26	URXD0	-	Receive data
PB27	UTXD0	-	Transmit data

Figure 3-42. JLINK-OB and CDC USB Connector J9 Location



The table below describes the pin assignment of USB connector J9.

Table 3-19. USB Connector J9 Pin Assignment

Pin No	Mnemonic	Signal Description
1	VBUS	5V power
2	DM	Data minus
3	DP	Data plus
4	ID	Not used
5	GND	Common ground

3.4.3.1 Board Edge Connector

This connector is used to upgrade or download code to the ATSAM3U4C microcontroller JLINK-OB.

3.5 PIO Usage on Expansion Connectors

3.5.1 PIOBU Interface

The SAMA5D2-PTC-EK board features eight tamper pins for static or dynamic intrusion detection, UART reception, and two analog pins for comparison.

For a description of intrusion detection, refer to the SAMA5D2 datasheet, chapter "Security Module".

Figure 3-43. PIOBU Connector

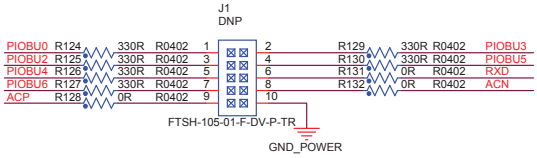
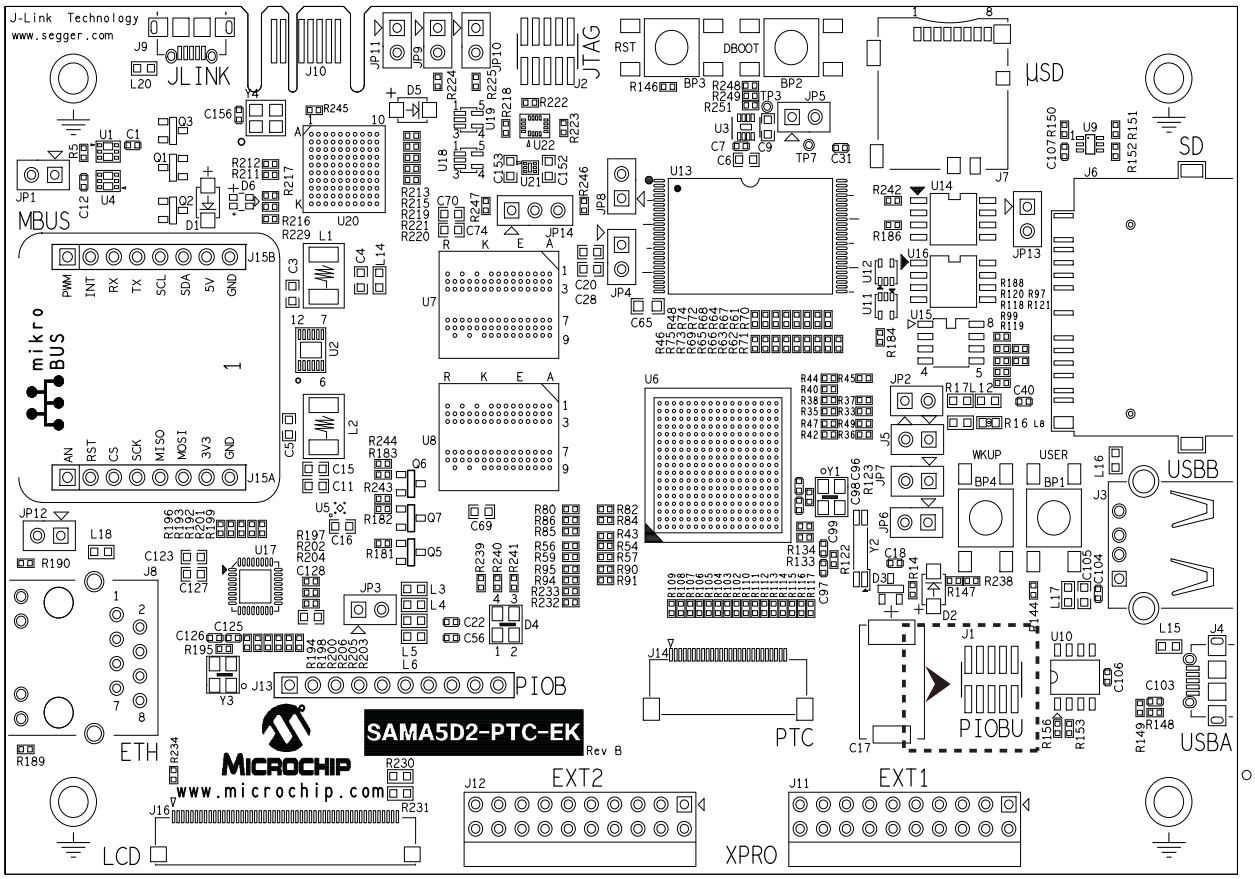


Figure 3-44. PIOBU Connector J1 Location



The table below describes the pin assignment of PIOBU connector J1.

Table 3-20. PIOBU Connector J1 Pin Assignment

Signal	Pin No.		Signal
PIOBU0	1	2	PIOBU3
PIOBU2	3	4	PIOBU5
PIOBU4	5	6	RXD
PIOBU6	7	8	ACN
ACP	9	10	GND

3.5.2 mikroBUS Interface

The SAMA5D2-PTC-EK hosts a pair of 8-pin female headers as mikroBus interface. The mikroBUS interface defines the main board sockets and add-on boards used for interfacing microprocessors with

integrated modules with proprietary pin configuration and silkscreen markings. The pinout consists of three groups of communication pins (SPI, UART and TWI), four additional pins (PWM, interrupt, analog input and reset) and two power groups (+3.3V and GND on the left, and 5V and GND on the right 1x8 header).

Figure 3-45. mikroBUS Interface

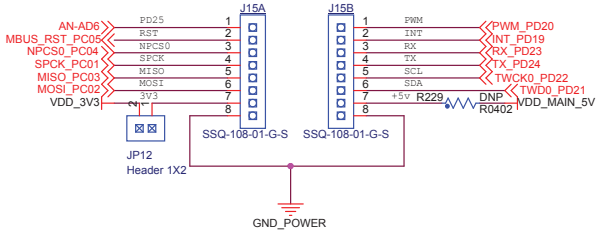
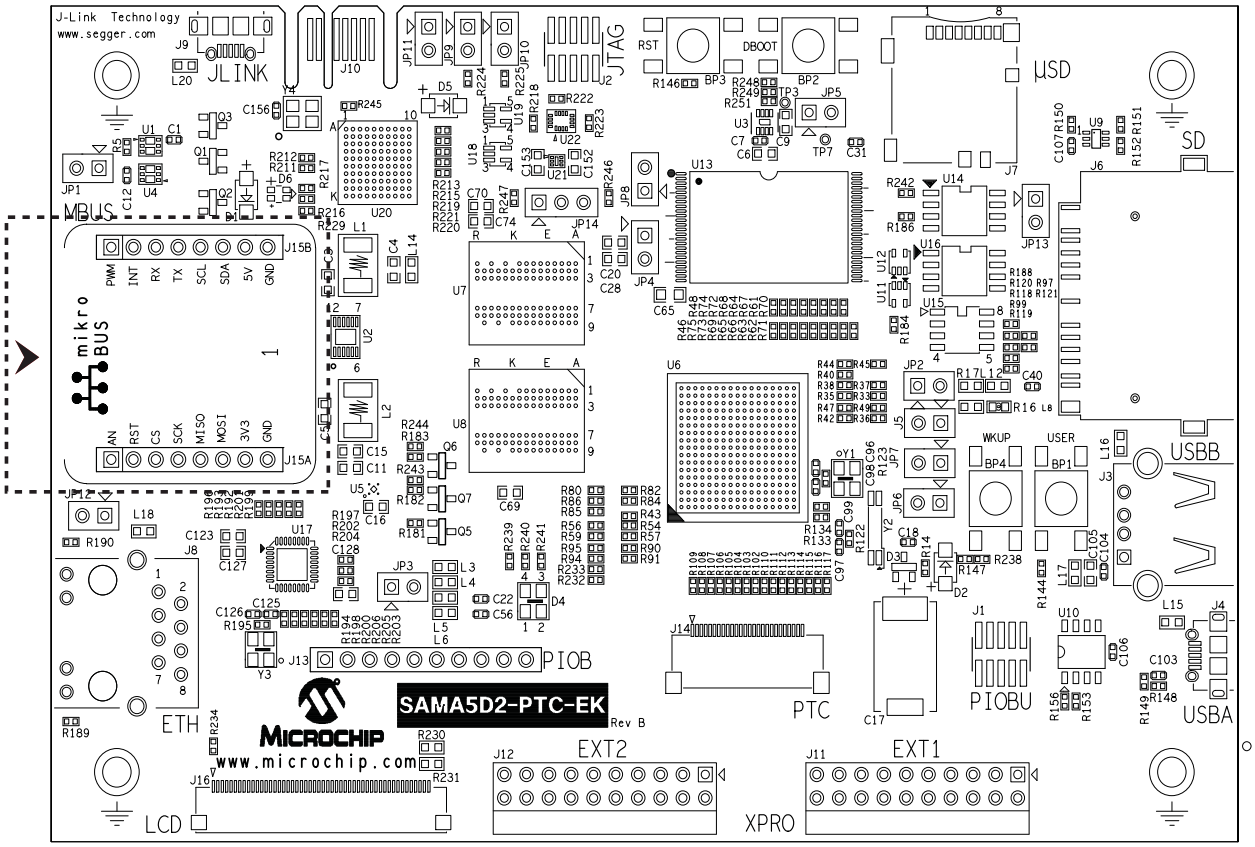


Figure 3-46. mikroBUS Connector J15 Location



The table below describes the pin assignment of mikroBUS1 connector J15.

Table 3-21. mikroBUS Connector J15 Pin Assignment

SAMA5D27		MBUS Signal	Pin No.		MBUS Signal	SAMA5D27	
Function	PIO					PIO	Function
Analog input	PD25	AN	1	1	PWM	PD20	PWM
Reset	PC05	RST	2	2	INT	PD19	Interrupt
SPI chip select	PC04	SPI_NPCS	3	3	UART_RX	PD23	UART receive

SAMA5D27		MBUS Signal	Pin No.		MBUS Signal	SAMA5D27	
Function	PIO					PIO	Function
SPI clock	PC01	SPI_SPCK	4	4	UART_TX	PD24	UART transmit
SPI MISO	PC03	SPI_MISO	5	5	TWI_SCL	PD22	TWI clock
SPI MOSI	PC02	SPI_MOSI	6	6	TWI_SDA	PD21	TWI data
3.3VCC	–	3V3 Supply	7	7	5V Supply	_	5VDD
GROUND	–	GND	8	8	GND	_	GROUND

3.5.3 XPRO Interface

The SAMA5D2-PTC-EK board hosts two connectors to interface XPRO QT boards. The QTouch Xplained Pro are extension boards that enable evaluation of Self-capacitance and Mutual capacitance modes using the Peripheral Touch Controller (PTC). The boards show how easy it is to design a capacitive touch board solution using the PTC without the need for any external components.

Nevertheless, the PTC IO pins available on XPRO connectors can be used as GPIO pins. Each of these can be configured as an input or output pin according to the PIO peripheral functions.

The GPIO voltage levels depend on the VDDIOP level supported by the SAMA5D2, 3.3V in this case.

Figure 3-47. XPRO EXT1 Connector

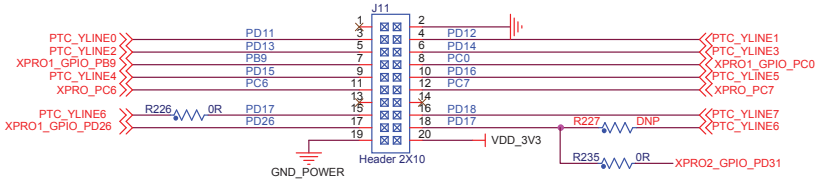
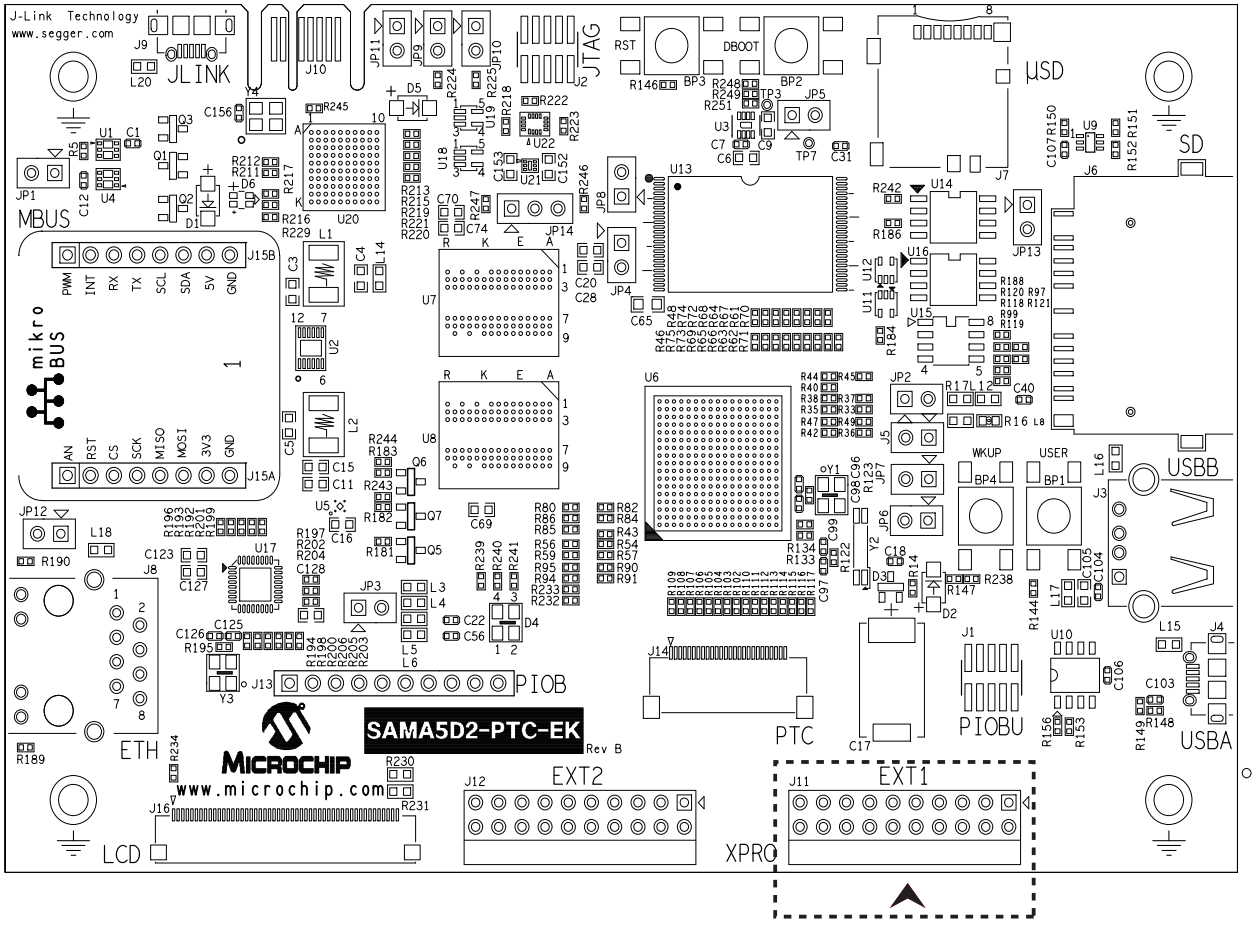


Figure 3-48. XPRO EXT1 Connector J11 Location



The table below describes the pin assignment of XPRO EXT1 connector J11.

Table 3-22. XPRO EXT1 Connector J11 Pin Assignment

SAMA5D27		XPRO Signal	Pin No.		XPRO Signal	SAMA5D27	
Function	Pin					Pin	Function
_	Not used	ID	1	2	GND	–	GROUND
PTC_YLINE0	PD11	ADC(+)	3	4	ADC(-)	PD12	PTC_YLINE1
PTC_YLINE2	PD13	GPIO	5	6	GPIO	PD14	PTC_YLINE3
GPIO	PA10	PWM(+)	7	8	PWM(-)	PC0	GPIO
PTC_YLINE4	PD15	IRQ/GPIO	9	10	SPI_SS_B/GPIO	PD16	PTC_YLINE5
XPRO_TWD	PC6	TWI_SDA	11	12	TWI_SCL	PC7	XPRO_TWCK
_	_	UART_RX	13	14	UART_TX	_	–
PTC_YLINE6	PD17	SPI_SS_A	15	16	SPI_MOSI	PD18	PTC_YLINE7
GPIO	PD26	SPI_MISO	17	18	SPI_SCK	PD31 or PD17	PTC_YLINE6
GROUND	–	GND	19	20	VCC 3V3	–	3.3V Supply

Figure 3-49. XPRO EXT2 Connector

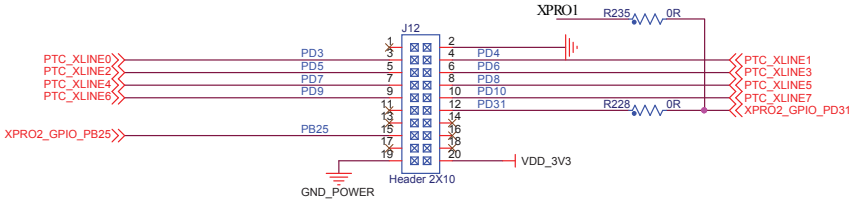
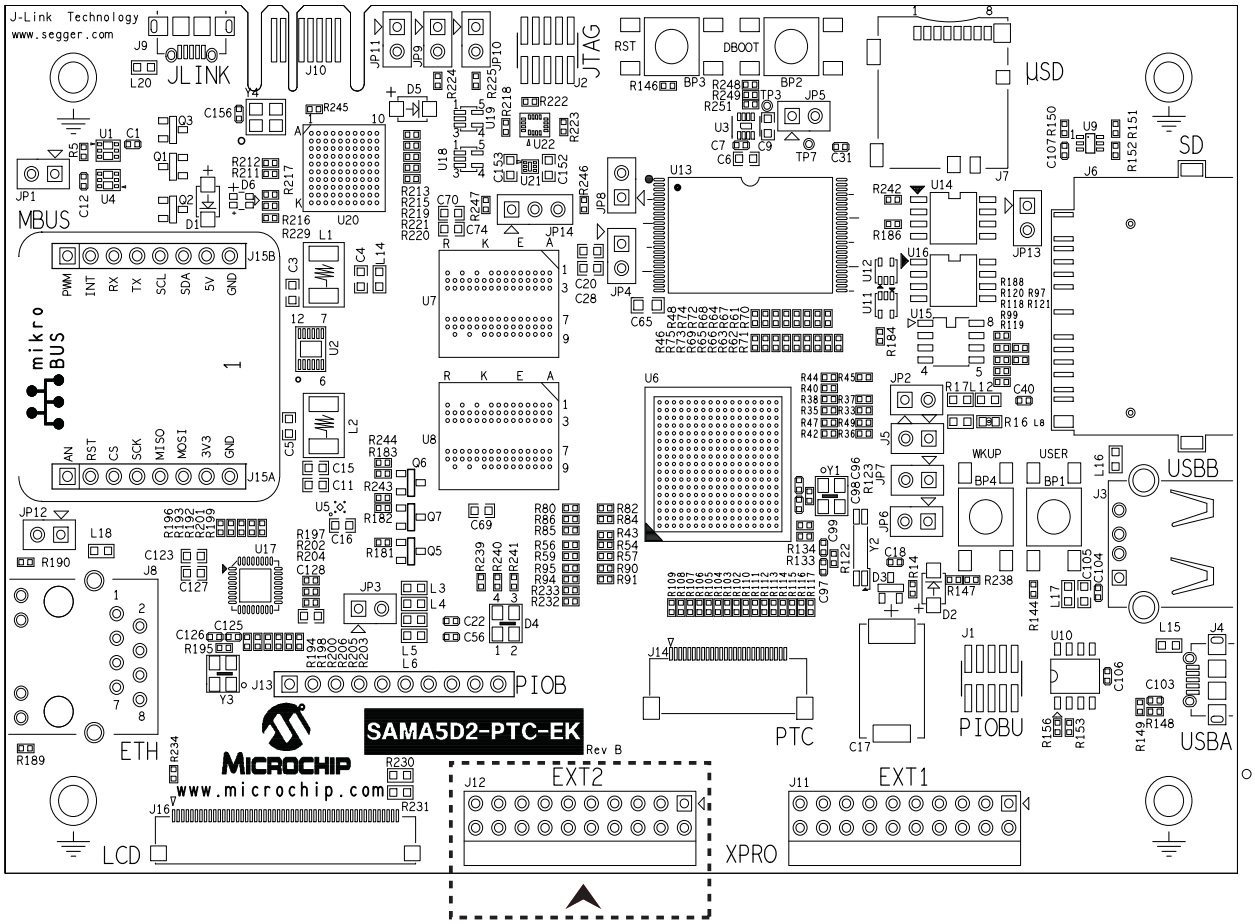


Figure 3-50. XPRO EXT2 Connector J12 Location



The table below describes the pin assignment of XPRO EXT2 connector J12.

Table 3-23. XPRO EXT2 Connector J12 Pin Assignment

SAMA5D27		XPRO Signal	Pin No.		XPRO Signal	SAMA5D27	
Function	Pio					Pio	Function
_	Not used	ID	1	2	GND	–	GROUND
PTC_XLINE0	PD3	ADC(+)	3	4	ADC(-)	PD4	PTC_XLINE1
PTC_XLINE2	PD5	GPIO	5	6	GPIO	PD6	PTC_XLINE3

SAMA5D27		XPRO Signal	Pin No.		XPRO Signal	SAMA5D27	
Function	Pio					Pio	Function
PTC_XLINE4	PD7	PWM(+)	7	8	PWM(-)	PD8	PTC_XLINE5
PTC_XLINE6	PD9	IRQ/GPIO	9	10	SPI_SS_B/GPIO	PD10	PTC_XLINE7
–	–	TWI_SDA	11	12	TWI_SCL	PD31	GPIO
–	–	UART_RX	13	14	UART_TX	–	–
GPIO	PB25	SPI_SS_A	15	16	SPI_MOSI	–	–
–	–	SPI_MISO	17	18	SPI_SCK	–	–
GROUND	–	GND	19	20	VCC 3V3	–	3.3V Supply

3.5.4 Miscellaneous PIOB[0-7]

PIOs PB00 to PB07 are available on connector J13 and can be used as GPIO pins. Each of these can be configured as an input or output pin according to the PIO peripheral functions.

Figure 3-51. PIOs PB[0-7] Connector

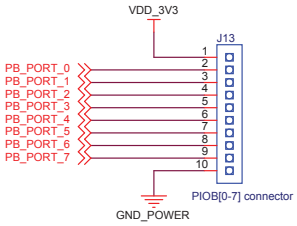
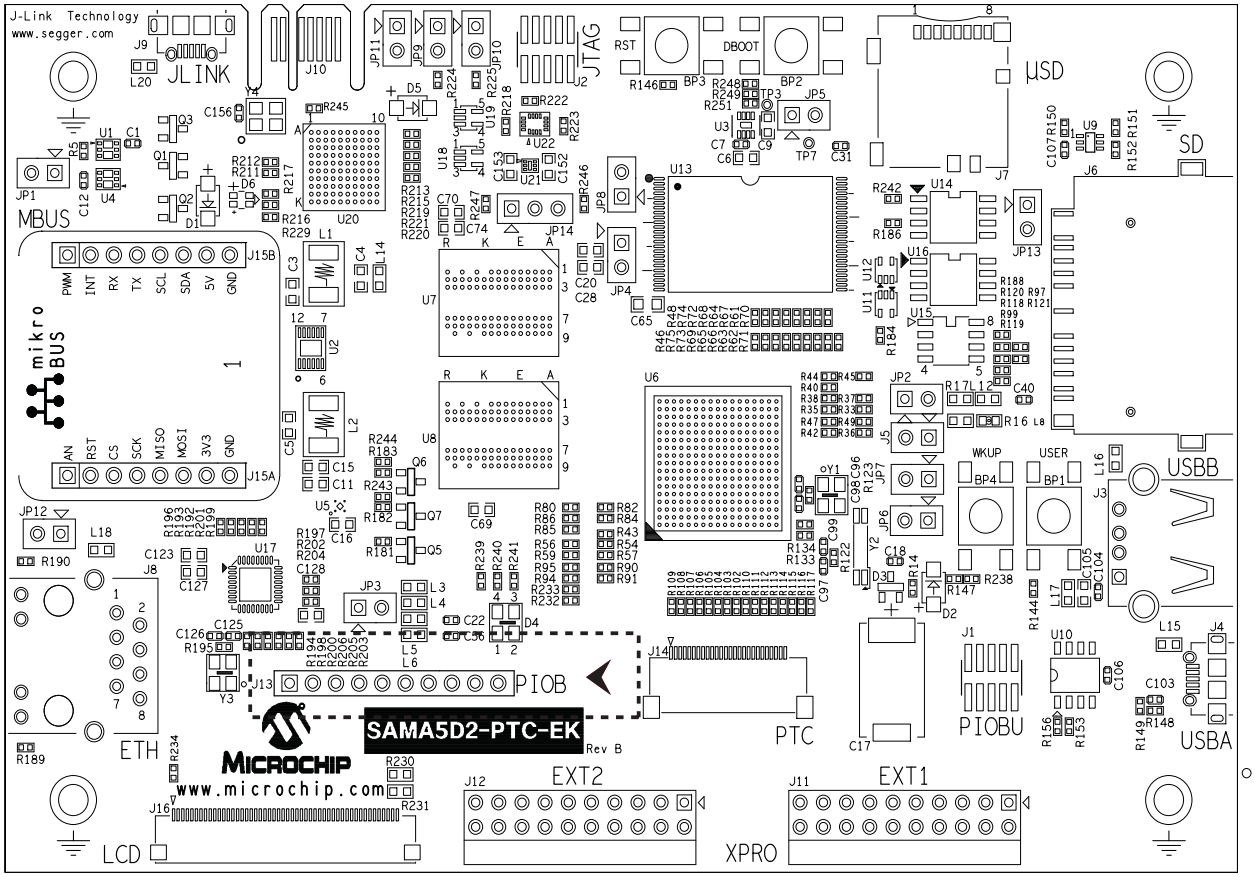


Figure 3-52. PIOB[0-7] Connector J13 Location



The table below describes the pin assignment of PIOs PB[0-7] connector J13.

Table 3-24. PIOs PB[0-7] Connector J13 Pin Assignment

Pin No	PIO	Mnemonic	Shared	Signal Description
1	_	VDD_3V3	_	Main 3.3V
2	PB0	GPIO	NAND Flash	PIO port B
3	PB1	GPIO	NAND Flash	PIO port B
4	PB2	GPIO	NAND Flash	PIO port B
5	PB3	GPIO	_	PIO port B
6	PB4	GPIO	_	PIO port B
7	PB5	GPIO	_	PIO port B
8	PB6	GPIO	LED_BLUE	PIO port B
9	PB7	GPIO	_	PIO port B
10	_	GND	_	Common ground

4. Installation and Operation

4.1 System and Configuration Requirements

The SAMA5D2-PTC-EK requires the following:

- Personal Computer
- USB cable

4.2 Board Setup

Follow these steps before using the SAMA5D2-PTC-EK:

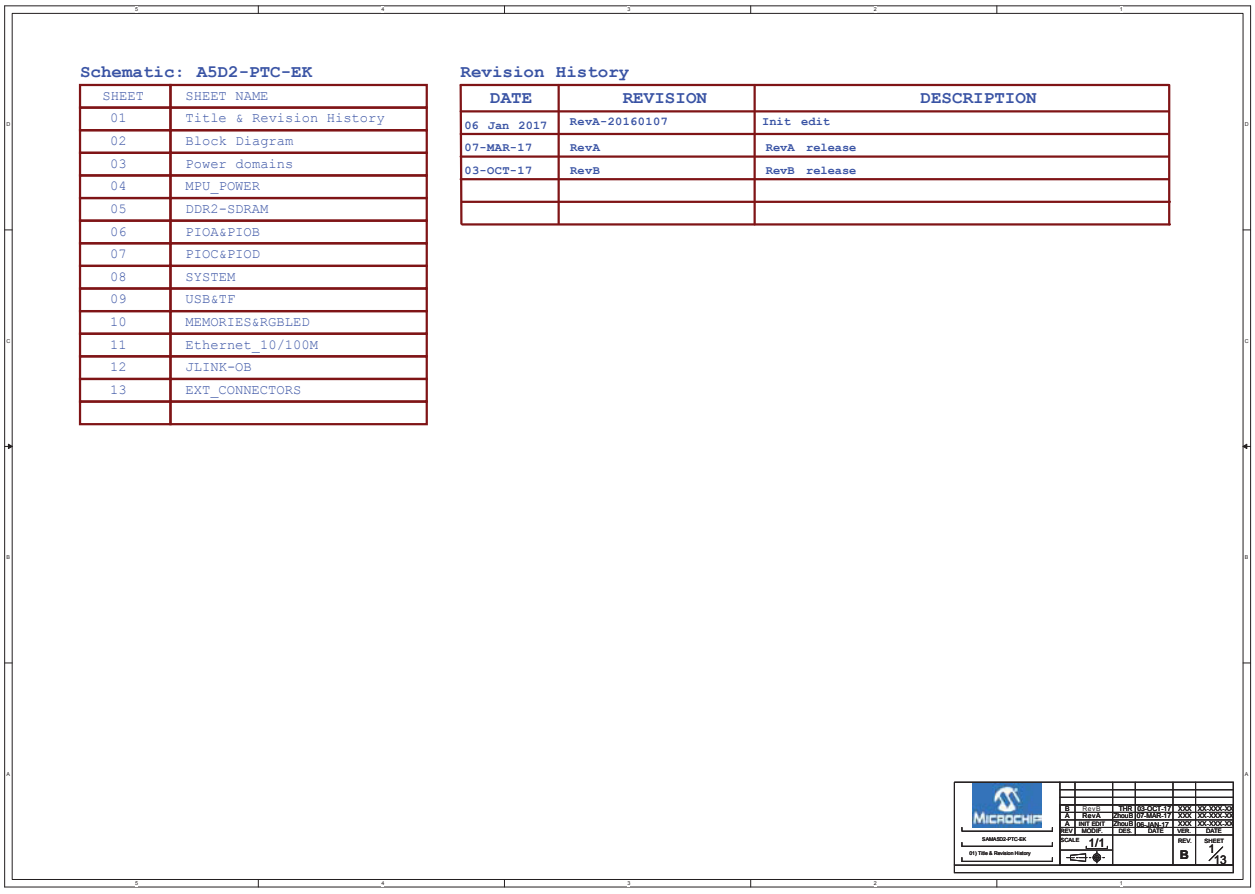
1. Unpack the board, taking care to avoid electrostatic discharge.
2. Check the default jumper settings.
3. Connect the USB Micro-AB cable to connector J9.
4. Connect the other end of the cable to a free port of your PC.
5. Open a terminal (console 115200, N, 8, 1) on your Personal Computer.
6. Reset the board. A startup message appears on the console.

5. Appendix A. Schematics and Layouts

This appendix contains the following schematics and layouts for the SAMA5D2-PTC-EK board:

- Title and Revision History
- Block Diagram
- Power Domains
- MPU Power
- DDR2-SDRAM
- PIOA & PIOB
- PIOC & PIOD
- System
- USB & TF
- Memories & RGB LED
- Ethernet 10/100M
- JLINK-OB
- EXT Connectors

Figure 5-1. Title and Revision History



Schematic: A5D2-PTC-EK

SHEET	SHEET NAME
01	Title & Revision History
02	Block Diagram
03	Power domains
04	MPU_POWER
05	DDR2-SDRAM
06	PIOA&PIOB
07	PIOC&PIOD
08	SYSTEM
09	USB&TF
10	MEMORIES&RGBLED
11	Ethernet_10/100M
12	JLINK-OB
13	EXT_CONNECTORS

Revision History

DATE	REVISION	DESCRIPTION
06 Jan 2017	RevA-20160107	Init edit
07-MAR-17	RevA	RevA release
03-OCT-17	RevB	RevB release

Figure 5-2. Block Diagram

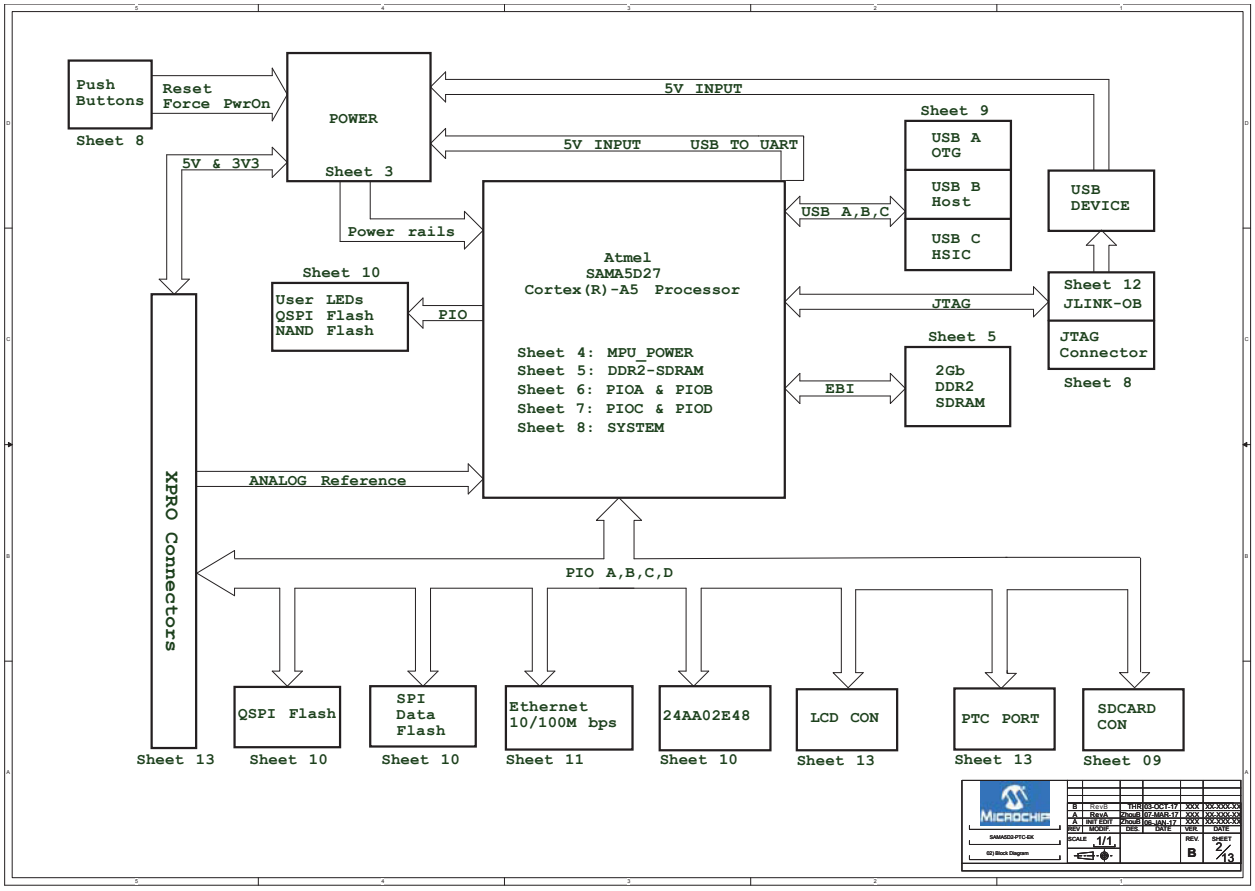


Figure 5-3. Power Domains

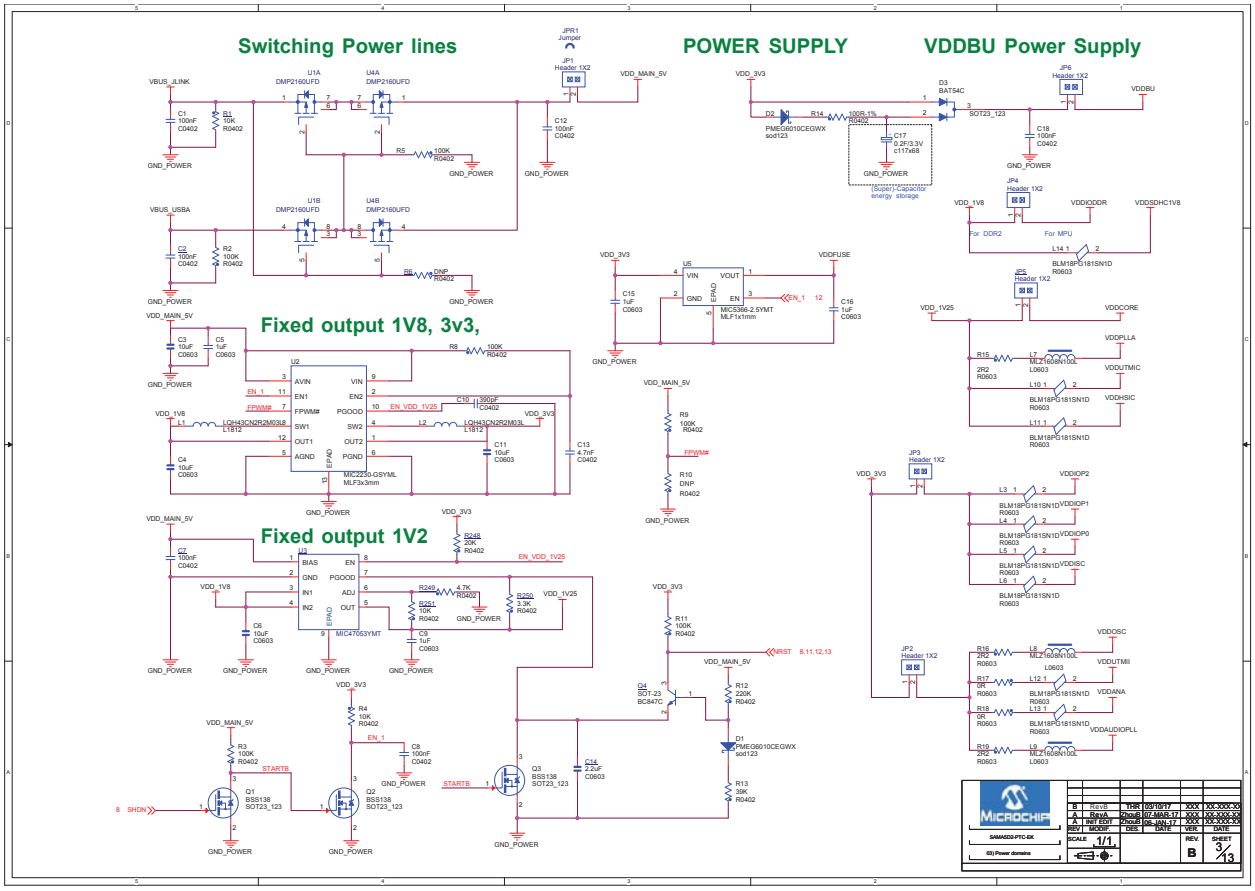


Figure 5-4. MPU Power

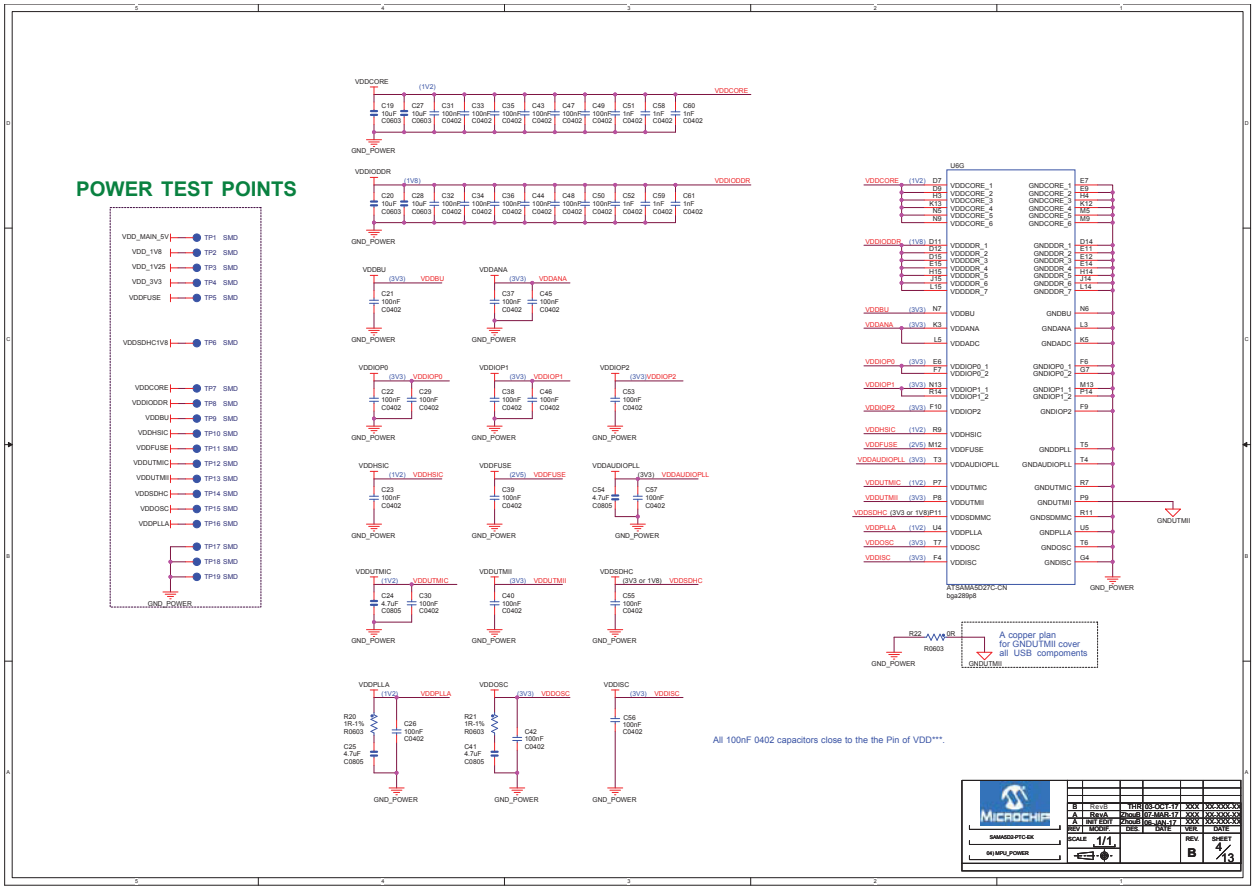


Figure 5-5. DDR2-SDRAM

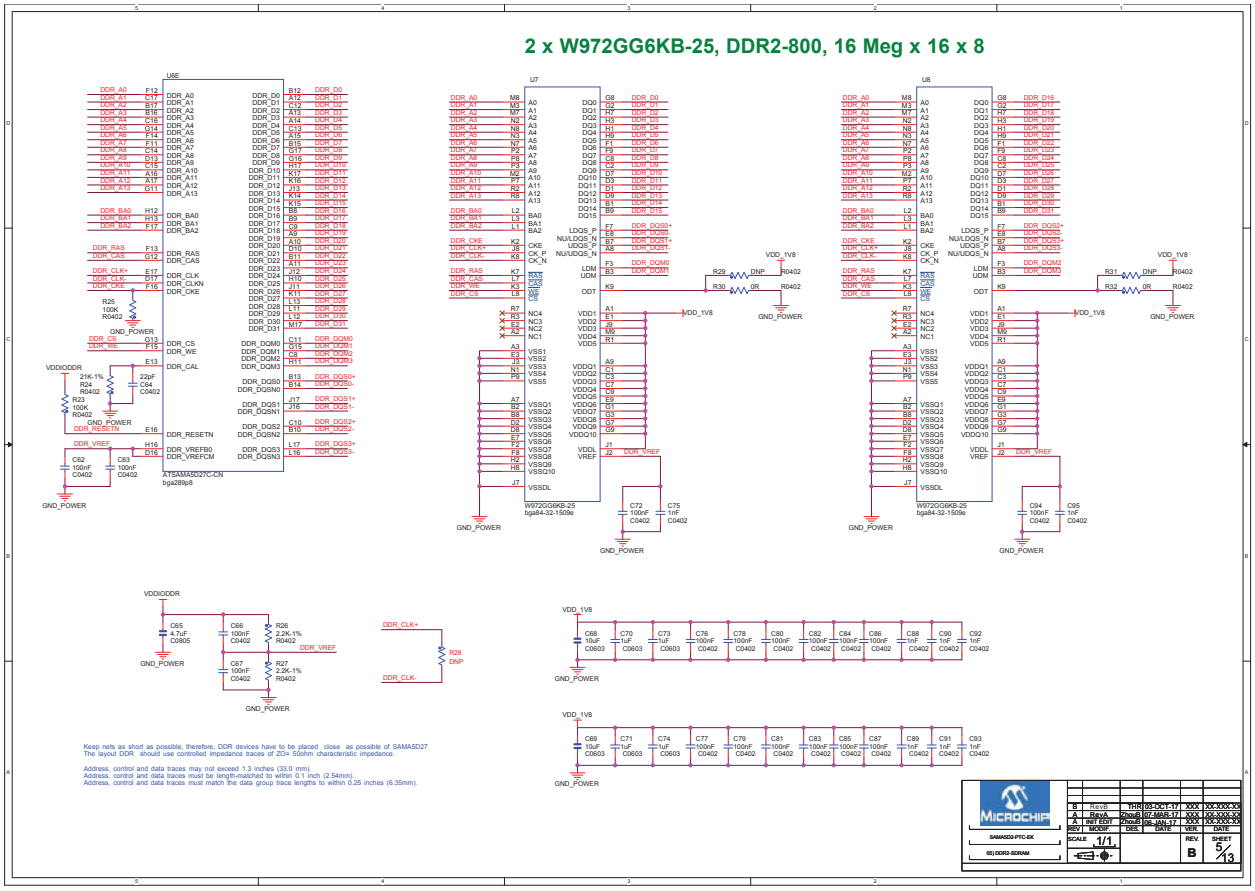


Figure 5-6. PIOA & PIOB

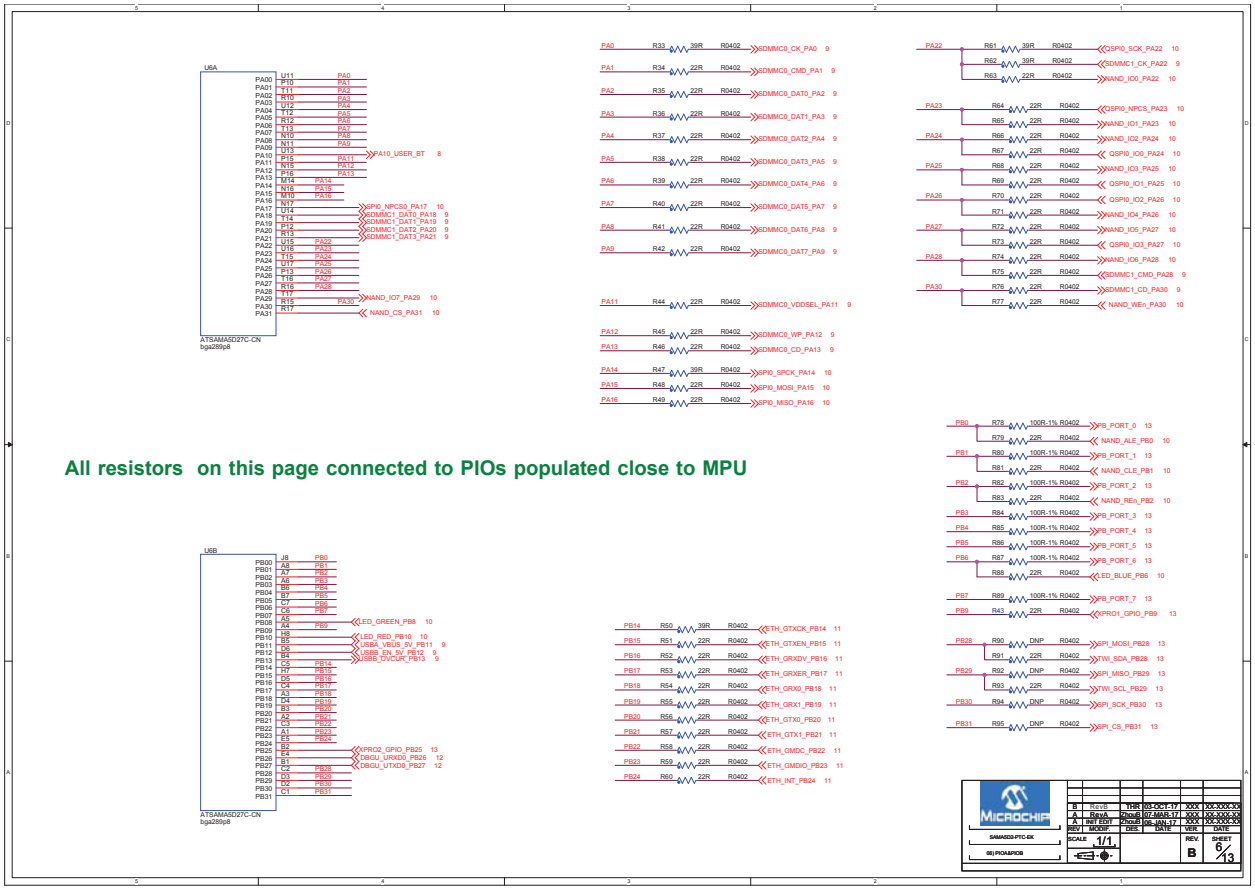


Figure 5-7. PIOC & PIOD

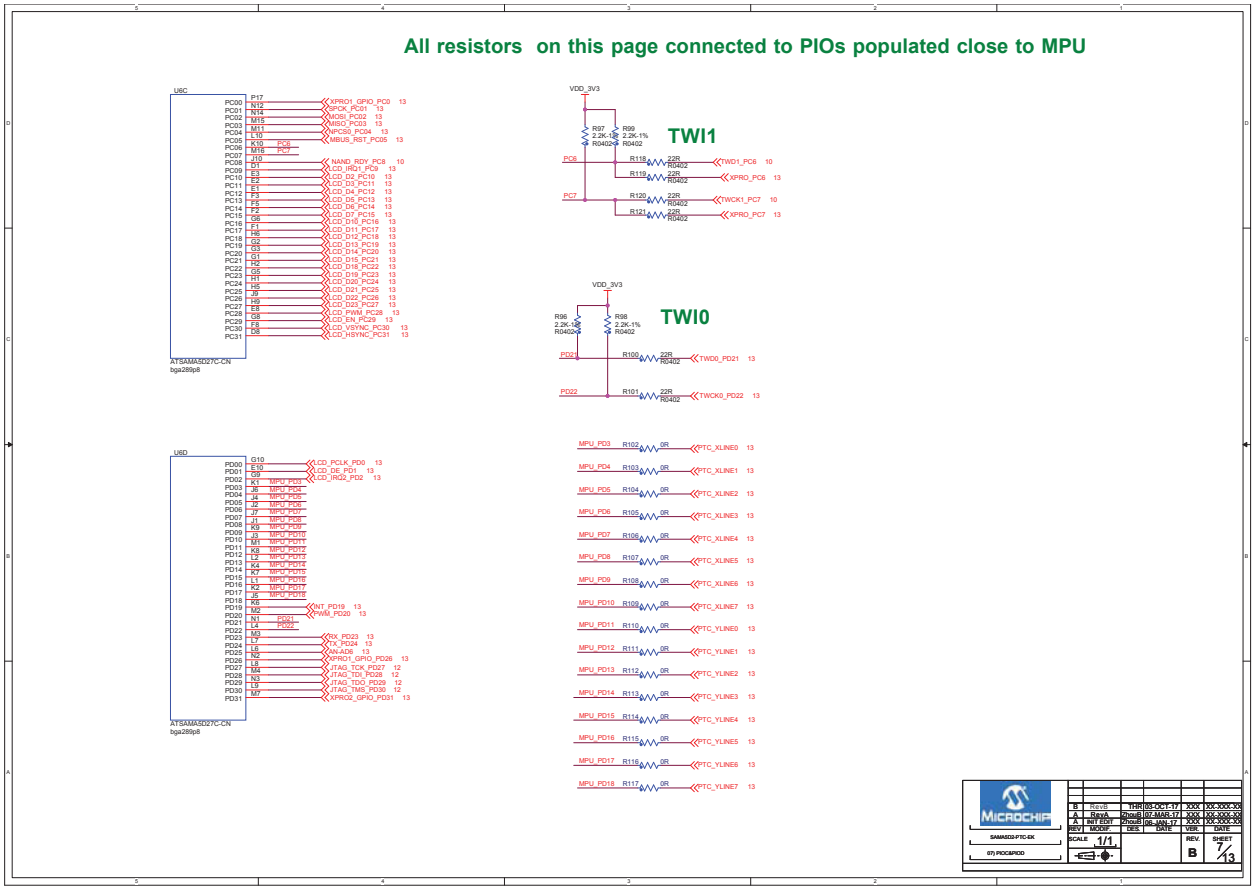


Figure 5-8. System

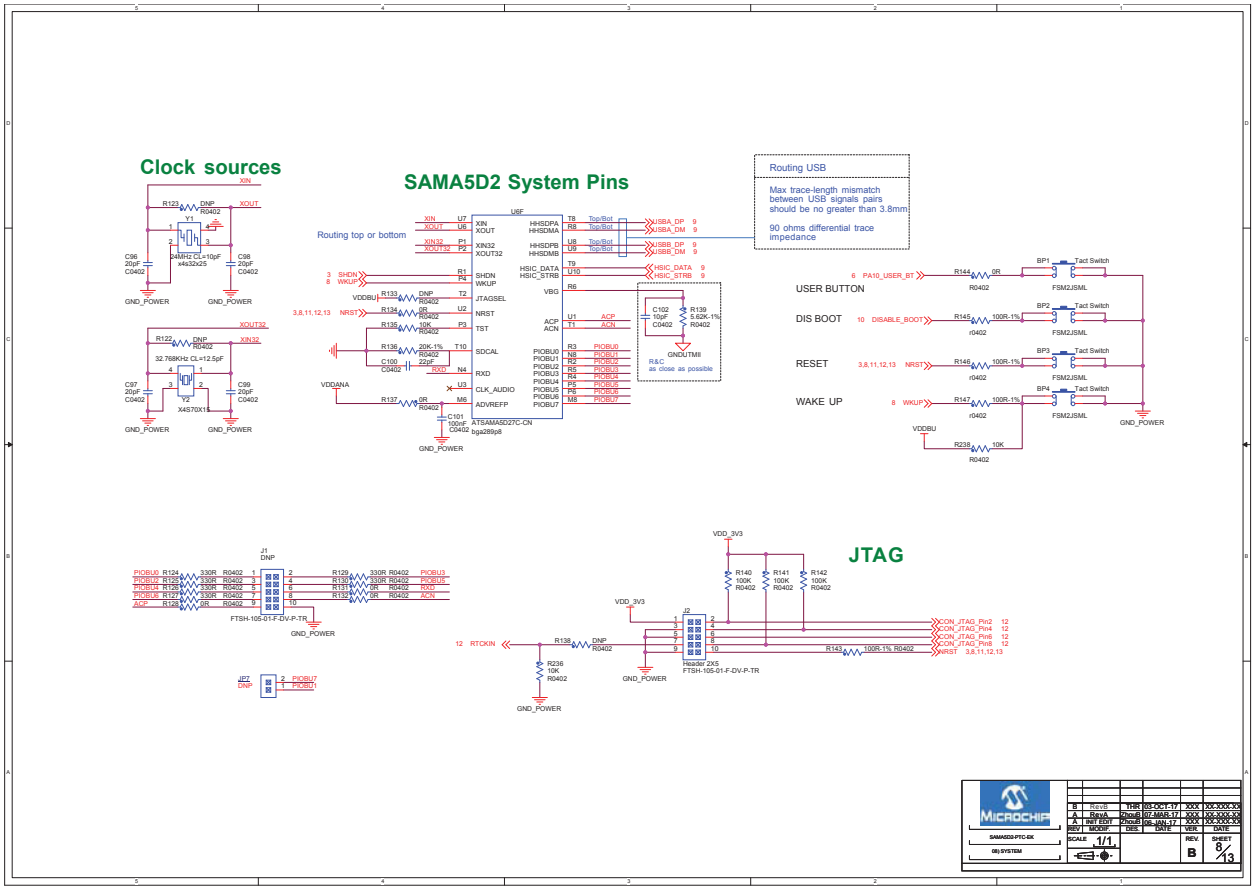


Figure 5-9. USB & TF

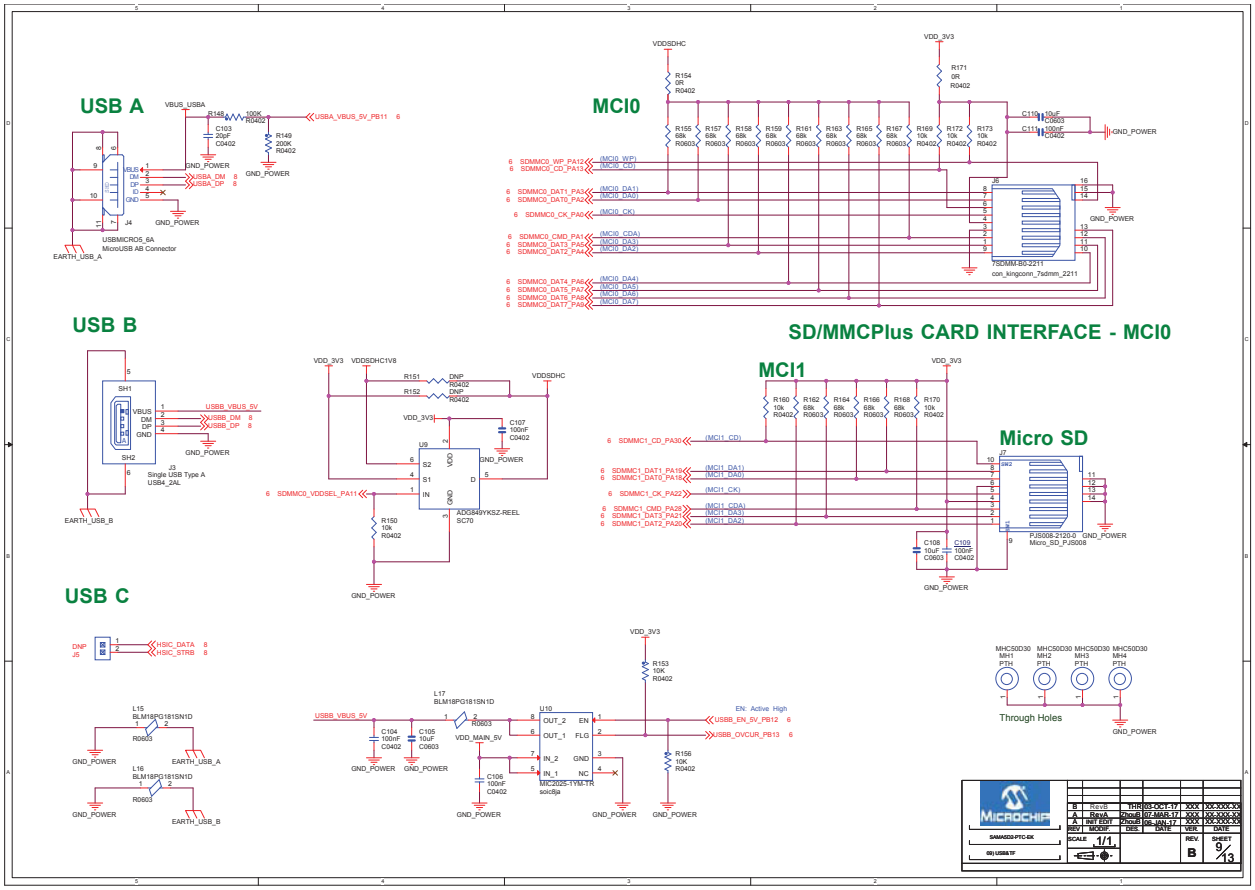


Figure 5-10. Memories & RGB LED

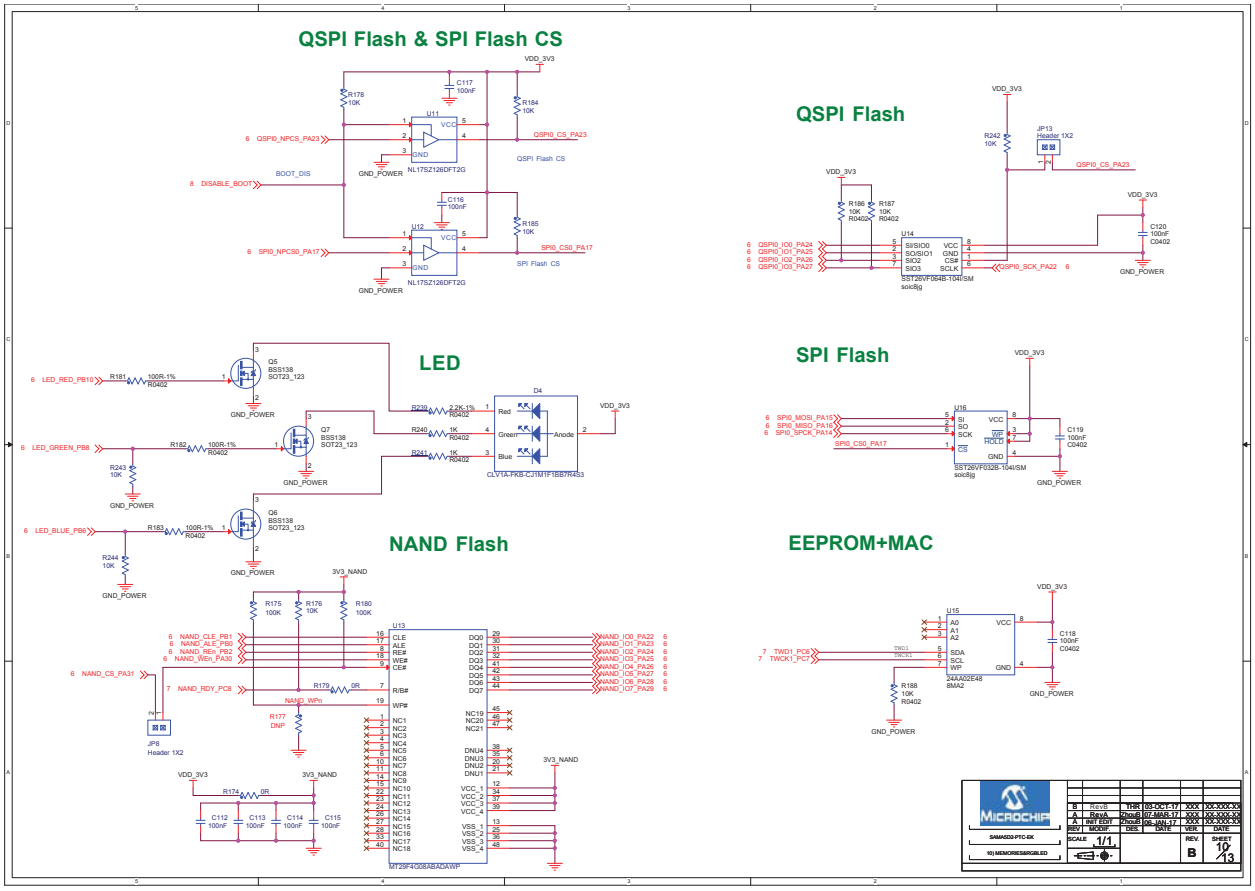


Figure 5-11. Ethernet 10/100M

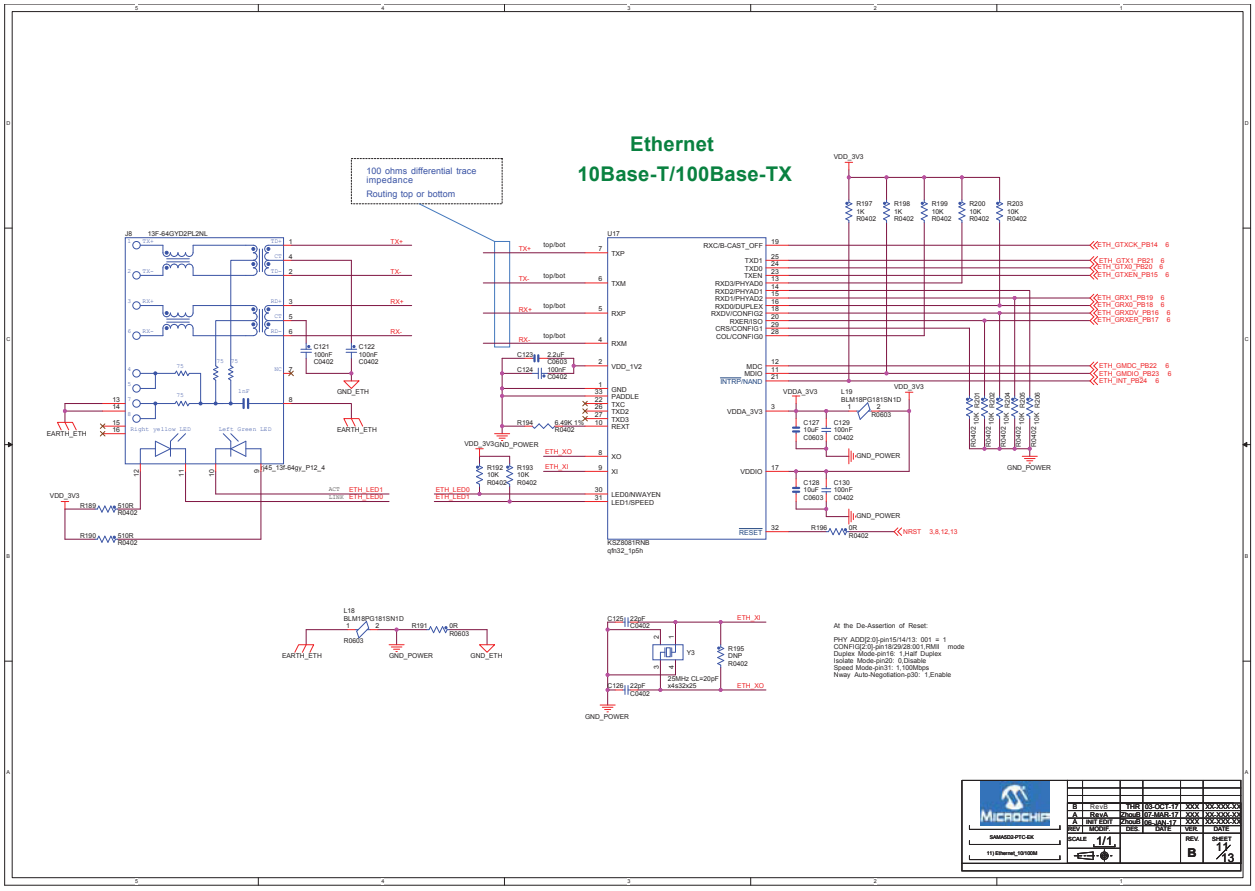


Figure 5-12. JLINK-OB

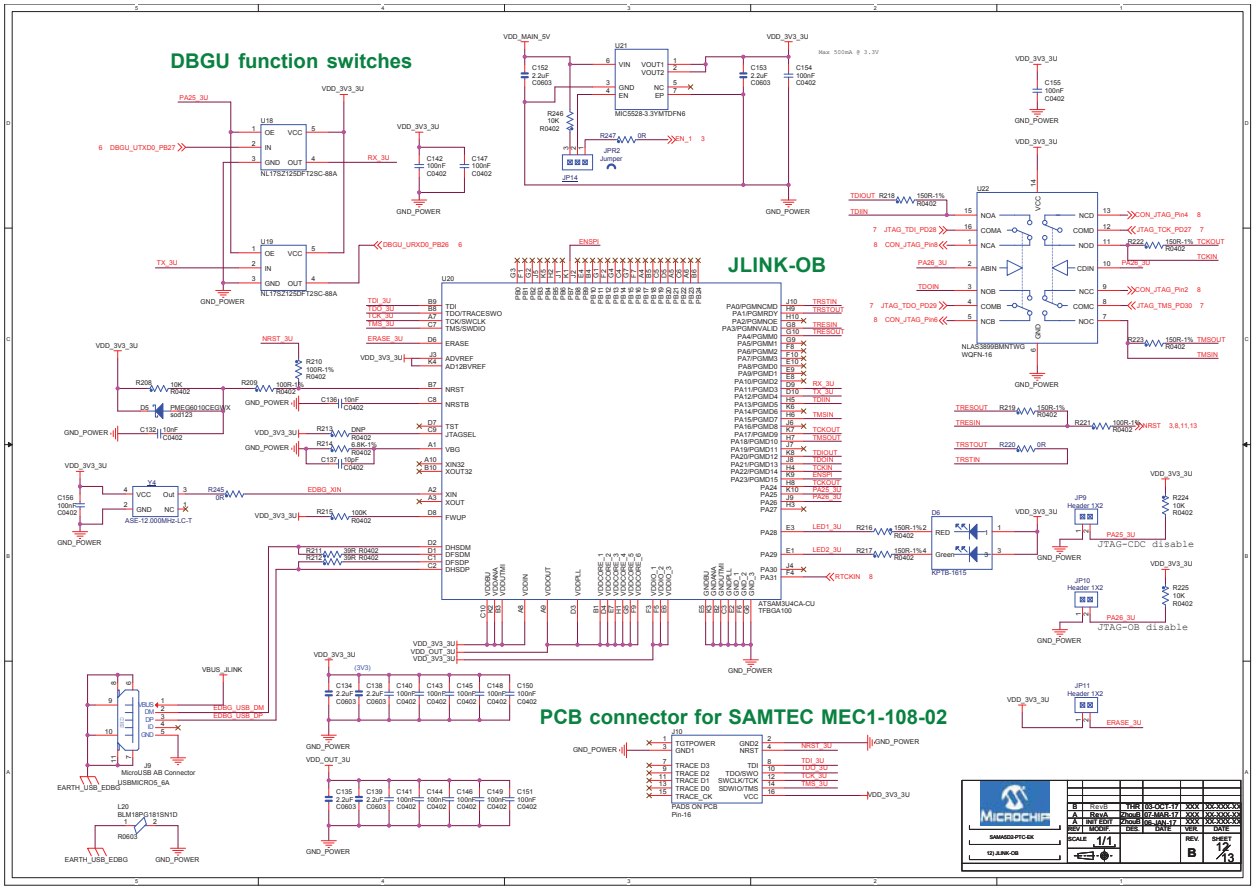
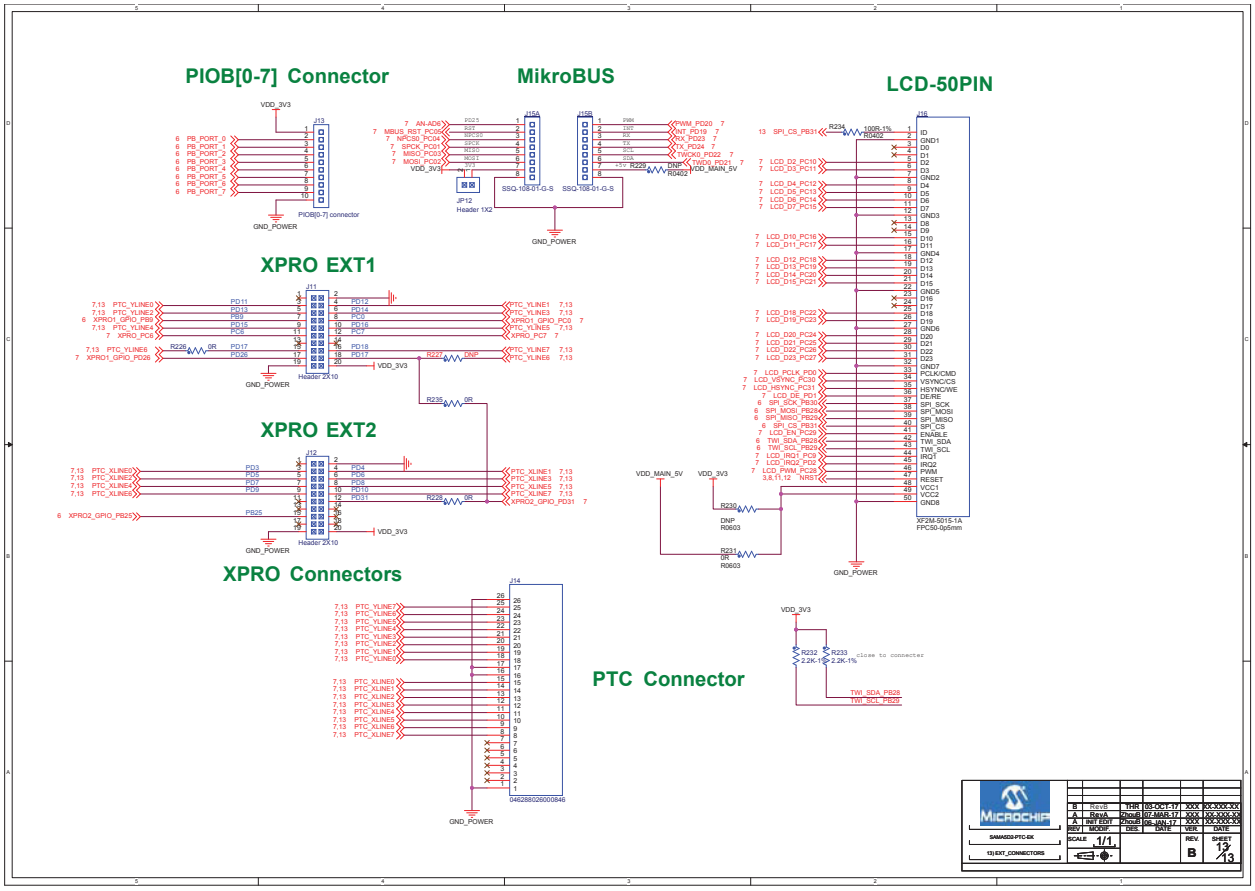


Figure 5-13. EXT Connectors



6. Revision History

6.1 Rev. A - 12/2017

This is the initial released version of this user's guide.

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