User's Guide

SLUUAU9A – December 2013 – Revised January 2014

Using the TPS92561 Off-Line Boost LED Driver

The TPS92561EVM is a 12-W maximum, 120-VAC non-isolated dimmable LED driver. The TPS92561EVM implements a dimming solution using the TPS92561 integrated circuit from Texas Instruments. This user's guide provides electrical specifications, performance data, typical characteristic curves, schematics, printed-circuit board layout, and a bill of materials.

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1 Introduction

The TPS92561EVM is a 12-W maximum, 120-VAC non-isolated dimmable LED driver whose form factor is intended for A-15, A-19, A-21, A-23, R-20, R-25, R-27, R-30, R-40, PS-25, PS-30, PS-35, BR-30, BR-38, BR-40, PAR-20, PAR-30, PAR-30L, G-25, G-30, G-40, and other LED bulbs.

2 Description

The TPS92561EVM implements a dimming solution using the TPS92561 integrated circuit from Texas Instruments. The TPS92561 is a boost controller for LED lighting applications utilizing high-voltage, low-current LEDs. The boost converter topology allows the creation of the smallest volume converter possible as well as enabling high efficiencies beyond 90%. The device incorporates a current sense comparator with a fixed offset enabling a simple hysteretic control scheme free of the loop compensation issues typically associated with a boost converter. Integrated overvoltage protection (OVP) and a VCC regulator further simplify the design procedure and reduce external component count.

2.1 Typical Applications

TRIAC-compatible LED lighting, including forward and reverse phase compatibility.

2.2 TPS92561 Features

- Simple hysteretic control
- Compact solution with small bill of material (BOM)
- High operating efficiency (typical 90% or higher)
- Low input current THD and high power factor solution
- Wide dimming range based on input voltage RMS value
- Compatible with forward, reverse and electronic dimmers
- Programmable output overvoltage protection (OVP)
- 8-pin MSOP PowerPAD™ package

3 Electrical Performance Specifications

Table 1 lists the electrical performance specifications of the TPS92561 device.

Table 1. TPS92561EVM-001 Boost Reference Design Electrical Performance Specifications(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
Input voltage range		90	120	135	V
Maximum input current				0.100	A
OUTPUT CHARACTERISTICS					
Output voltage, V_{OUT}	Output current changes with LED stack. Nominal output is 215 V, 50 mA (10.75 W)	200	215	250	V
Output voltage regulation	Line regulation: 110 V ≤ V_{IN} ≤ 130 V		±2.5%		
Output Current ripple	120-Hz LED ripple, typical with 215-V LED stack and 22-µF output energy storage capacitor		30		mApp
Ouput Current			45		mA
SYSTEMS CHARACTERISTICS					
Peak efficiency			92		%
Peak Power Factor			0.99		
Input current THD	Based on 12-W maximum		7.3		%
Operating temperature			25	125	ºC

(1) All performance results are for this design configuration only. Many opportunities exist to balance one performance factor for another in this design.

4 Schematic

Figure 1 shows the EVM schematic, and Figure 2 shows suggested dimming connections.

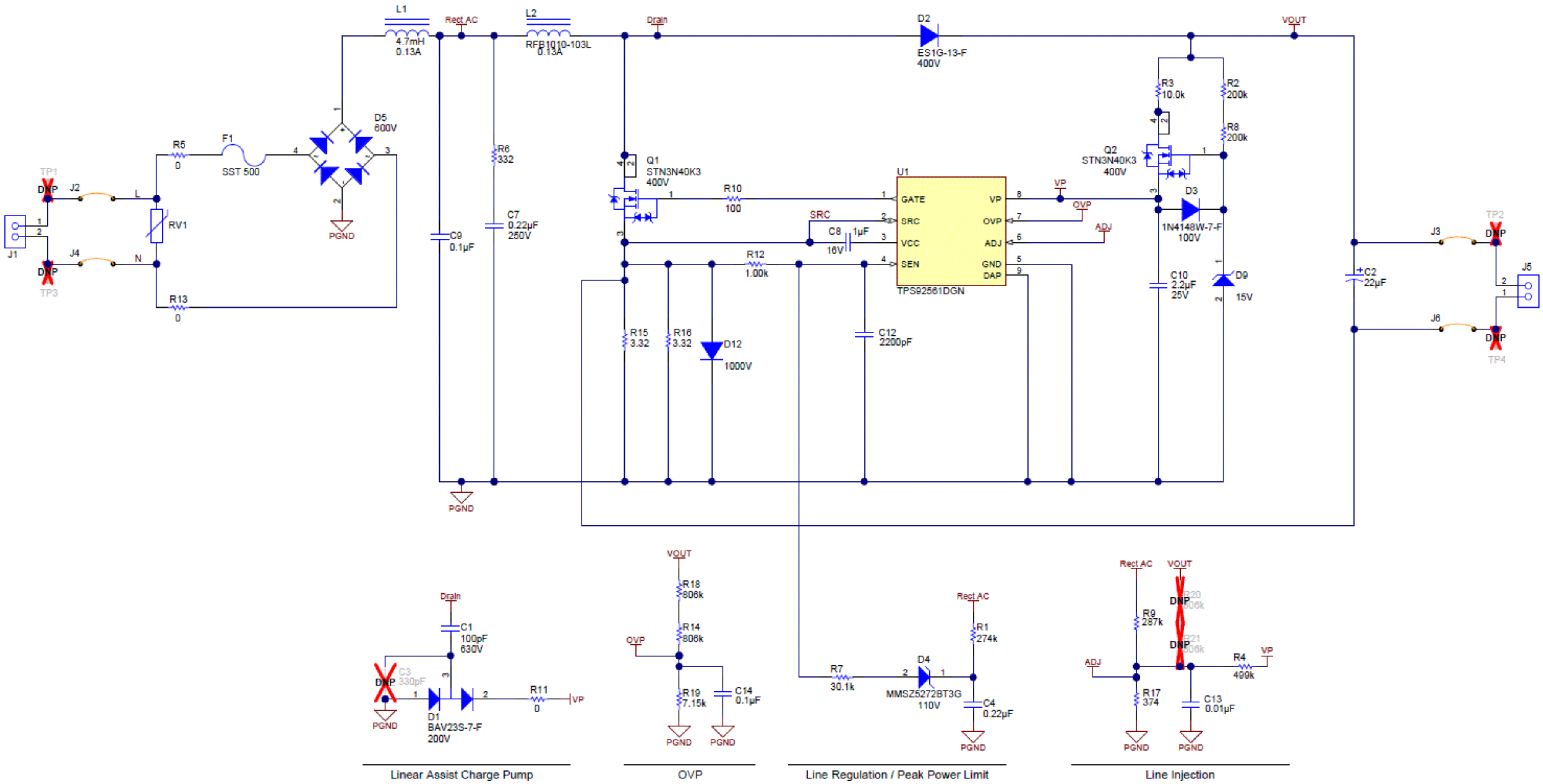


Figure 1. TPS92561 Boost Schematic

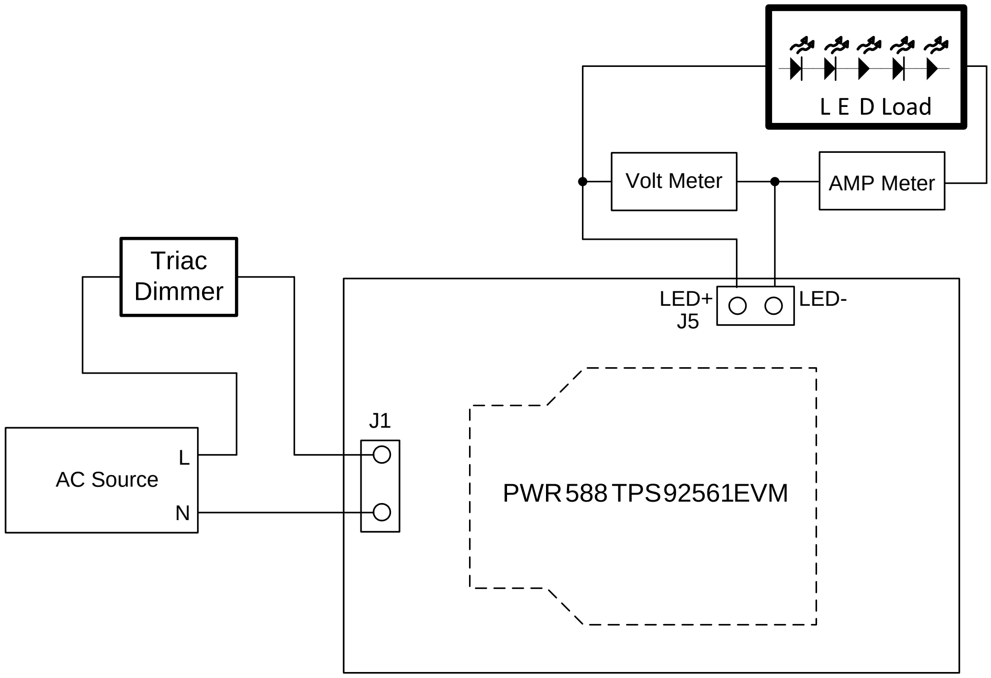


Figure 2. Dimming Wiring Diagram

5 Performance Data and Typical Characteristic Curves

Conditions: 215-V LED stack voltage; approximately 50-mA LED current; approximately 10-W boost LED driver

5.1 Efficiency

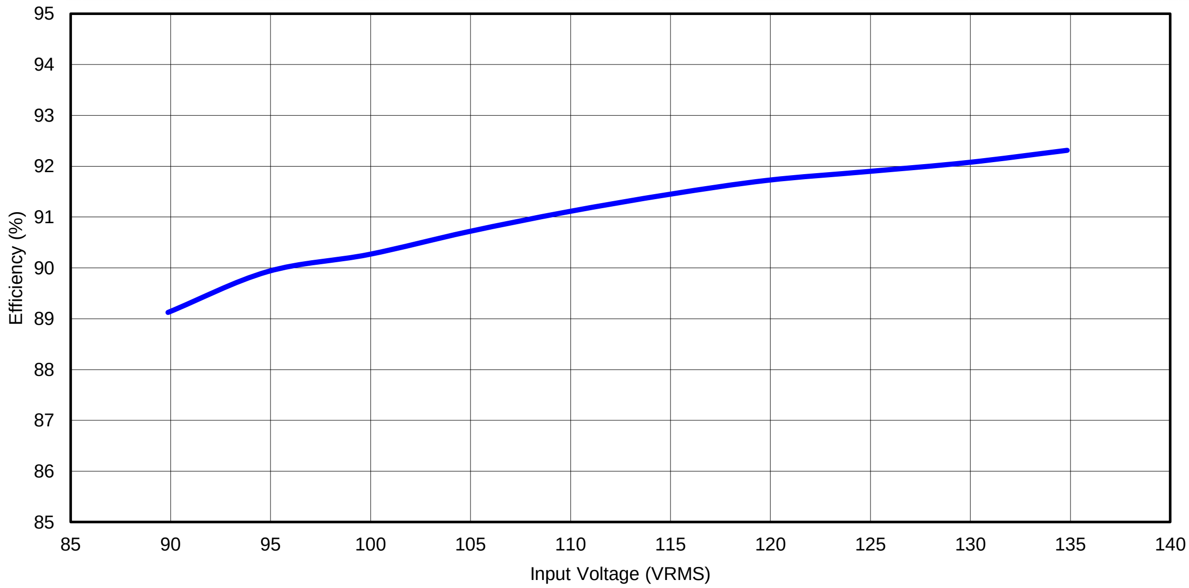


Figure 3. TPS92561 Boost Efficiency

5.2 Power Factor

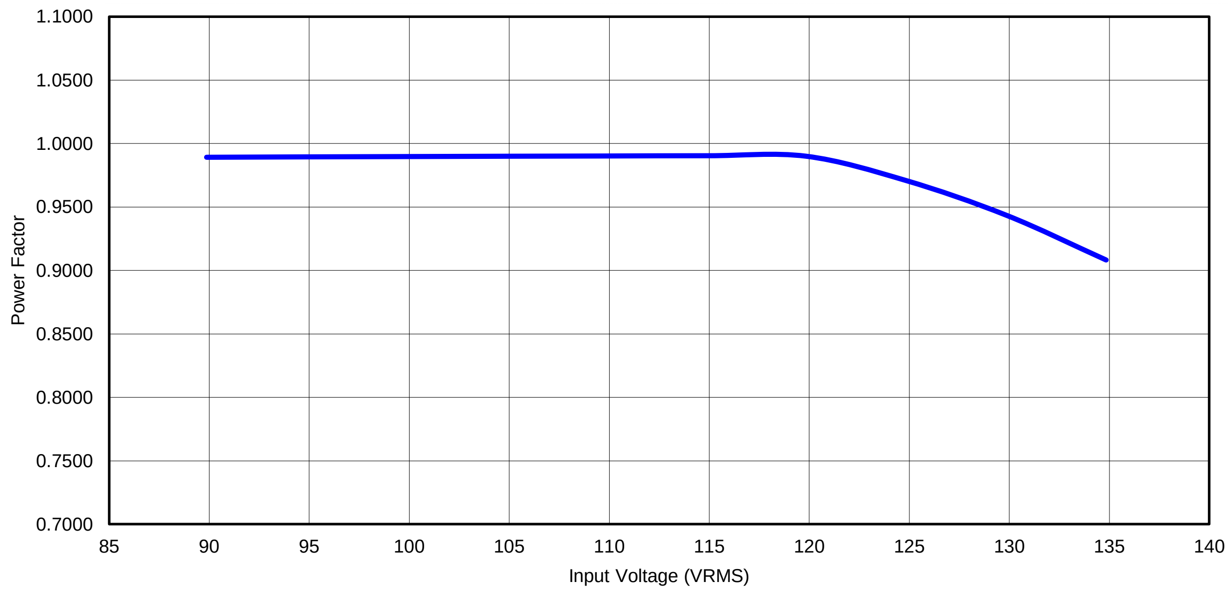


Figure 4. TPS92561 Boost Input Power Factor

5.3 Input Current Total Harmonic Distortion

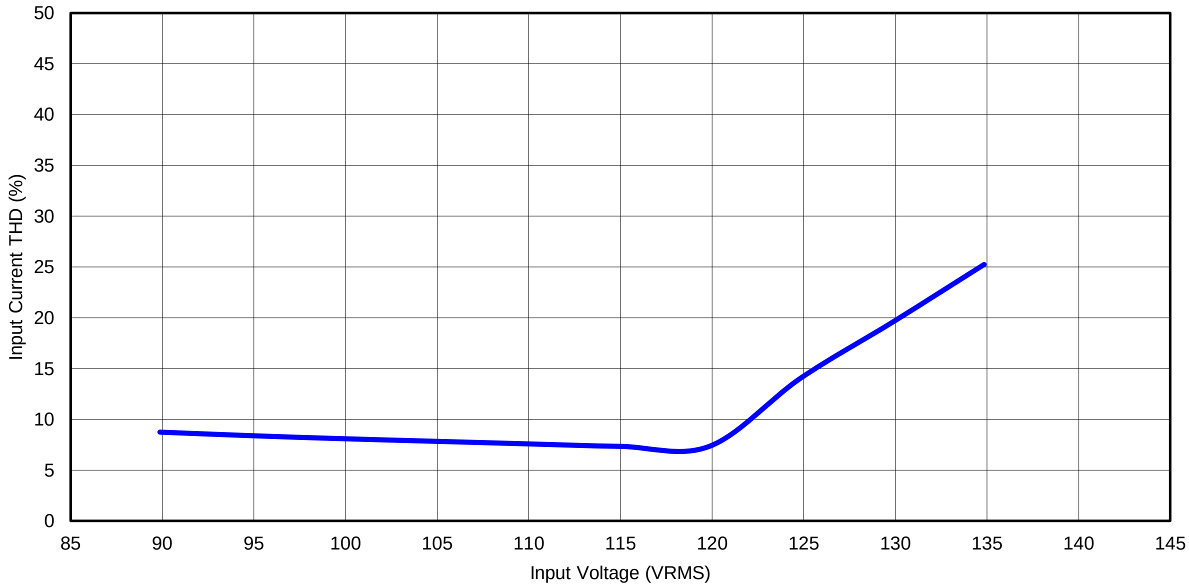
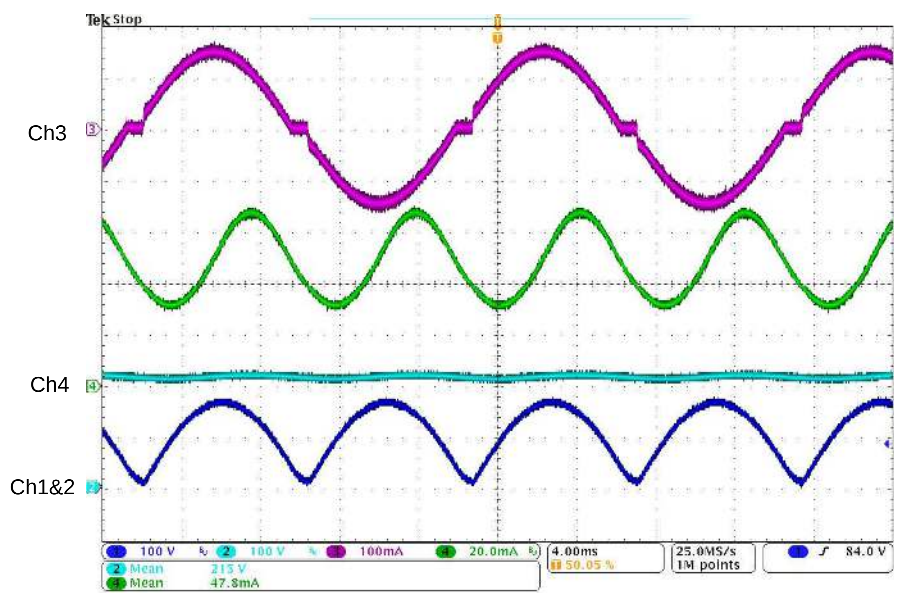


Figure 5. TPS92561 Boost Input Current Total Harmonic Distortion

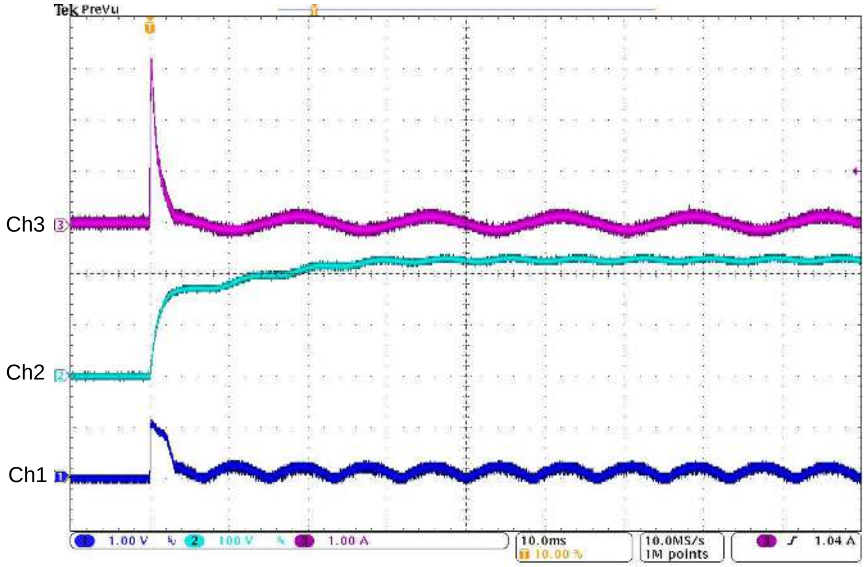
5.4 Output Ripple



Ch1: Rectified Input Voltage (100V/div); Ch2: Output Voltage (100V/div);
Ch3: Input Current (100mA/div); Ch4: LED Current (20mA/div); Time (4ms/div)

Figure 6. Output Ripple (V_{OUT} = 215 V, I_{OUT} = 50 mA, THD 7.5%)

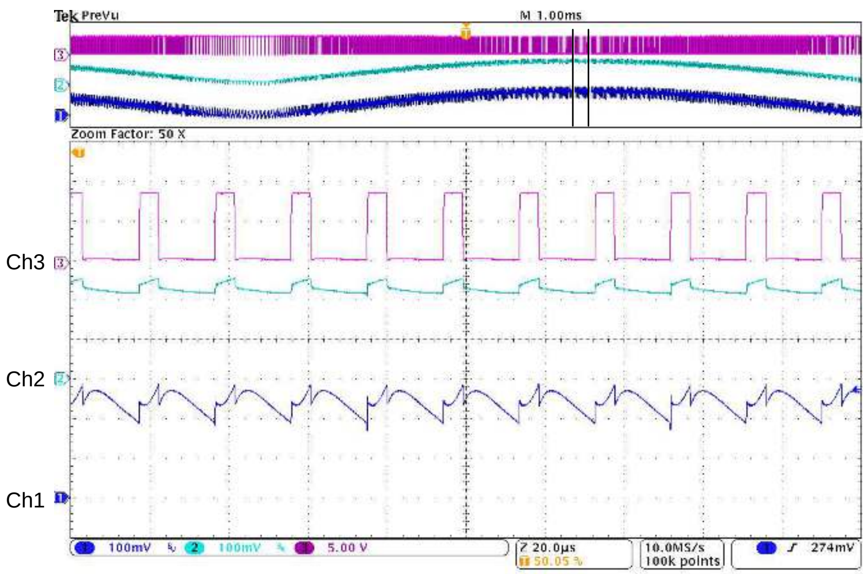
5.5 Turn On Waveform



Ch1: VSEN Voltage (1V/div); Ch2: Output Voltage (100V/div);
Ch3: Input Current (100mA/div); Time (10ms/div)

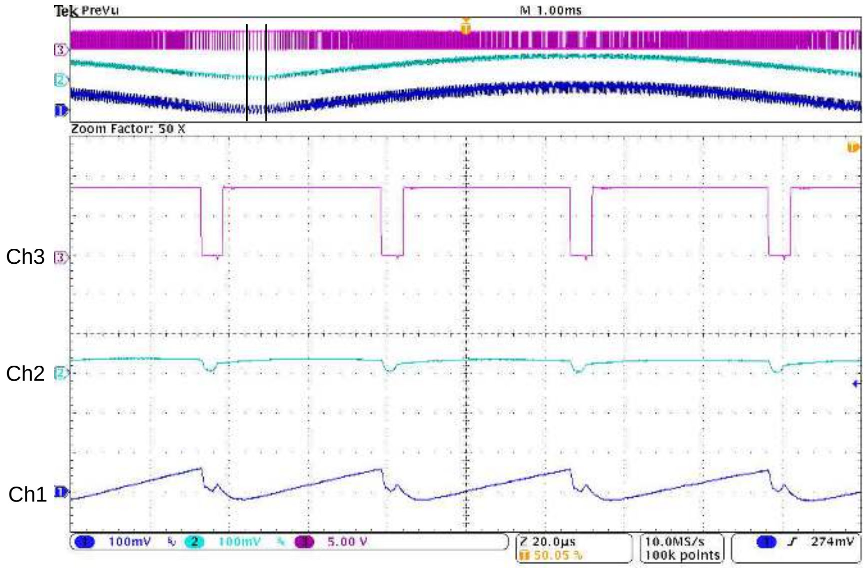
Figure 7. Turn On Waveform, Turn-On Time ≡ 20 ms

5.6 Hysteretic Boost PFC Operation



Ch1: VSEN Voltage (100mV/div); Ch2: VADJ Voltage (100mV/div);
Ch3: GATE Voltage (5V/div); Time (20µs/div)

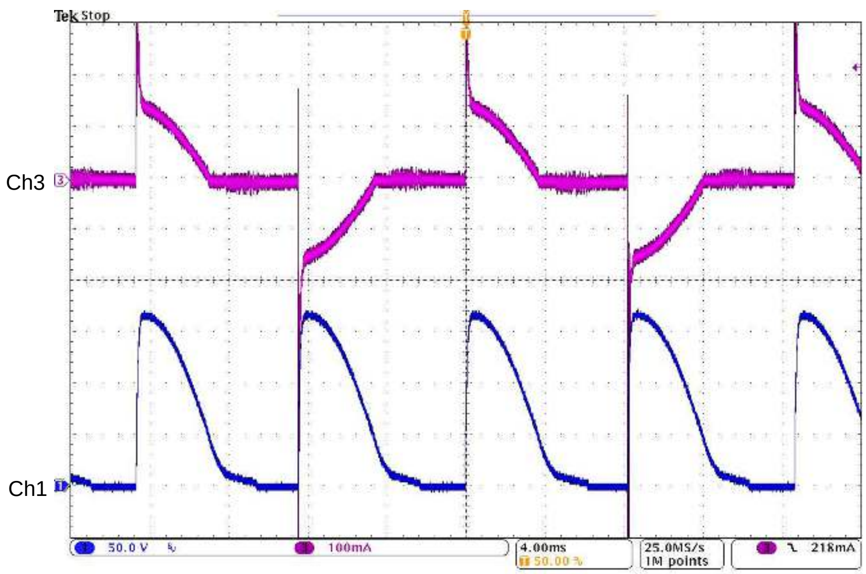
Figure 8. Hysteretic Control of Boost Inductor Current (at Maximum V_{ADJ} Voltage)



Ch1: VSEN Voltage (100mV/div); Ch2: VADJ Voltage (100mV/div);
Ch3: GATE Voltage (5V/div); Time (20µs/div)

Figure 9. Hysteretic Control of Boost Inductor Current (at Minimum V_{ADJ} Voltage)

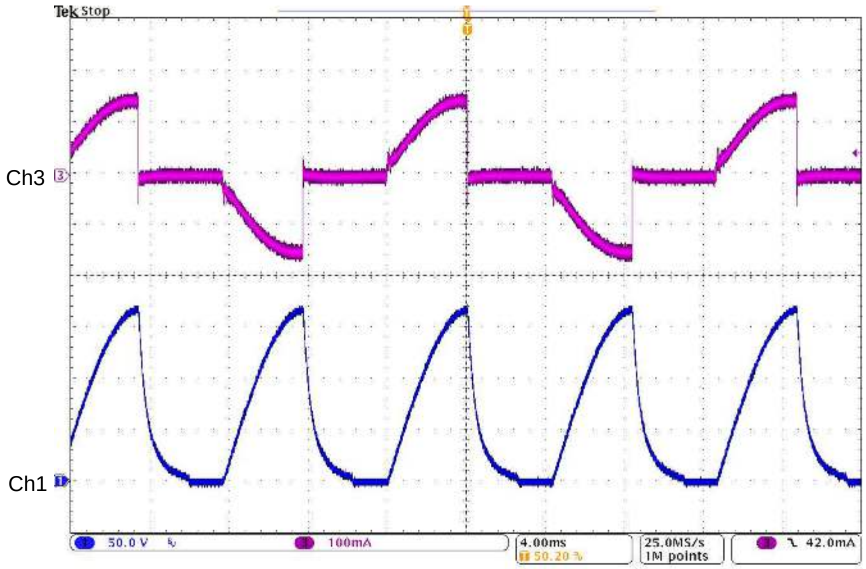
5.7 Dimming – Leviton 6683 Forward Phase Dimmer



Ch1: Rectified Input Voltage (50V/div); Ch3: Input Current (100mA/div);
Time (4ms/div)

Figure 10. Leviton Forward Phase Dimmer (90° Conduction Angle)

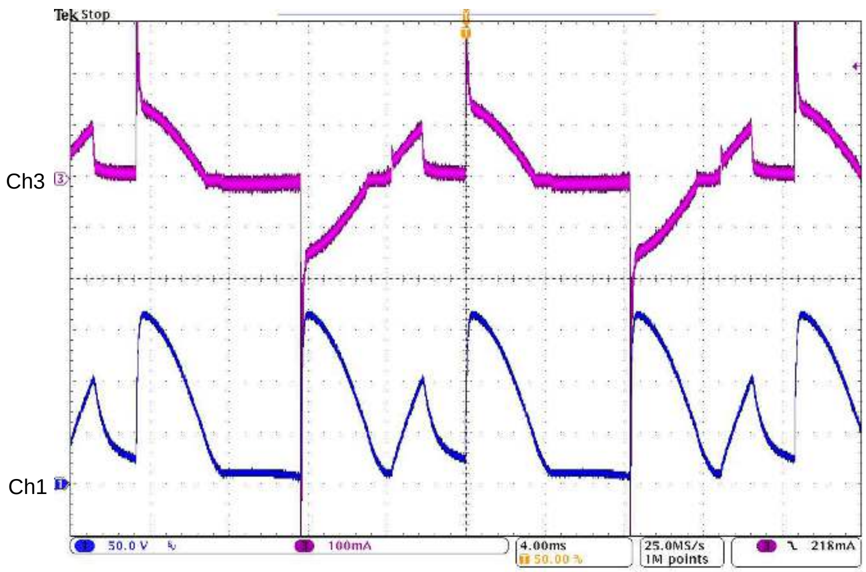
5.8 Dimming – Lutron Diva 303P Reverse Phase Dimmer



Ch1: Rectified Input Voltage (50V/div); Ch3: Input Current (100mA/div);
Time (4ms/div)

Figure 11. Lutron Reverse Phase Dimmer (90° Conduction Angle)

5.9 Dimming – Lutron Maestro MAW-600H-LA Electronic Dimmer



Ch1: Rectified Input Voltage (50V/div); Ch3: Input Current (100mA/div);
Time (4ms/div)

Figure 12. Lutron Forward Phase Electronic Dimmer (90° Conduction Angle)

5.10 Dimming – NEMA SSL-6 Compliance

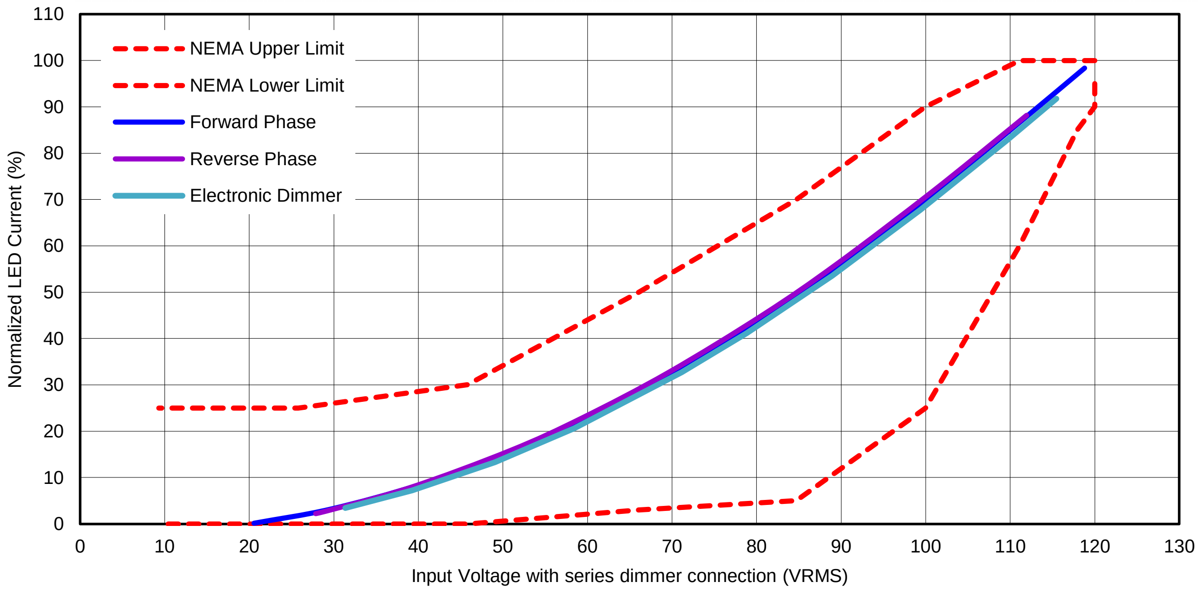
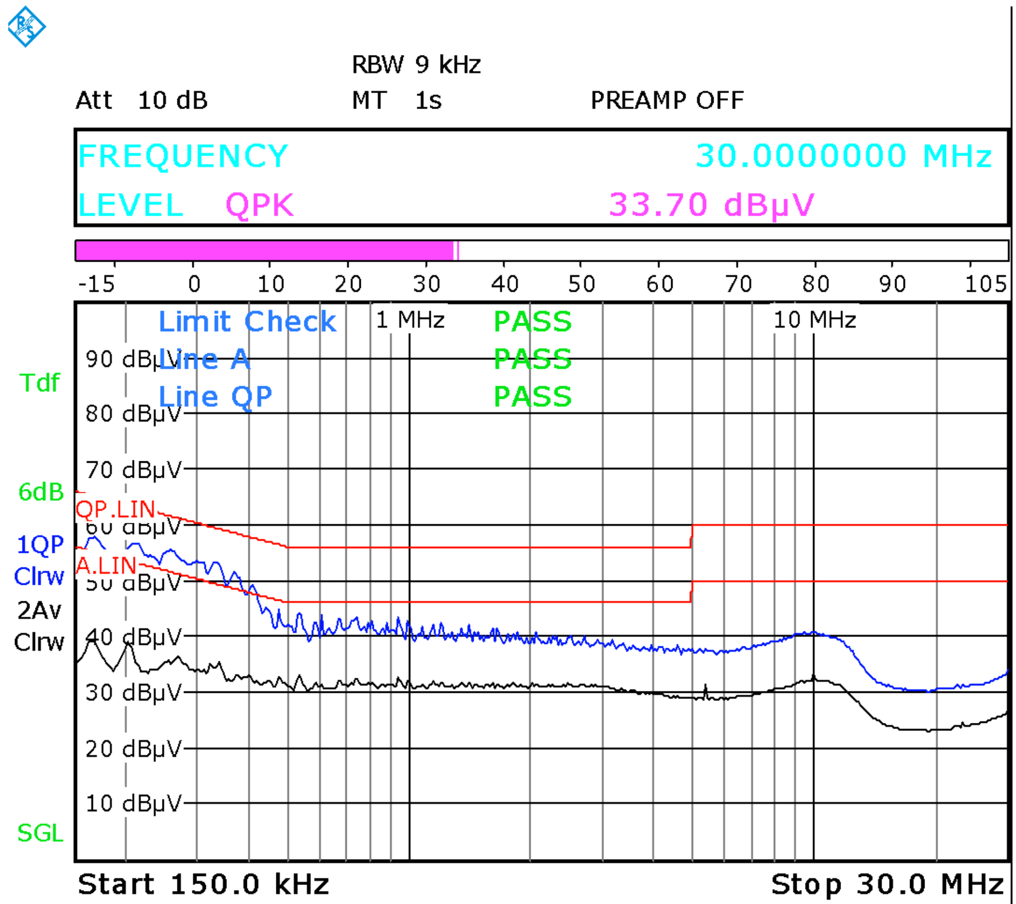


Figure 13. NEMA SSL-6 Compliance Data Based on Forward Phase – Leviton 6683, Reverse Phase Dimmer – Lutron Diva 303P, and Electronic Dimmer - Lutron Maestro MAW-600H-LA Dimmer

5.11 EMI Scan



Blue Trace: Quasi-Peak, Black Trace: Average

Figure 14. Conducted EMI Scan

NOTE: When using unshielded inductors, it is important that the devices sit in perpendicular planes. If the input filter inductors are not positioned at right angles, conducted emissions increase.

5.12 Radiated EMI

Radiated EMI was recorded using this EVM with the following addition: R5 and R13 where replaced with ferrite beads from Laird: HZ1206C202R-10.

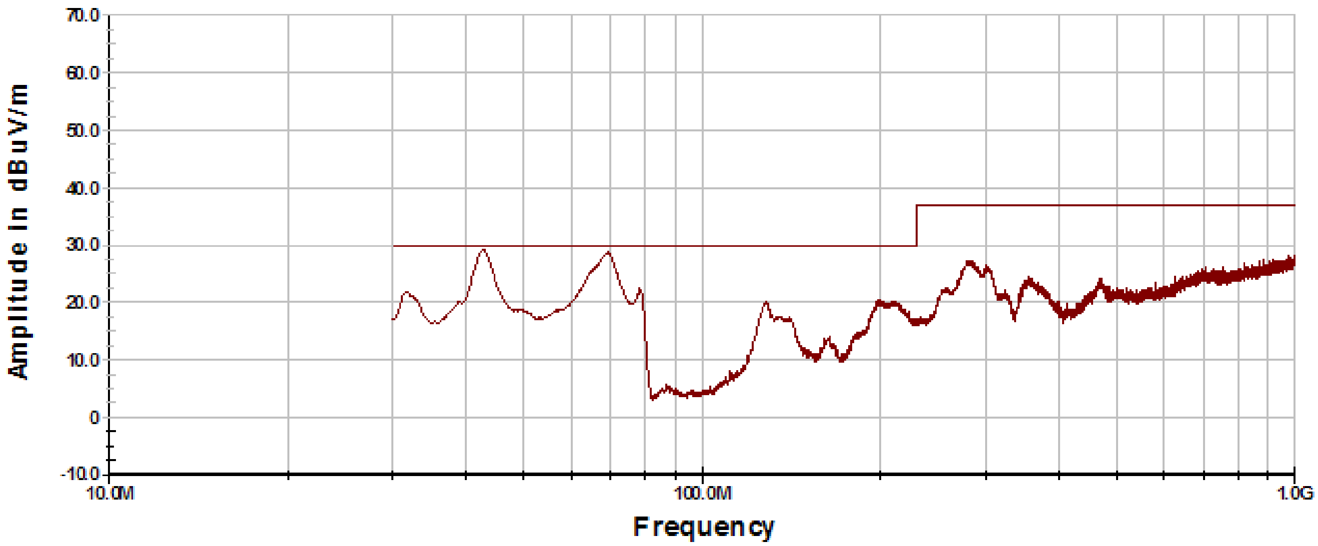


Figure 15. Amplitude vs Frequency, R10 = 100 Ω and C9 = 0.1 µF

5.13 Dimmer Testing

Table 2. Dimmer Testing

Conditions: 120-VAC, 215-V LED stack				
MANUFACTURER	**SERIES**	**PART NUMBER**	**FLICKER-FREE STEADY STATE**	
			1 Lamp	3 Lamps
Lutron	Maestro Duo	MAW-600H-LA	y	y
Lutron	Skylark Contour	CT-600PR-LA	y	y
Leviton	Decora	RPI06	y	y
Lutron	Skylark Contour	CTCL-153PDH	y	y
Leviton	SureSlide	6631	y	y
Leviton	Trimatron	6683	y	y
Lutron	Diva	DV-600PR-LA	y	y
Lutron	Diva	DVELV-303P	y	y
Lutron	Skylark	S-600PR-WH	y	y
Lutron	Toggler	TG-10PR-WH	y	y
Lutron	Toggler CFL/LED	TGCL-153PH-WA	y	y
Lutron	Toggler	TG-603PNL	y	y
Lutron	Diva	DVW-603PGH-WH	y	y
Lutron	Diva CFL/LED	DVWCL-153PH-LA	y	y
Lutron	Ariadni	AY-600P	y	y
Lutron	Nova	NTLV-600	y	y
Lutron	Lyneo Lx	LXLV-600PL-WH	y	y
Lutron	Diva	DVPDC-203P-IVN	y	y
Lutron	Nova	NLV-600-IV	y	y
Lutron	Skylark	SLV-600P	y	y
Lutron	Qoto	Q600P	y	y
Lutron	Ariadni CFL/LED	AYCL-153P-WH	y	y
Leviton	Trimatron	6684	y	y
Leviton	Electro-Mechanical	6161	y	y
Lutron	Ceana	CN-603P-AL	y	y

6 Reference Design, Assembly Drawing, PCB Layout, and Bill of Materials

6.1 Reference Design, Assembly Drawing, and PCB Layout

See Figure 16 to Figure 18 for the reference design, assembly drawing, and PCB layout.

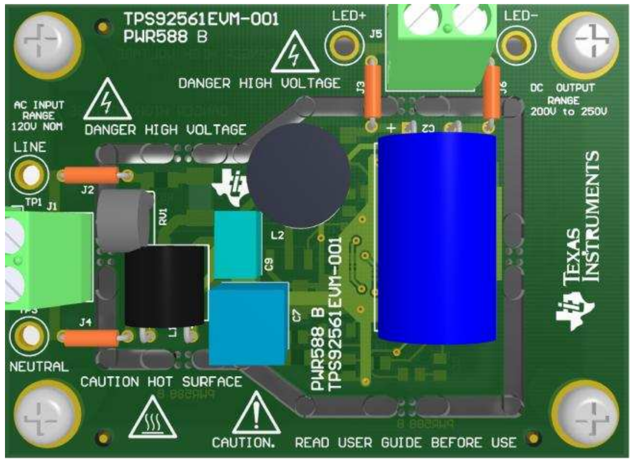


Figure 16. PCB 3D Top View

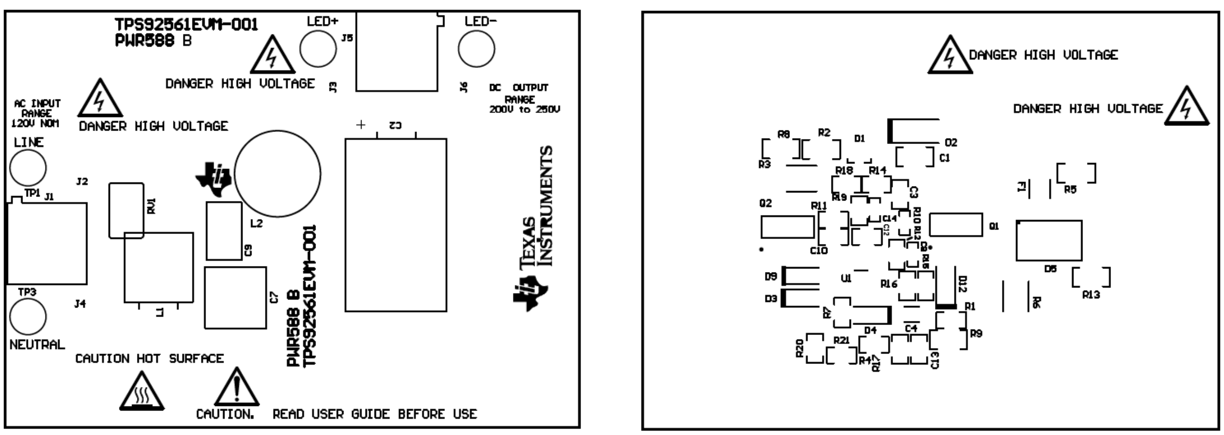


Figure 17. TPS92561 Boost Top (Left) and Bottom (Right) Layer Assembly Drawing

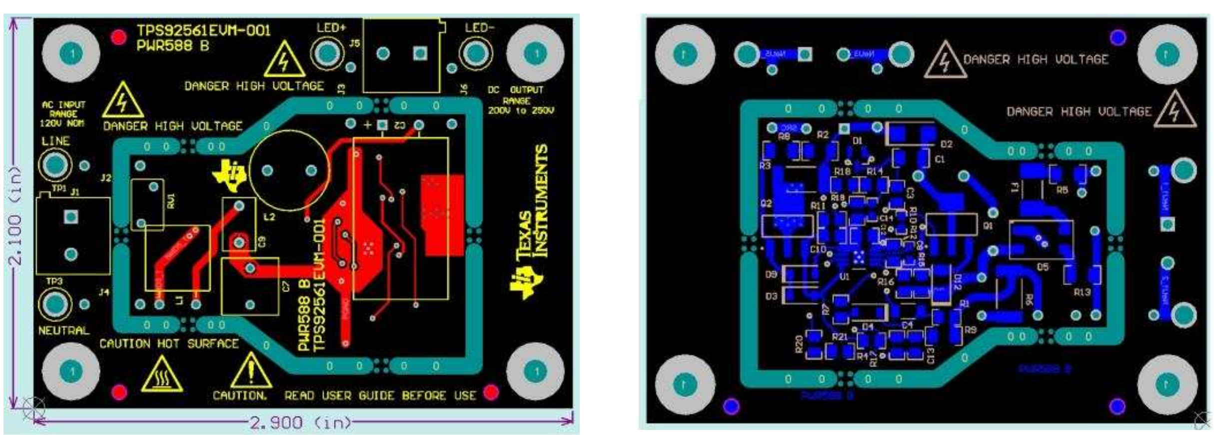


Figure 18. TPS92561 Boost Top (Left) and Bottom (Right) Copper Layer

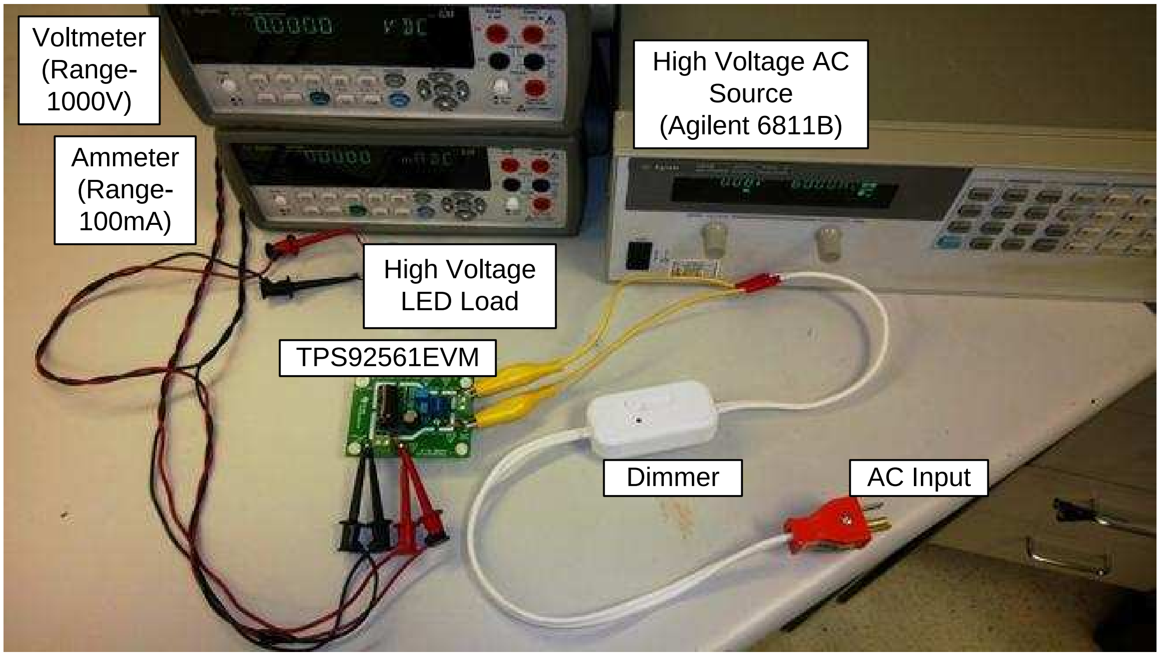
6.2 Bill of Materials

REF DES	QTY	DESCRIPTION	MANUFACTURER	PART NUMBER
U1	1	Phase Dimmable Hysteretic Boost LED Driver	Texas Instruments	TPS92561DGN
C1	1	Capacitor, ceramic, 100 pF, 630 V, ±5%, C0G/NP0, 1206	MuRata	GRM31A5C2J101JW01D
C2	1	Capacitor, aluminum, 22 µF, 350 V, 20% RADIAL	Panasonic Electronic Components	EEU-ED2V220
C4	1	Capacitor, ceramic, 0.22 µF, 250V, X7T, 10%, 1206	TDK Corporation	C3216X7T2E224K160AA
C7	1	Capacitor, Film, 0.22 µF, 25 V, ±5%, TH	EPCOS Inc	B32529D3224J
C8	1	Capacitor, ceramic, 1 µF, 16 V, ±10%, X7R, 0603	MuRata	GRM188R71C105KA12D
C9	1	Capacitor, Film, 0.1 µF, 250 V, ±10%, TH	EPCOS Inc	B32529C3104K
C10	1	Capacitor, ceramic, 2.2 µF, 25 V, ±10%, X7R, 0805	MuRata	GRM21BR71E225KA73L
C12	1	Capacitor, ceramic, 2200 pF, 100 V, +10/%, X7R, 0805	TDK	C2012X7R2A222K
C13	1	Capacitor, ceramic, 0.01 µF, 50V, +10/%, X7R, 0805	MuRata	GRM216R71H103KA01D
C14	1	Capacitor, ceramic, 0.1 µF, 16V, ±10%, X7R, 0603	MuRata	GRM188R71C104KA01D
D1	1	Diode, Switch, 200 V, 350 mA, SOT-23	Diodes Inc	BAV23S-7-F
D2	1	Diode Superfast, 400 V, 1 A, SMA	Diodes Inc	ES1G-13-F
D3	1	Diode, Ultrafast, 100 V, 0.15 A, SOD-123	Diodes Inc.	1N4148W-7-F
D4	1	Diode Zener, 110 V, 500 mW, SOD123	ON Semiconductor	MMSZ5272BT3G
D5	1	Diode, Switching-Bridge, 600V, 0.8A, MiniDIP	Diodes Inc.	HD06-T
D9	1	Diode, Zener, 15 V, 500 mW, SOD-123	Diodes Inc.	MMSZ5245B-7-F
D12	1	Diode, P-N, 1000 V, 1 A, 3.9 × 1.7 × 1.8 mm	Comchip Technology	CGRM4007-G
F1	1	Fuse, 500 mA, 125 V, 6125, slow SST	Bel Fuse Inc	SST 500
L1	1	Inductor 4700 µH, 0.13 A, radial	TDK Corporation	TSL0808RA-472JR13-PF
L2	1	Inductor, 10 mH, 0.173 A, radial	CoilCraft	RFB1010-103L
Q1, Q2	2	MOSFET N-channel, 400 V, 1.8 A, SOT-223	ST Microelectronics	STN3N40K3
R1	1	Resistor, 274 kΩ, 1%, 0.125 W, 0805	Vishay-Dale	CRCW0805274KFKEA
R2, R8	2	Resistor, 200 kΩ, 1%, 0.25 W, 1206	Vishay-Dale	CRCW1206200KFKEA
R3	1	Resistor, 10 kΩ, 1%, 1W, 2512	Vishay Dale	CRCW251210K0FKEG
R4	1	Resistor, 499 kΩ, 1%, 0.125 W, 0805	Vishay-Dale	CRCW0805499KFKEA
R5, R13	2	Resistor, 0 Ω, 5%, 0.25 W, 1206	Vishay-Dale	CRCW12060000Z0EA
R6	1	Resistor, 332 Ω, 1 W, 1%, 2512, SMD	Vishay Dale	CRCW2512332RFKEG
R7	1	Resistor, 30.1 kΩ, 1%, 0.125 W, 0805	Vishay-Dale	CRCW080530K1FKEA
R9	1	Resistor, 287 kΩ, 1%, 0.25 W, 1206	Vishay-Dale	CRCW1206287KFKEA
R10	1	Resistor, 100 Ω, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603100RFKEA
R11	1	Resistor, 0 Ω, 5%, 0.125 W, 0805	Vishay-Dale	CRCW08050000Z0EA
R12	1	Resistor, 1.00 kΩ, 1%, 0.125 W, 0805	Vishay-Dale	CRCW08051K00FKEA
R14, R18	2	Resistor, 806 kΩ, 1%, 0.125 W, 0805	Vishay-Dale	CRCW0805806KFKEA
R15, R16	2	Resistor, 3.32 Ω, 1%, 0.125 W, 0805	Vishay-Dale	CRCW08053R32FKEA
R17	1	Resistor, 374 Ω, 1%, 0.125 W, 0805	Vishay-Dale	CRCW0805374RFKEA
R19	1	Resistor, 7.15 kΩ, 1%, 0.125 W, 0805	Vishay-Dale	CRCW08057K15FKEA
RV1	1	Varistor, 200 V, 600 A, 5mm, radial, TH	Panasonic	ERZ-V05D201

REF DES	QTY	DESCRIPTION	MANUFACTURER	PART NUMBER
HARDWARE FOR EVM				
H1, H2, H3, H4	4	Machine Screw, Round, #4-40 x 1/4, Nylon	B&F Fastener	NY PMS 440 0025 PH
H5, H6, H7, H8	4	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C
H15	1	RTV167 Adhesive Sealant	Momentive	RTV167
J2, J3, J4, J6	4	Jumper 300mil spacing, Orange, 200 pc	3M	923345-03-C
J1, J5	2	Conn Term Block, 2POS, 5.08 mm PCB	Wurth Electronics	691212710002

Appendix A Detailed Test Setup and Test Data

A.1 Connection Snap-Shot



Remove the dimmer for a non-dimming setup.

Figure 19. Suggested Dimming Connection

A.2 Table Data – Boost Configuration

Table 3. Test Data Approximately 215-V LED Load

V_{IN} (Vrms)	I_{IN} (mArms)	P_{IN} (W)	PF	% THD	V_{OUT} (Vdc)	I_{OUT} (mAdc)	P_{OUT} Meas (W)	P_{OUT} Eff (%)
90	73.88	6.562	0.9887	8.9	213.61	27.30	5.83	88.87
95	78.55	7.337	0.9891	8.6	214.54	30.74	6.59	89.89
100	83.34	8.236	0.9893	8.2	215.2	34.47	7.42	90.07
105	88.06	9.138	0.9896	8.0	215.63	38.36	8.27	90.52
110	92.79	10.087	0.9898	7.7	215.88	42.49	9.17	90.94
115	97.62	11.103	0.9900	7.5	216.05	46.91	10.13	91.28
120	102.37	12.150	0.9901	7.3	215.88	54.54	11.13	91.58
125	102.73	12.476	0.9734	13.2	215.60	53.11	11.45	91.78
130	101.9	12.523	0.9464	19.0	215.35	53.47	11.51	91.95
135	98.73	12.176	0.9149	24.2	215.07	52.20	11.23	92.20

Table 4. Test Data: Forward Phase Dimmer – Leviton 6683

Forward Phase Dimmer – Leviton 6683				
LED Voltage (No dimmer)			215.46	V_{RMS}
LED Current (No dimmer)			51.65	mA
INPUT VOLTAGE (V_{RMS})	**INPUT POWER (W)**	**OUTPUT VOLTAGE (V)**	**LED CURRENT (mA)**	**LED CURRENT (% OF MAX)**
119	11.99	215.5	50.80	98.35
110	10.51	214.7	44.16	85.50
100	8.74	214.0	36.45	70.57
90	7.06	213.6	29.14	56.42
80	5.57	213.0	22.63	43.81
70	4.28	212.1	16.98	32.88
60	3.16	211.1	12.01	23.25
50	2.22	209.9	7.86	15.22
40	1.44	208.2	4.38	8.48
30	0.81	205.4	1.64	3.18
21	0.42	195.1	0.07	0.14

Table 5. Test Data: Reverse Phase Dimmer – Lutron Diva 303P

Reverse Phase Dimmer – Lutron Diva 303P				
LED Voltage (No dimmer)			215.46	V_{RMS}
LED Current (No dimmer)			51.65	mA
INPUT VOLTAGE (V_{RMS})	**INPUT POWER (W)**	**OUTPUT VOLTAGE (V)**	**LED CURRENT (mA)**	**LED CURRENT (% OF MAX)**
112	10.80	215.7	45.54	88.17
110	10.42	215.3	43.92	85.03
101	8.82	214.4	37.01	71.66
90	6.99	213.7	28.99	56.13
81	5.71	213.2	23.37	45.25
70	4.22	212.0	16.88	32.68
59	3.06	210.8	11.81	22.87
51	2.22	209.8	8.17	15.82
39	1.28	207.4	4.06	7.86
29	0.68	204.4	1.44	2.79
28	0.61	204.5	1.14	2.21

Table 6. Test Data: Electronic Dimmer – Lutron Maestro MAW-600H-LA

Lutron Maestro MAW-600H-LA				
LED Voltage (No dimmer)			215.46	V_{RMS}
LED Current (No dimmer)			51.65	mA
INPUT VOLTAGE (V_{RMS})	**INPUT POWER (W)**	**OUTPUT VOLTAGE (V)**	**LED CURRENT (mA)**	**LED CURRENT (% OF MAX)**
115	11.42	217.8	47.39	91.75
110	10.44	216.7	42.71	82.69
99	8.72	215.3	34.99	67.74
89	7.05	214.3	27.66	53.55
79	5.57	213.4	21.26	41.16
71	4.56	212.6	16.91	32.74
58	3.08	211.1	10.67	20.66
49	2.00	209.7	6.89	13.34
39	1.28	207.8	3.74	7.24
31	0.81	205.7	1.78	3.45

Appendix B Layout Considerations

B.1 Hysteretic Boost Converter Layout

Take special care when routing high di/dt and dv/dt traces in order to minimize the conducted and radiated EMI signature generated by the hysteretic boost converter circuit. A tight loop between the input capacitor, boost inductor and rectifying diode is recommended to minimize radiated EMI and prevent ground voltage difference (ground bounce). Please refer to the EVM layout, Figure 17 for further details.

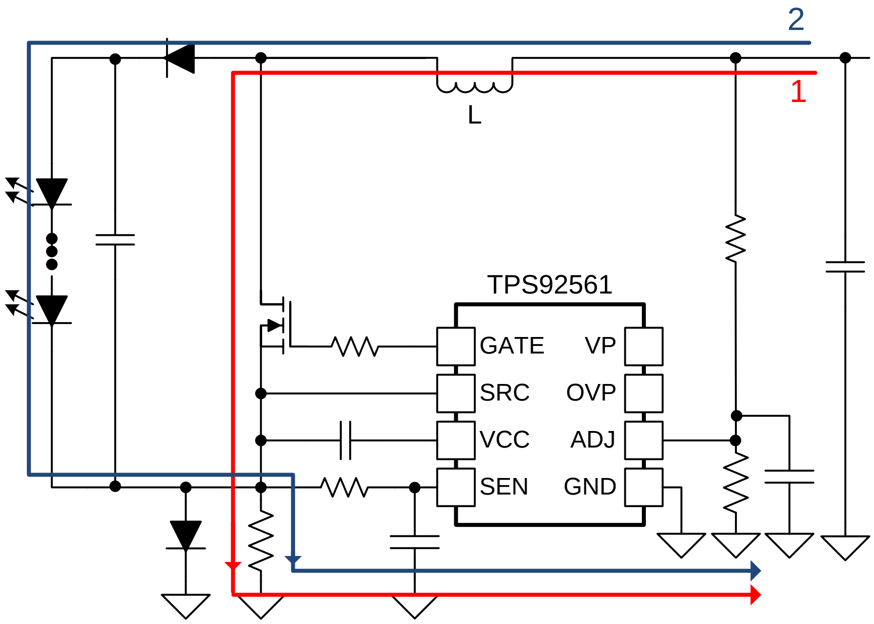


Figure 20. Critical Current Paths in Boost Topology

B.2 Current Sense Circuit Layout

A low-pass RC filter is used to attenuata switching noise from affecting the current sense operation. To be effective, the filter resistor, R12 and capacitor, C12 (refer to Figure 1) are required to be placed close to the device SEN pin (pin 4). The recommended layout is shown in Figure 21.

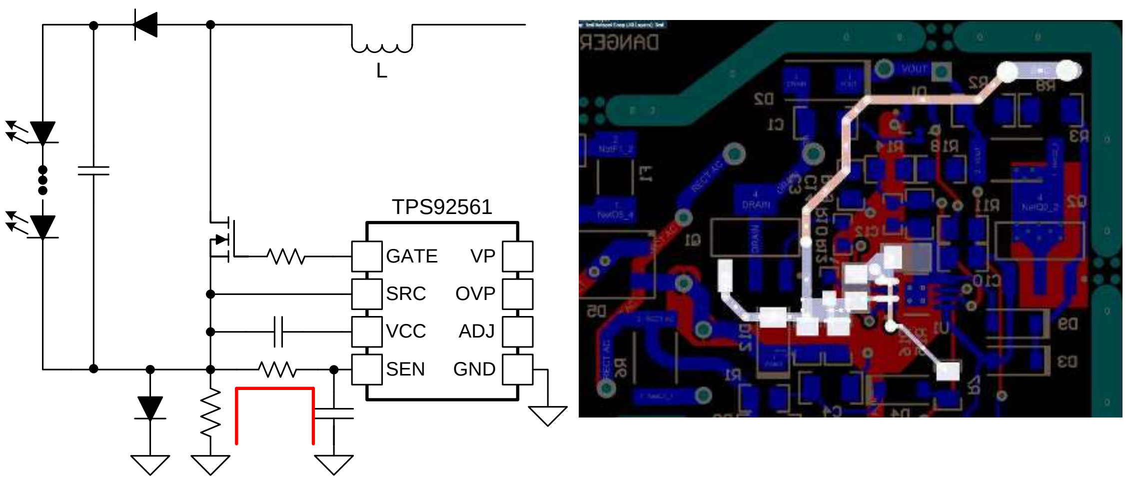


Figure 21. Current Sense Resistor and Filter Layout (Pin 4: SEN of TPS92561)

B.3 Gate-Drive Output and Switching MOSFET Layout

An external resistor is recommended to limit the interference between the noise generated by internal gate driver circuit and other sensitive nodes of the device. The placement of resistor close to GATE pin is recommended for maximum effectiveness, as shown in Figure 22.

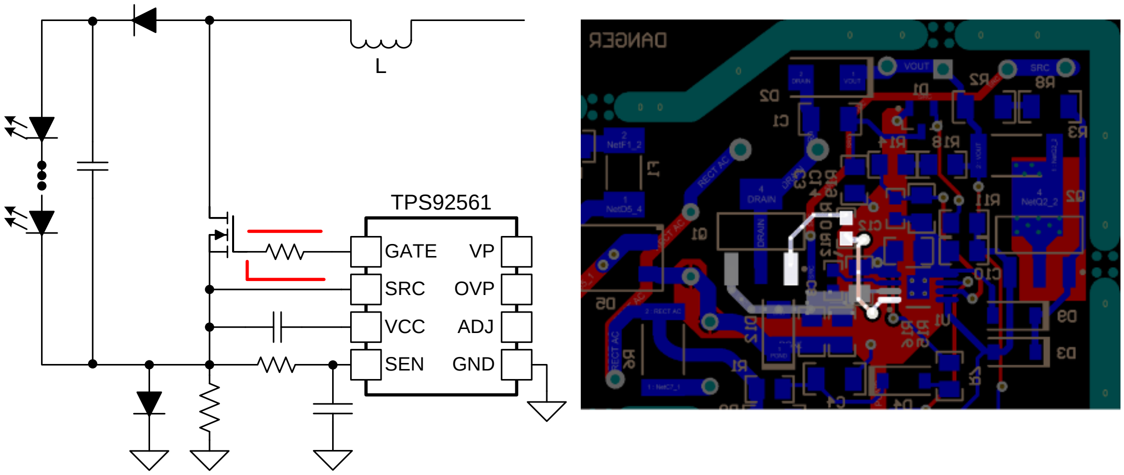


Figure 22. Gate Drive Output Circuit (Pin 1: GATE of TPS92561)

Appendix C EVM Circuit Options Used

C.1 Charge Pump Linear Assist

The TPS92561 data sheet describes methods to provide power to the IC. The method selected for this EVM uses the 'Linear regulator from output' method, deriving the IC bias voltage from the converter output. This causes a larger loss in the linear circuitry but provides performance advantages including: a more consistent turn off and a VP voltage with less variation when dimming. To gain some of the efficiency loss back, a charge pump is used (C1 and D1), as shown in Figure 1 , to assist the main linear regulator (Q2, D9, R2, R3, R8) by transferring charge to the bias circuit using a method that incurs lower losses than if it were derived from the linear regulator directly.

If the value of C1 is too high, the increase in associated switching losses in Q1 will not offset the gains made by reducing the current draw through the linear. An optimal operation point is reached when the voltage provided by the charge pump is just slightly higher then the voltage generated by the linear circuitry. As a good starting point to selecting the C1 value, we consider the current capability of the capacitance circuit and the current requirements of the IC. The IC uses approximately 1 mA plus the additional current required to switch the main FET ($Qg \times f_{sw}$). The C1 capacitor can provide a current based on the capacitance value, the voltage across the capacitor and the frequency of operation:

$$C \times V_{LED} \times f_{sw} \tag{1}$$

By combining the terms and solving for C1 we obtain:

$$C1 = \frac{1\text{ mA} + \left(Qg \times f_{sw}\right)}{V_{LED} \times f_{sw}} \tag{2}$$

After a capacitance value is obtained, some fine tuning under typical operating conditions should be considered as several factors affect the circuit performance including: exact LED voltage, VP bias voltage (Zener voltage and FET V_{GS} voltage), main FET gate charge requirements, and the variability of the converter switching frequency. In general the addition of the charge pump circuit can increase the converter efficiency 1% to 2% when compared to the linear from the output voltage alone. The highest possible efficiency is still achieved if an auxiliary winding is used to generate the bias voltage.

C.2 Line Regulation and Peak Power Limit

The EVM reference (ADJ pin voltage) is generated by dividing down the rectified AC voltage. This is a very simple method of generating the converter reference, but it also means the reference will change if the line voltage changes. When considering an LED bulb design for the US or Canadian market, long-term operation at input voltages that vary greatly from the nominal are not always considered. A simple means to ensure the LED heat sink temperature will remain controlled is to add this power limiting/line regulation circuit (R1, R7, D4, C4).

We can first estimate the voltage change at the ADJ pin (our reference voltage) based on the line change and consider an example for a line change from 120 to 132 VAC.

$$\Delta VrectAC = (132 - 120) \times \sqrt{2} \times .638 = 10.8 \text{ V} \tag{3}$$

Equation 3 gives us the average change in the average rectified AC voltage of approximately 10.8 V. We can apply this to our divider based on R9 and R17:

$$\Delta V\_ADJ = \frac{10.8 \times R17}{R9 + R17} \approx 140 \text{ mV} \tag{4}$$

The Zener was selected as 110 V based on the average rectified AC voltage for 120 VAC of 108 V.

Next we can design our compensation circuit to apply that same voltage offset when the average rectified AC voltage increases. Based on the circuit designators R1, D4, R7, R12 and the combination of R15 and R16 we can solve for the series resistance required to provide the current required to apply an offset voltage equal to the amount change due to the line. A simplified expression can be used:

$$R\_total = \frac{(V\_high\_line \times 0.9) - Vz}{\Delta V\_ADJ \div R12} = 586 \text{ k}\Omega \tag{5}$$

Equation 5 represents the total resistance of R1 + R7. The resistance should be split with a heavy bias to R1 limiting the voltage ripple on C4. After the circuit is in place, a few tests should be completed to allow fine tuning of the resistance values. This simplified approach did not account for the smaller variation from the conversion itself (given that the converter is controlling the input current, not the output current by the relationship:

$$Vin \times Iin = \frac{Vout \times Iout}{n} \tag{6}$$

Revision History

Changes from Original (December 2013) to A Revision **Page**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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- Increase the separation between the equipment and receiver.
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