KTPF4210EPEVBUG

KITPF4210EPEVB evaluation board

Rev. 1.0 — 8 February 2018 User guide

1 KITPF4210EPEVB

aaa-029237

2 Important notice

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The tool summary page for KITPF4210EPEVB is located at http://www.nxp.com/KITPF4210EPEVB. The overview tab provides an overview of the device, product features, a description of the kit contents, a list of (and links to) supported devices, list of (and links to) any related products and a **Get Started** section.

The **Get Started** section provides links to everything needed to start using the device and contains the most relevant, current information applicable to the KITPF4210EPEVB.

- Go to http://www.nxp.com/KITPF4210EPEVB.
- On the **Overview** tab, locate the **Jump To** navigation feature on the left side of the window.
- Select either the **Get Started** link or scroll in the main window of the **Overview** tab until the **Get Started** section is visible.
- Review each entry in the **Get Started** section.
- Download an entry by clicking on the title.
- After reviewing the **Overview** tab, visit the other product related tabs for additional information:
  - **Documentation**: download current documentation
  - **Software & Tools**: download current hardware and software tools
  - **Buy/Parametrics**: purchase the product and view the product parametrics

After downloading files, review each file, including the user guide which includes setup instructions. If applicable, the bill of materials (BOM) and supporting schematics are also available for download in the **Get Started** section of the **Overview** tab.

3.1 Kit contents/packing list

The KITPF4210EPEVB contents include:

- Assembled and tested KITPF4210EPEVB board in an anti-static bag
- Quick start guide
- Warranty card

3.2 Required equipment

To use this kit, you need:

- Power supply:
  - Output voltage range from 3.1 V to 4.5 V
  - Current capability from 3.0 to 5.0 A (current requirement is dependent on output loading)
- Supply to board connection cables (capable of withstanding up to 5.0 A current)
- USB (male) to mini USB (male) communication cable
- USB-enabled computer

3.3 System requirements

The kit requires the following to function properly with the software:

- Windows XP or Windows 7 operating system

4 Getting to know the hardware

4.1 Board features

- Input voltage operation range from 3.1 V to 4.5 V
- Output voltage supplies accessible through detachable terminal blocks
  - Four to six independent buck converters
  - One 5.0 V boost regulator
  - Six general purpose LDO regulators
  - One DDR memory termination voltage reference
  - One VSRTC supply
- Coin cell support for “Try-Before-Buy” (TBB) mode
- On/off push button support
- Hardware configuration flexibility through various jumper headers and resistors
- Integrated USB to I^2C programming interface for full control/configuration
  - Onboard PMIC control through the I^2C register map
  - Fully featured programmer through J36 for external device control/programming
- On board connectors for interfacing with future evaluation/debug tools
- Compact form factor (4 x 4 in^2)

4.2 Device features

Table 1. Device features

Device	Description	Features
PF4210	The PF4210 Power Management Integrated Circuit (PMIC) provides a highly programmable/configurable architecture with fully integrated power devices and minimal external components. With up to six buck converters, six linear regulators, RTC supply, and coin-cell charger, the PF4210 can provide power for a complete system, including applications processors, memory, and system peripherals, in a wide range of applications.	• Four to six buck converters, depending on configuration – Single/Dual phase/ parallel options – DDR termination tracking mode option • Boost regulator to 5.0 V output • Six general purpose linear regulators • Programmable output voltage, sequence, and timing • OTP (One Time Programmable) memory for device configuration • Coin cell charger and RTC supply • DDR termination reference voltage • Power control logic with processor interface and event detection • I^2C control • Individually programmable ON, OFF, and Standby modes
MC9S08JM60	The KITPF4210EPEVB implements a NXP MC9S08JM60 low-cost, high-performance 8-bit HCS08 microcontroller to interface via USB to I^2C to control the main PMIC.	• 8-bit HCS08 Central Processing Unit (CPU) – Up to 24 MHz internal bus (48 MHz HCS08 core) frequency offering 2.7 to 5.5 V across temperature range of −40 °C to +85 °C – Support for up to 32 peripheral interrupt/reset sources • On-chip memory – Up to 60 K flash read/program/erase over full operating voltage and temperature – Up to 4 K RAM – 256 Byte USB RAM

4.3 Board description

The KITPF4210EPEVB operates with a single power supply from 3.1 V to 4.5 V and is controlled via USB with help of an integrated USB-I2C communication bridge. By applying the input voltage supply, the KITPF4210EPEVB powers up according to the default power-up sequence described in the PF4210 data sheet.

Important: *If power-up sequences and configurations are to be modified, the user must ensure that the register settings are consistent with the hardware configuration. This is most important for the buck regulators, where the quantity, size, and value of the inductors depend on the configuration (single/dual phase or independent mode) and the switching frequency. Additionally, if an LDO is powered by a buck regulator, it is gated by the buck regulator in the start-up sequence. See PF4210 data sheet for details on buck regulator setup.*

4.3.1 Jumper definitions

By default, the KITPF4210EPEVB evaluation board is set to power up from the default power-up sequence. Verify that the jumpers are placed in the right position as shown in Figure 1. For a detailed description of the jumper functionality, see Table 2.

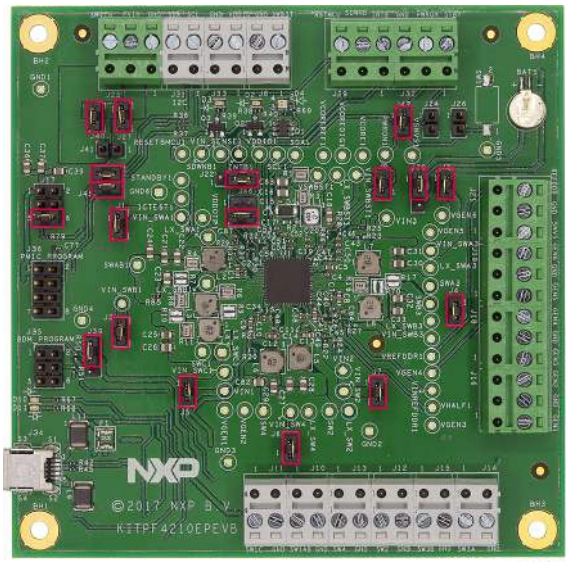

Figure 1. Default jumper configuration

Table 2. Jumper definitions

Jumper	Default	Description
J1-J7	Closed	Buck regulators input power path isolation Short these jumpers to allow SWxIN to be powered from the SWVIN supply
J9	Closed	SWBST regulator input power path isolation Short this jumper to allow SWBSTIN to be powered from the SWVIN supply
J17	5-6	VDDOTP supply selector • 1-2: Connect VDDOTP to the OTP Boost output (VDDOTPIN) for OTP programming • 3-4: Connect VDDOTP to GND to power up from OTP/TBB sequence • 5-6: Connect VDDOTP to VCOREDIG to power up from default power-up sequence
J20	1-2	Coin cell selector • 1-2: Enables BAT1 as the main coin cell supply • 2-3: Enables BAT2 as the main coin cell supply
J40	Closed	Shorts PVIN and SWVIN Allows supply isolation to provide more accurate efficiency readings on the switching supplies
J41	Open	Shorts SWVIN to VIN Allows one to isolate or connect the PF4210 logic input supply to SWVIN net. (debugging option)
J27	Closed	Shorts PVIN to VIN Allows one to isolate or connect the PF4210 logic input supply to PVIN net. (debugging option)
J22	2-3	PF4210 input logic supply selector • 1-2: Connects PF4210 VIN terminal to the 3.3 V external LDO regulator for debugging purposes • 2-3: Connects PF420 VIN terminal to the main input supply
J26	Open	Short to hold PWRON pin low
J24	Open	Short to pull STANDBY to VSNVS voltage supply
J39	1-2	Control interface input supply selector • 1-2: Enables PVIN node as the input supply source for the control interface • 2-3: Enables USB power as the input supply source for the control interface

4.3.2 Connector and terminal block definitions

Table 3. Terminal block definitions

Connector	Function	Pin definition
J8	SWBST	Pin 1 - SWBST output Pin 2 - GND
J10	SW1AB	Pin 1 - SW1AB output Pin 2 - GND
J11	SW1C	Pin 1 - SW1C output Pin 2 - GND
J12	SW2	Pin 1 - SW2 output Pin 2 - GND
J13	SW4	Pin 1 - SW4 output Pin 2 - GND
J14	SW3A	Pin 1 - SW3A output Pin 2 - GND
J15	SW3B	Pin 1 - SW3B output Pin 2 - GND
J16	VGEN1/VGEN2	Pin 1 - VGEN1 output Pin 2 - GND Pin 3 - VGEN2 output
J18	VGEN3/VGEN4	Pin 1 - VGEN3 output Pin 2 - GND Pin 3 - VGEN4 output
J19	VGEN5/VGEN6	Pin 1 - VGEN5 output Pin 2 - GND Pin 3 - VGEN6 output
J21	VSNVS/VREFDDR	Pin 1 - VSNVS output Pin 2 - GND Pin 3 - VREFDDR output
J25	Main input supply	Pin 1 - GND Pin 2 - PVIN Pin 3 - SWVIN
J29	Interfacing 1	Pin 1 - INTB Pin 2 - SDWNB Pin 3 - RESETBMCU
J32	Interfacing 2	Pin 1 - STANDBY Pin 2 - PWRON Pin 3 - GND
J31	I^2C signals	Pin 1 - SCL Pin 2 - SDA
J33	VDDIO	Pin 1 - VDDIO Pin 2 - GND

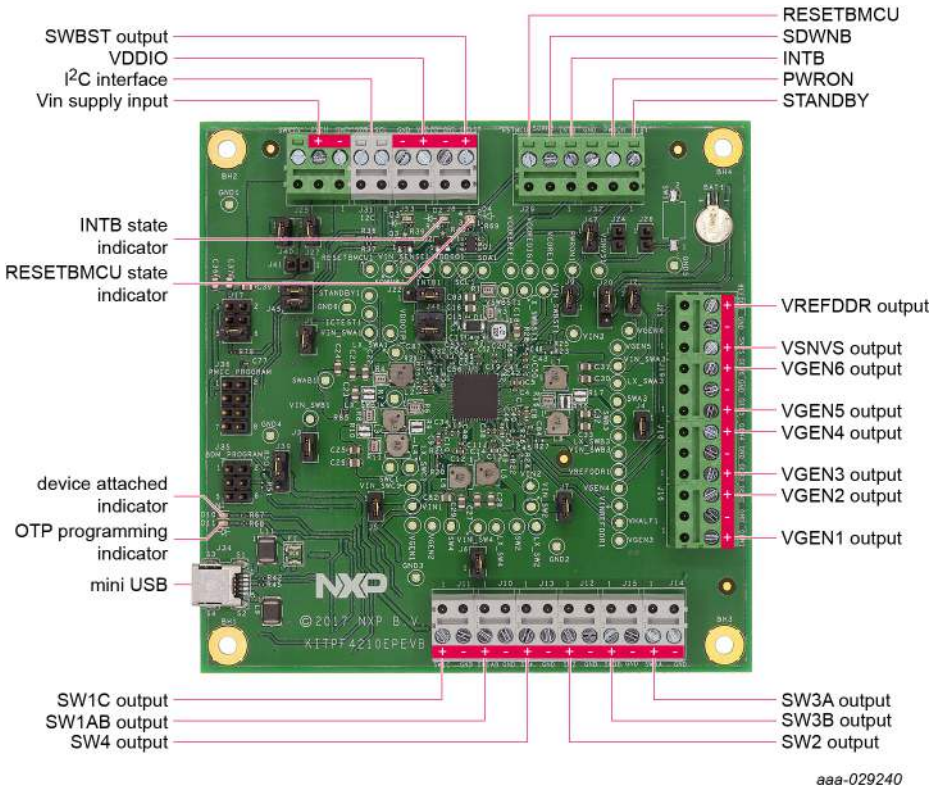

Figure 2. Input/output terminal blocks

Table 4. Connector definitions

Connector	Function	Pin definition
J34	Mini USB connector	Pin 1 - VBUS Pin 2 - D− Pin 3 - D+ Pin 4 - NC Pin 5 - GND Chassis - GND
J35	BDM connector	Pin 1 - BKGD_JM60 Pin 2 - GND Pin 3 - NC Pin 4 - RST_JM60 Pin 5 - NC Pin 6 - USB_PWR
J36	Programmer connector	Pin 1 - VDDOTPIN (8.5 V boost output) Pin 2 - 3V3 (3.3 V LDO output) Pin 3 - GND Pin 4 - MCU_SCL (I^2C clock signal) Pin 5 - MCU_SDA (I^2C data signal) Pin 6 - PWRON (controls the PWRON on the target device) Pin 7 - GPIO 1 (general purpose GPIO) Pin 8 - GPIO 2 (general purpose GPIO)
J42	Debug Port 1	Debugging connector for future development tools
J43	Debug Port 2	Debugging connector for future development tools
J44	Debug Port 3	Debugging connector for future development tools

4.3.3 Debug and configuration components

The KITPF4210EPEVB allows full flexibility to change the default configuration of SW1A/B/C and SW3A/B outputs to one more suitable for a specific application scenario. It also provides several source options for the LDO supplies to test various loading and supplying scenarios.

Test points are provided on key nodes of the KITPF4210EPEVB to allow full debugging capability during application development.

4.3.3.1 SW1A/B/C configuration components

The SW1A/B/C regulator can be configured in various operating modes as described in Table 5.

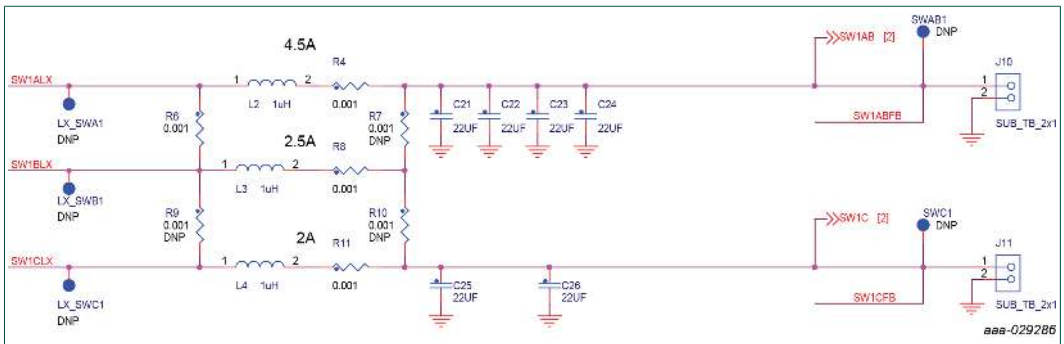

Figure 3. SW1A/B/C output configuration

Table 5. SW1A/B/C configuration chart

Component	SW1A/B/C single phase	SW1A/B single phase SW1C independent	SW1A/B dual phase SW1C independent
R6	Closed	Closed	DNP
R9	Closed	DNP	DNP
R4	Closed	Closed	Closed
R7	Closed	DNP	Closed
R8	DNP	DNP	Closed
R10	Closed	DNP	DNP
R11	DNP	Closed	Closed
L2	1.0 µH ISAT = 6.0 A	1.0 µH ISAT = 4.5 A	1.0 µH ISAT = 2.4 A
L3	N/A	N/A	1.0 µH ISAT = 2.4 A
L4	N/A	1.0 µH ISAT = 2.4 A	1.0 µH ISAT = 2.4 A

4.3.3.2 SW3A/B configuration components

The SW3A/B regulator can be configured in various operating modes as described in Table 6.

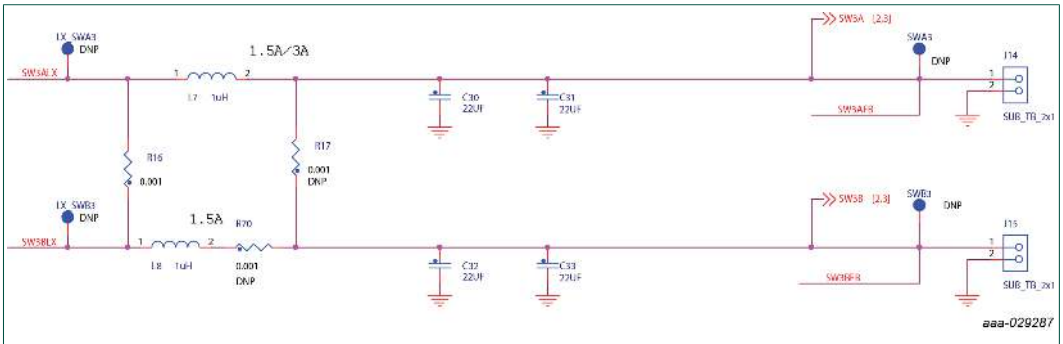

Figure 4. SW3A/B output configuration

Table 6. SW3A/B configuration chart

Component	SW3A/B single phase	SW3A/B dual phase	SW3A independent SW3B independent
R16	Closed	DNP	DNP
R17	Closed	Closed	DNP
R70	DNP	Closed	Closed
L7	1.0 µH ISAT = 3.9 A	1.0 µH ISAT = 3.0 A	1.0 µH ISAT = 3.0 A
L8	N/A	1.0 µH ISAT = 3.0 A	1.0 µH ISAT = 3.0 A

4.3.3.3 LDO input supply source selection

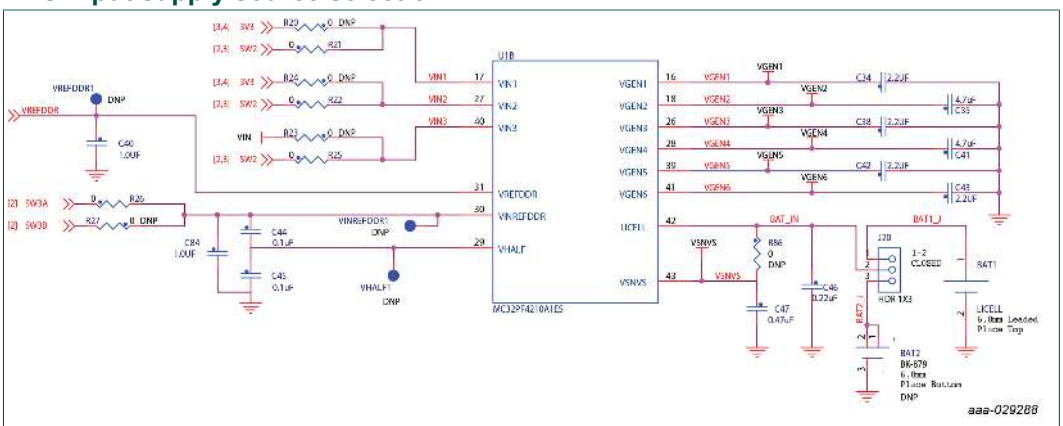

Figure 5. LDO schematic configuration

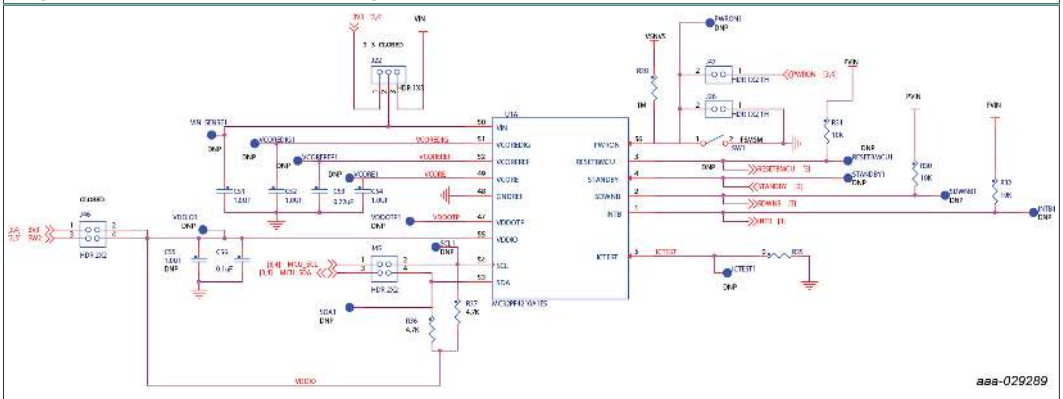

Figure 6. Logic and core supplies

Table 7. LDO input supply configuration chart

Input pin	Input options [1]
VIN1	Input supply for VGEN1 and VGEN2 R20 = SW4 R21 = SW2
VIN2	Input supply for VGEN3 and VGEN4 R24 = SW4 R22 = SW2
VIN3	Input supply for VGEN5 and VGEN6 R23 = VIN R25 = SW2
VINREFDDR	VREFDDR input supply R26 = SW3A R27 = SW3B
VDDIO	VDDIO input supply 3V3 J46 = 1-2 SW2 J46 = 2-3

[1] Make sure to populate only one option per input pin to avoid shorts between various sources.

4.3.3.4 Test point definitions

All test points are clearly marked on the KITPF4210EPEVB evaluation board. Figure 7 shows the location of various test points.

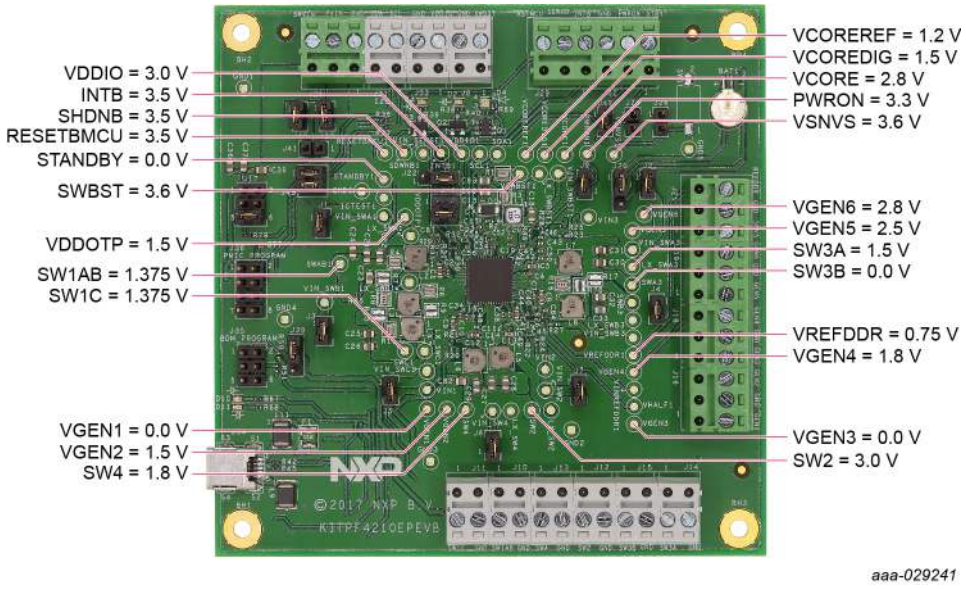

Figure 7. Key test point locations and default voltages

4.3.4 Miscellaneous components

4.3.4.1 Power on push button

A footprint for a normally open, momentary push-button is provided at the PWRON terminal to allow a momentary low state by pressing the push button. J47 allows isolation of the PWRON terminal from the MCU GPIO controlling this pin.

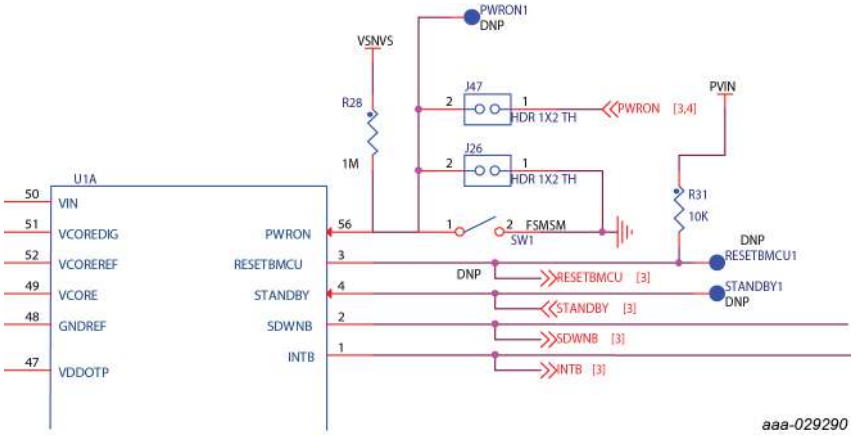

Figure 8. Power on circuit

4.3.4.2 PMIC LED indicators

LED indicators are provided to notify the PMIC status to the user. Figure 9 shows the PMIC status. LEDs D2 and D4, and a reserved LED indicator D3, allow an external rework connection to the transistor gate if any given signal debug is required.

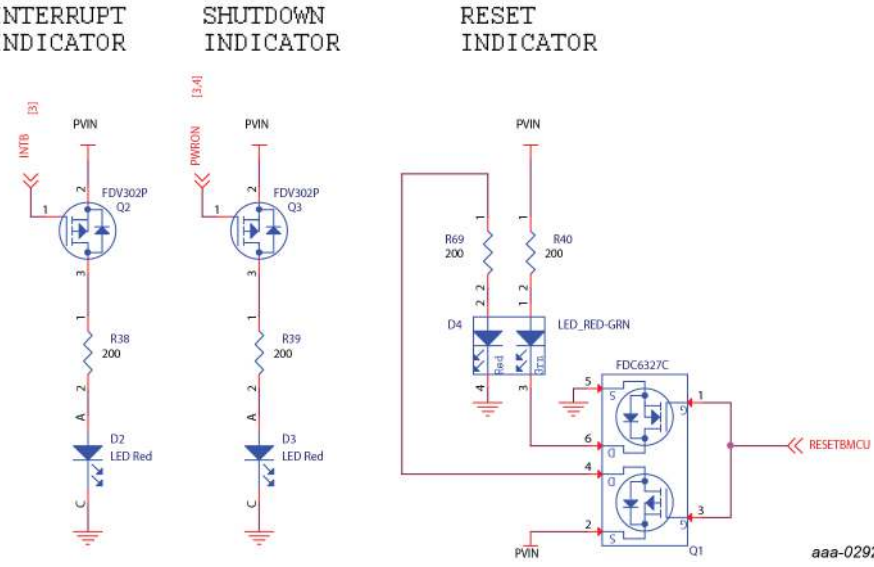

Figure 9. PMIC status indicator

Table 8. LED state description

LED	Description
D2	Interrupt notification ON = PMIC has detected an unmasked interrupt OFF = No interrupt detected
D4	RESETBMCU notification Green = PMIC is in regulation and operating properly Red = PMIC is out of regulation
D3	PWRON notification ON = PWRON is low OFF = PWRON is high

4.3.4.3 Control/programming interface

This onboard USB-to-I^{2}C interface comprises three basic blocks.

1. Controlling MCU (MC9S08JM60CGTE) for USB-I2C translation
2. 3.3 V LDO supply for external device controlling
3. 8.25 V boost converter for OTP programming

The control/programming interface allows one to program the onboard PF4210 PMIC. Alternatively, the interface can serve as a programmer for external devices though the connector J36.

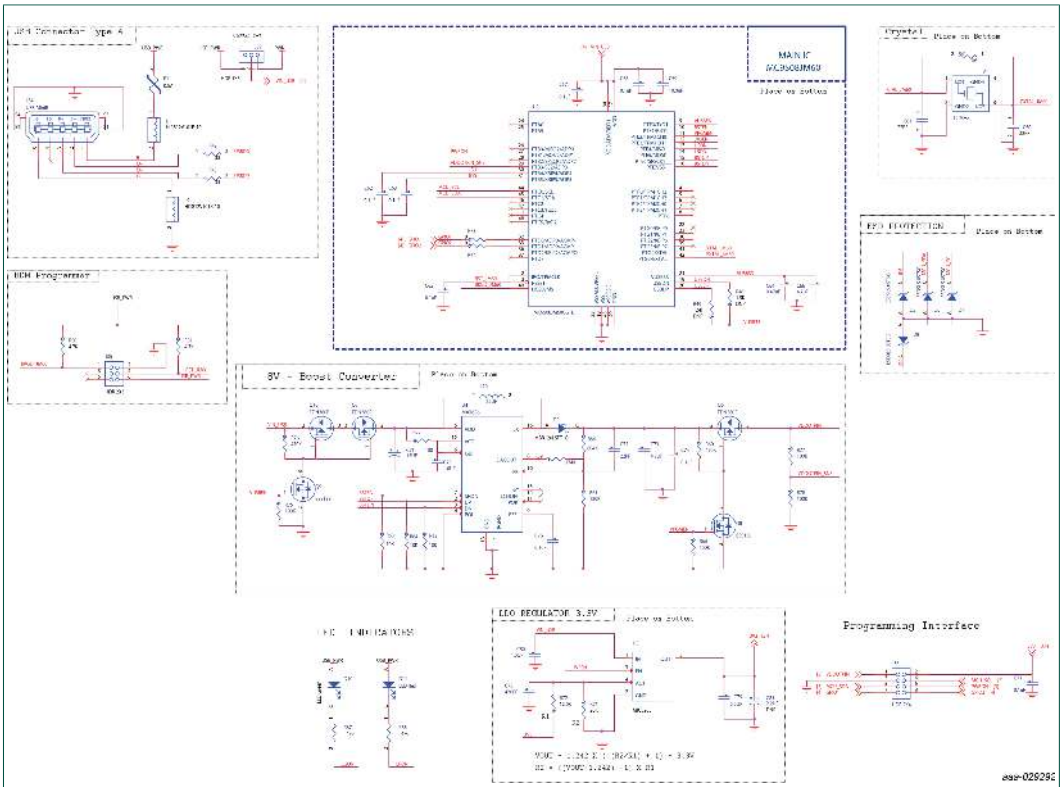

Figure 10. Control/programming interface

5 Configuring the hardware

Connect the power supply and the USB communication cables as shown in Figure 11. Voltmeters are optional but it is recommended in order to accurately verify that each one of the output supplies is providing the correct voltage level.

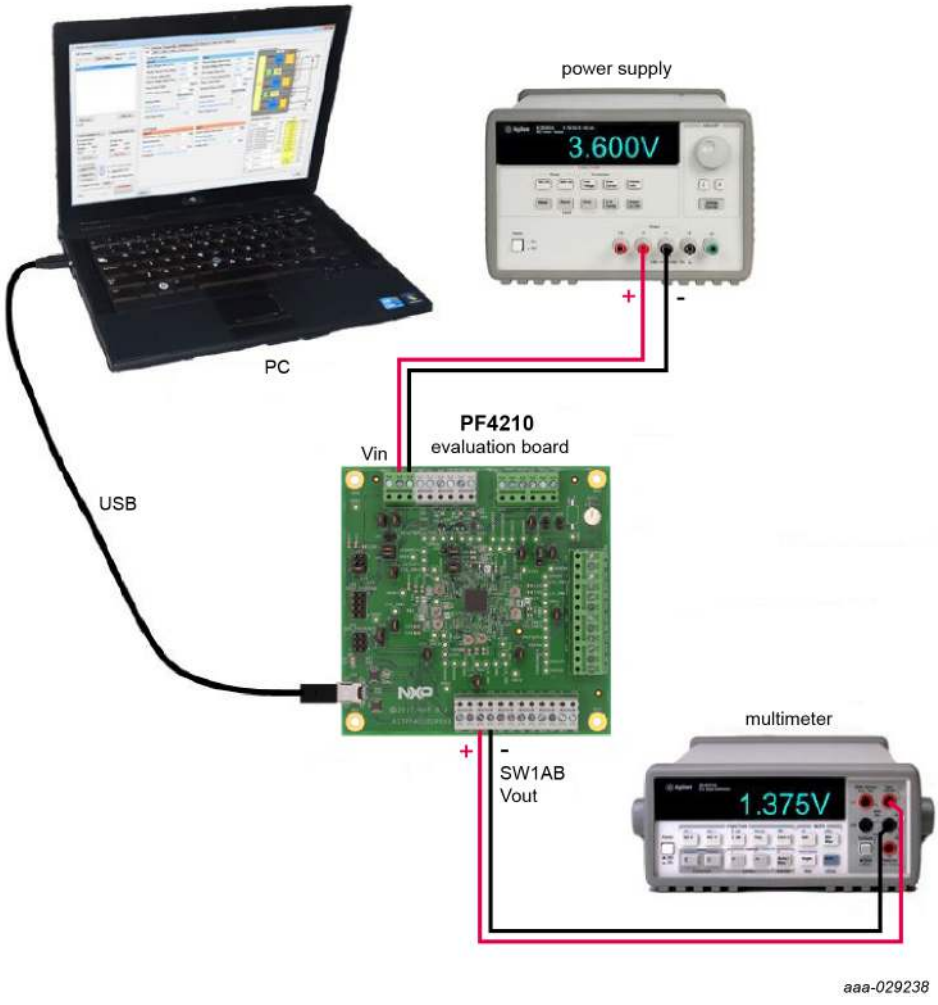

Figure 11. Evaluation board setup

Note: *The KITPF4210EPEVB allows the selection of SW2 regulator output or an external 3.3 V LDO output as the VDDIO/I^2C pull-up supply. By default, the SW2 regulator is the source for the VDDIO supply (J46 = 3-4). If the SW2 regulator is to be set below 3.0 V, then switch the 3.3 V LDO connection to VDDIO (J46 = 1-2).*

6 Schematics, board layout and bill of materials

Board schematics, board layout and bill of materials are available in the download tab of the tool summary page: http://www.nxp.com/KITPF4210EPEVB.

7 References

Following are URLs where you can obtain information on related NXP products and application solutions:

NXP.com support pages	Description	URL
KITPF4210EPEVB	Tool summary page	http://www.nxp.com/KITPF4210EPEVB
PF4210	Product summary page	http://www.nxp.com/PF4210

Revision history

Revision history

Rev	Date	Description
v.1	20180208	Initial version

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