

CD54/74HC182 CD54/74HCT182



NOT RECOMMENDED FOR NEW DESIGNS

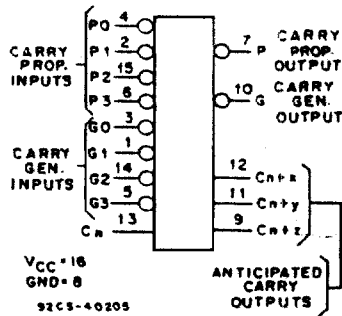
December 1997

High-Speed CMOS Logic

Look-Ahead Carry Generator

Type Features:

- Provides carry look-ahead across a group of four ALU's
- Multi-level look-ahead for high-speed arithmetic operation over long word length



FUNCTIONAL DIAGRAM

The Harris CD54/74HC182 and CD54/74HCT182 carry look-ahead generators are high-speed silicon-gate CMOS devices and are pin compatible with low-power Schottky TTL (LSTTL).

The CD54/74HC/HCT182 accept up to four pairs of active LOW carry propagate ($\overline{P}_0, \overline{P}_1, \overline{P}_2, \overline{P}_3$) and carry generate ($\overline{G}_0, \overline{G}_1, \overline{G}_2, \overline{G}_3$) signals and an active HIGH carry input (C_n). The devices provide anticipated active HIGH carries ($C_{n+x}, C_{n+y}, C_{n+z}$) across four groups of binary adders. The HC/HCT182 also has active LOW carry propagate (\overline{P}) and carry generate (\overline{G}) outputs which may be used for further levels of look ahead.

The logic equations provided at the outputs are:

$$C_{n+x} = P_0 C_n + G_0$$

$$C_{n+y} = G_1 + P_1 G_0 + P_1 P_0 C_n$$

$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$$

$$\overline{G} = \overline{G}_3 + \overline{P}_3 \overline{G}_2 + \overline{P}_3 \overline{P}_2 \overline{G}_1 + \overline{P}_3 \overline{P}_2 \overline{P}_1 \overline{G}_0$$

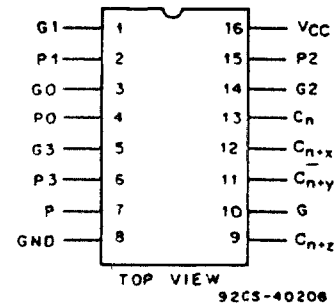
$$\overline{P} = \overline{P}_3 \overline{P}_2 \overline{P}_1 \overline{P}_0$$

The CD54/74HC/HCT182 can also be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry look-ahead generator are identical in both cases.

The CD54HC182 and CD54HCT182 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC182 and CD74HCT182 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (over temperature range):
Standard outputs - 10 LSTTL loads
Bus driver outputs - 15 LSTTL loads
- Wide operating temperature range:
-55 to +125°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- Alternate source is Philips/Sigmetrics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High noise immunity: $N_{IL} = 30\%, N_{IH} = 30\%$ of V_{CC} @ $V_{CC} = 5 V$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL input logic compatibility
 $V_{IL} = 0.8 V$ max., $V_{IH} = 2 V$ Min.
CMOS input compatibility
 $I_i \leq 1 \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

HARRISD14

Technical Data

CD54/74HC182

CD54/74HCT182

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC} *			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_i, V_o	0	V_{CC}	V
Operating Temperature T_A	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

FUNCTION TABLE

INPUTS									OUTPUTS				
C_n	G_0	P_0	G_1	P_1	G_2	P_2	G_3	P_3	C_{n+1}	C_{n+2}	C_{n+3}	G	P
X L X H	H L L X	H X X L							L L H H				
X X L X X H	X H H X L X	X H X X L	H H L X	H X X L						L L L H H			
X X X L X X X H	X X H H X X L X	X X H X X X L	X H H H X L X X	X H X X X L L	H H H L X X	H X X X X L L				L L L L H H H			
	X X X H X X X L		X X H H X X L X	X X H X X X L	X H H H X L X	X H X X X L L	H H H L X X X	H X X X X L L L				H H H L L L L	
		H X X X L		X H X L		X X H X L		X X H L					H H H L

H = HIGH voltage level

L = LOW voltage level

X = don't care

CD54/74HC182 CD54/74HCT182

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC182/CD54HC182										CD74HCT182/CD54HCT182										UNITS
	TEST CONDITIONS			AMBIENT TEMPERATURE (T _A)							TEST CONDITIONS			AMBIENT TEMPERATURE (T _A)							
	V _I V	I _O mA	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V _I V	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C			
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5	2	—	—	2	—	2	—	V	
			4.5	3.15	—	—	3.15	—	3.15	—	—	to	—	—	—	—	—	—	—		
			6	4.2	—	—	4.2	—	4.2	—	5.5	—	—	—	—	—	—	—			
Low-Level Input Voltage V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5	—	—	0.8	—	0.8	—	0.8	V	
			4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	—	—	—	—	—		
			6	—	—	1.8	—	1.8	—	1.8	—	5.5	—	—	—	—	—	—	—		
High-Level Output Voltage V _{OH} CMOS Loads	V _{IL} or V _{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL} or V _{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V	
			4.5	4.4	—	—	4.4	—	4.4	—											
			6	5.9	—	—	5.9	—	5.9	—											
TTL Loads	V _{IL} or V _{IH}	-4 -5.2	4.5	3.98	—	—	3.84	—	3.7	—	V _{IL} or V _{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V	
			6	5.48	—	—	5.34	—	5.2	—											
Low-Level Output Voltage V _{OL} CMOS Loads	V _{IL} or V _{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL} or V _{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V	
			4.5	—	—	0.1	—	0.1	—	0.1											
			6	—	—	0.1	—	0.1	—	0.1											
TTL Loads	V _{IL} or V _{IH}	4 5.2	4.5	—	—	0.26	—	0.33	—	0.4	V _{IL} or V _{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V	
			6	—	—	0.26	—	0.33	—	0.4											
Input Leakage Current I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA	
Quiescent Device Current I _{CC}	V _{CC} or Gnd	0	6	—	—	8	—	80	—	160	V _{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA	
Additional Quiescent Device Current per input pin: 1 unit load ΔI _{CC} *											V _{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA	

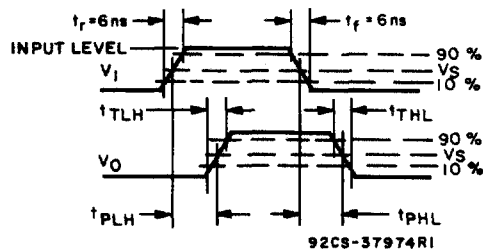
*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
P ₀ , P ₁ , P ₂ , G ₀ , G ₁	1.5
P ₃ , G ₂ , C _n	1.25
G ₃	0.3

* Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC182
CD54/74HCT182



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition times and propagation delay times.