

General Description

The DSC2123FI2-E0024 is a programmable, high performance dual output oscillator utilizing Microchip's proven silicon MEMS technology to provide excellent jitter and stability while incorporating additional device functionalities.

The DSC2123FI2-E0024 allows the user to independently modify the frequency of each output using I2C interface.

The user can also select from two pre-programmed default output frequencies using the frequency select pin.

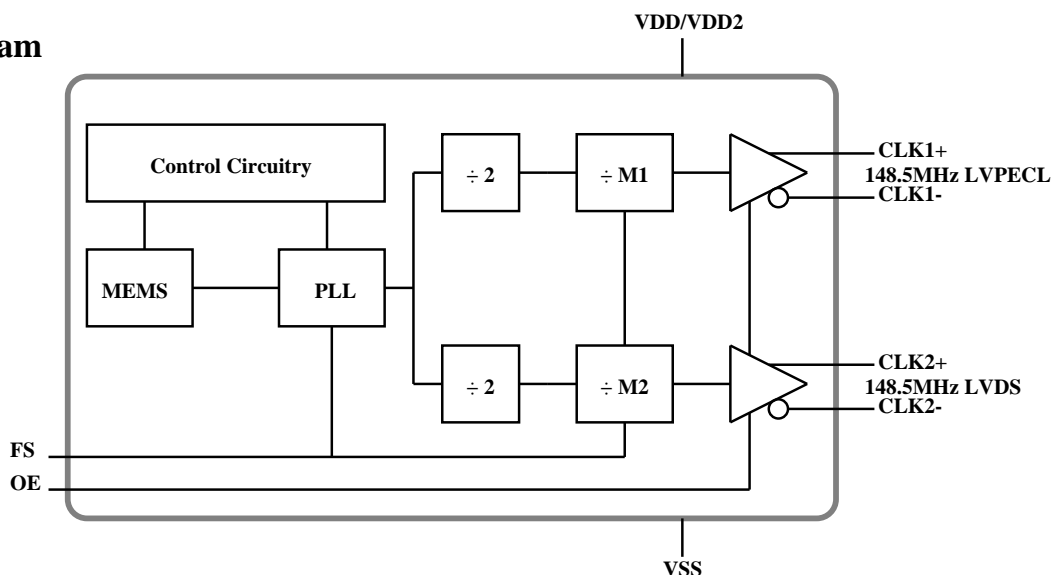
Applications

- Consumer Electronics
- Storage Area Networks
 - SATA, SAS, Fibre Channel
- Passive Optical Networks
 - EPON, 10G-EPON, GPON, 10G-GPON
- Ethernet
 - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- HD/SD/SDI Video & Surveillance
- PCI Express
- Automotive

Features

- Frequency and output formats:
 - LVPECL
148.5/148.5MHz
 - LVDS
148.5/148.5MHz
- Low RMS phase jitter: <1ps (typ)
- ±25ppm frequency stability
- -40°C to +85°C industrial temperature range
- High supply noise rejection: -50dBc
- I2C programmable frequencies
- Excellent shock & vibration immunity
 - Qualified to MIL-STD-883
- High reliability
 - 20x better MTF than quartz oscillators
- Supply range of 2.25 to 3.6V
- AEC-Q100 automotive qualified
- 14-pin 3.2mm x 2.5mm QFN package

Block Diagram



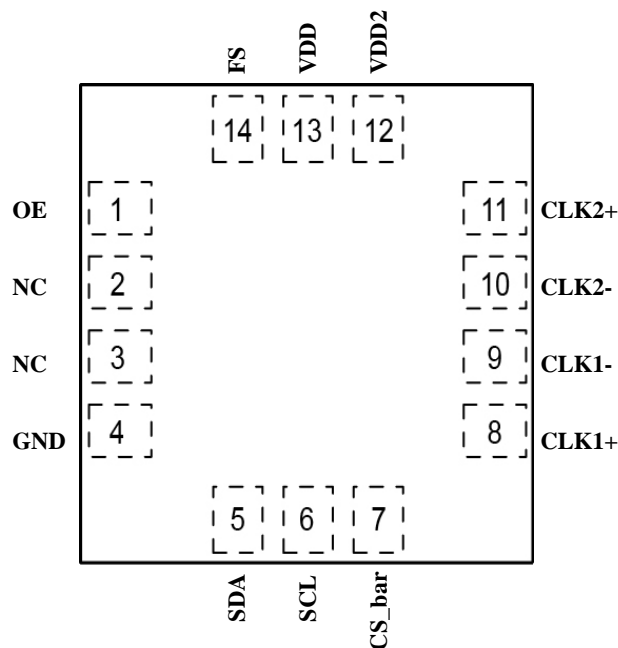
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Ordering Information

Ordering Part Number	Industrial Temperature Range	Shipping	Package
DSC2123FI2-E0024	-40°C to +85°C	Tube	14-pin 3.2mm x 2.5mm QFN
DSC2123FI2-E0024T	-40°C to +85°C	Tape and Reel	14-pin 3.2mm x 2.5mm QFN

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



14-pin 3.2mm x 2.5mm QFN

Pin Description

Pin Number	Pin Name	Pin Type	Pin Function
1	OE	I	Enables outputs when high and disables outputs when low
2	NC		Leave unconnected or connect to ground
3	NC		Leave unconnected or connect to ground
4	GND	PWR	Ground
5	SDA	I	I2C serial data
6	SCL	I	I2C serial clock
7	CS_bar	I	I2C chip select (active low)
8	CLK1+	O	Positive LVPECL output
9	CLK1-	O	Negative LVPECL output
10	CLK2-	O	Negative LVDS output
11	CLK2+	O	Positive LVDS output
12	VDD2	PWR	Power supply for LVDS output CLK2, 1.65V to 3.6V ($VDD2 \leq VDD$)
13	VDD	PWR	Power supply
14	FS	I	Frequency select pin, see Table 1 for details

Operational Description

The DSC2123FI2-E0024 is a dual oscillator with an LVPECL output and an LVDS output. The device consists of a MEMS resonator and a supporting PLL IC. Two outputs are generated through independent 8-bit programmable dividers from the output of the internal PLL.

DSC2123FI2-E0024 allows for easy programming of the output frequencies using I2C interface.

Upon power-up, the output frequencies are controlled by an internal pre-programmed memory (OTP). This memory stores all coefficients required by the PLL for two different frequency pairs.

The control pin (FS) selects the initial pair. Once the device is powered up, a new output selects frequency pair can be specified using the I2C interface.

Programming details are provided in the Programming Guide.

When OE (pin 1) is floated or connected to VDD, the DSC2123FI2-E0024 is in operational mode. Driving OE to ground will disable both output drivers (high-impedance mode).

Output Clock Frequencies

Frequency select bits are weakly tied high so if left unconnected the default setting will be [1] and the device will output the associated frequency highlighted in bold.

Freq (MHz)	Freq Select Bits [FS] - Default is [1]	
	0	1
CLK1	148.5	148.5
CLK2	148.5	148.5

Table 1. Pin-Selectable Output Frequencies

Absolute Maximum Ratings

Item	Min.	Max.	Units	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	VDD + 0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD				
HBM		4000	V	
MM		400		
CDM		1500		

1000+ years of data retention on internal memory

Specifications (Unless specified otherwise: T = 25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Supply Voltage ¹	VDD		2.25		3.6	V
Supply Current	IDD	OE pin low - output is disabled		21	23	mA
Supply Current ²	IDD	OE pin high - outputs are enabled RL = 500ohms, F01 = F02 = 156.25MHz		76		mA
Frequency Stability	ΔF	Includes frequency variation due to initial tolerance, temp. and power supply voltage			± 25	ppm
Aging	ΔF	First year (@ 25°C)			± 5	ppm
Startup Time ³	tSU	T = 25°C			5	ms
Input Logic Levels Input Logic High Input Logic Low	VIH VIL		0.75 x VDD -		- 0.25 x VDD	V
Output Disable Time ⁴	tDA				5	ns
Output Enable Time	tEN				20	ns
Pull-Up Resistor ²		Pull-up exists on all digital IO		40		kOhms
LVPECL Output						
Output Logic Levels Output Logic High Output Logic Low	VOH VOL	RL = 500ohms	VDD - 1.08 -		- VDD - 1.55	V
Pk to Pk Output Swing		Single-Ended		800		mV
Output Transition Time ⁴ Rise Time Fall Time	tR tF	20% to 80% RL = 500ohms		250		ps
Frequency	CLK1	[FS2, FS1, FS0] = [1, 1, 1]		148.5		MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter ⁵	JPER	F01 = F02 = 156.25MHz		2.5		psRMS
Integrated Phase Noise	JPH	200kHz to 20MHz @ 156.25MHz 100kHz to 20MHz @ 156.25MHz 12kHz to 20MHz @ 156.25MHz		0.25 0.38 1.7	2	psRMS
LVDS Output						
Output Offset Voltage		RL = 100ohms Differential	1.125		1.4	V
Delta Offset Voltage					50	mV
Pk to Pk Output Swing		Single-Ended		350		mV
Output Transition Time ⁴ Rise Time Fall Time	tR tF	20% to 80% RL = 500ohms, CL = 2pF (to GND)		200	350	ps
Frequency	CLK2	[FS2, FS1, FS0] = [1, 1, 1]		148.5		MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter ⁵	JPER	F01 = F02 = 156.25MHz		2.5		psRMS
Integrated Phase Noise	JPH	200kHz to 20MHz @ 156.25MHz 100kHz to 20MHz @ 156.25MHz 12kHz to 20MHz @ 156.25MHz		0.28 0.4 1.7	2	psRMS

1. Pin 12 VDD2, and pin 13 VDD should be filtered with 0.1uF capacitors.

2. Output is enabled if OE pin is floated or not connected.

3. tSU is time to 100ppm stable output frequency after VDD is applied and outputs are enabled.

4. Output Waveform and Test Circuit figures below define the parameters.

5. Period Jitter includes crosstalk from adjacent output.

Nominal Performance Parameters (Unless specified otherwise: T = 25°C, VDD = 3.3V)

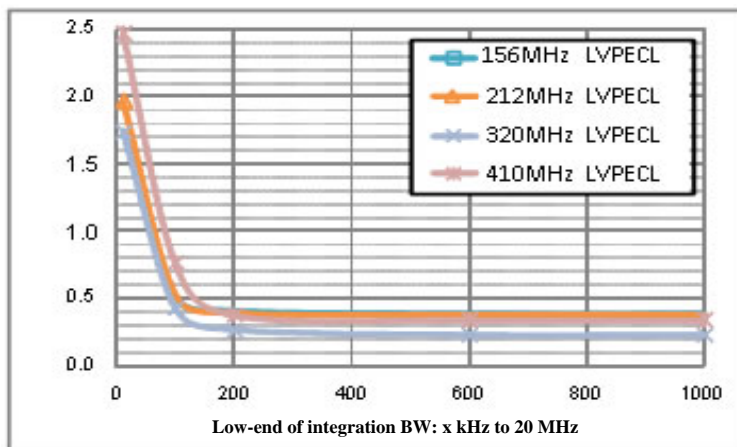


Figure 1. LVPECL Phase Jitter (integrated phase noise)

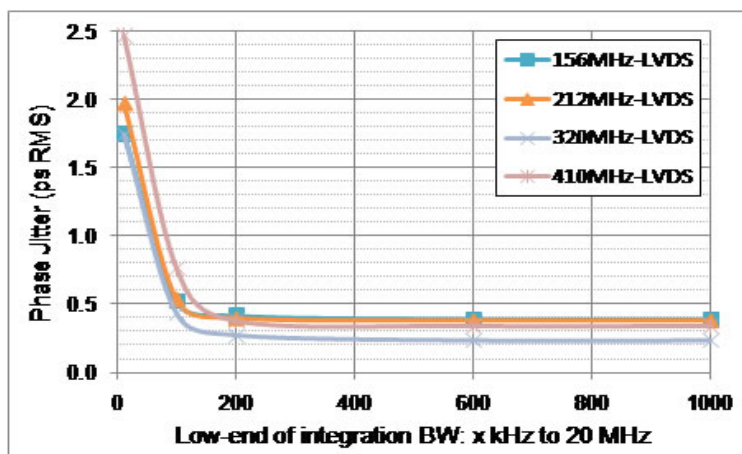


Figure 2. LVDS Phase Jitter (integrated phase noise)

LVPECL Output Waveform

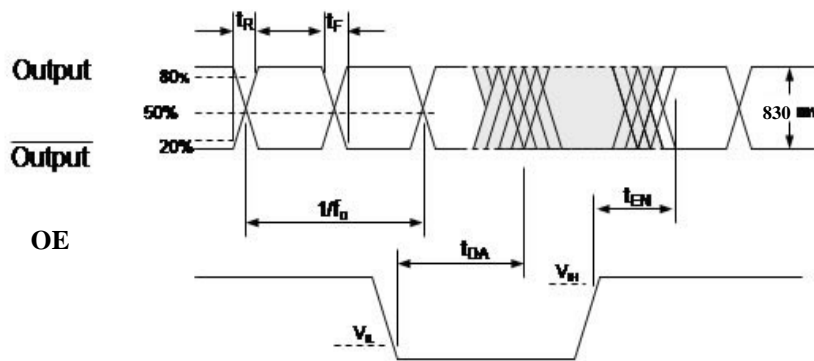


Figure 3. LVPECL Output Waveform

LVDS Output Waveform

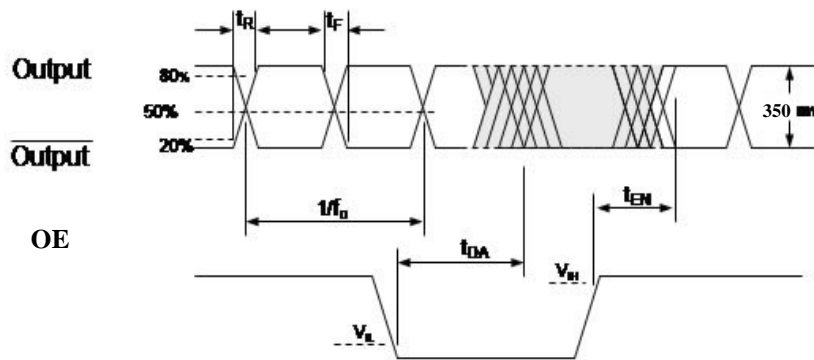


Figure 4. LVDS Output Waveform

MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/sec Max.
Preheat Time 150°C to 200°C	60 - 180 sec
Time maintained above 217°C	60 - 150 sec
Peak Temperature	255 - 260°C
Time within 5°C of actual Peak	20 - 40 sec
Ramp-Down Rate	6°C/sec Max.
Time 25°C to Peak Temperature	8 min Max.

Solder Reflow Profile

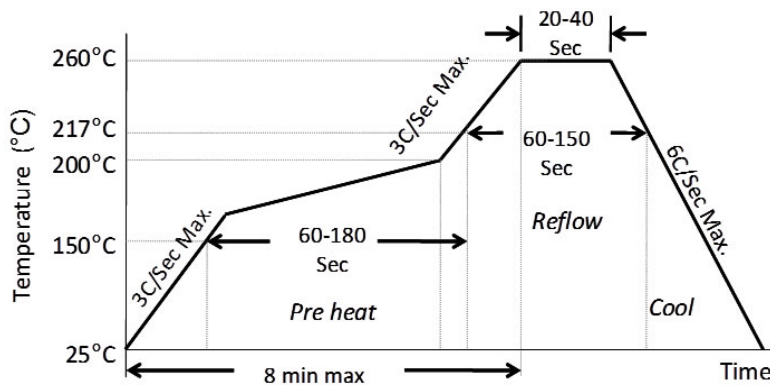
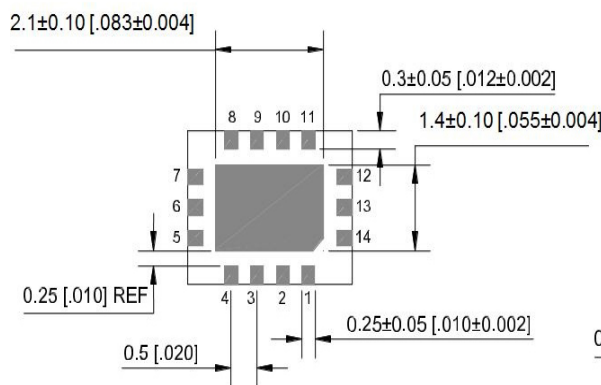
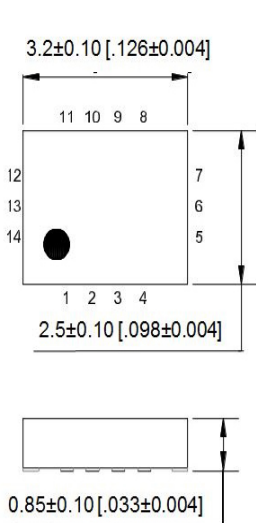


Figure 5. Solder Reflow Profile

Package Information⁷

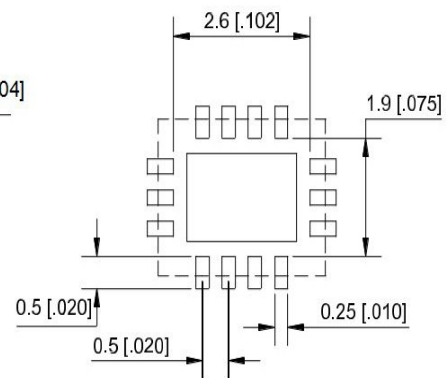
External Dimensions

units: mm[inch]



Recommended Solder Pad Layout

units: mm[inch]



3.2mm x 2.5mm 14 Lead Plastic Package

Notes:

- Connect the exposed die paddle to ground.
- Package information is correct as of the publication date. For updates and most current information, go to www.microchip.com.

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