34 V Input Synchronous Step-down DC / DC Controller Evaluation Board

NO.EEV-351-032A050-0500-220218

R1272S032A050-0500EV is the evaluation board for R1272 which has the below features, benefits and specifications.

OUTLINE

The R1272S is a step-down DC/DC controller which can generate an output voltage of 0.7 V to 5.3 V by driving external high- / low-side NMOSs. By the adoption of a unique current mode PWM architecture without an external current sense resistor, the R1272S can make up a stable DC/DC converter with high-efficiency even if adding low Ron MOSFETs and a low DCR inductor externally. And, by the frequency characteristics optimization with using external phase compensation capacitor, the R1272S can achieve a high-speed response to variations of input voltage and load current. The user-settable oscillation frequency is adjustable over a range of 250 kHz to 1 MHz(1) by external resistors, and also can be synchronized to an external clock.
Output Voltage Control Methods have three operating modes: Forced PWM mode, PLL_PWM mode, and PWM/VFM Auto-switching mode. These modes are selectable according to conditions of the MODE pin. Especially, the PWM/VFM Auto-switching mode can improve efficiency under light load conditions.
The R1272S can minimize the output voltage drop caused by an input voltage drop at cranking, with reducing the operating frequency (the lowest possible limit is a quarter of the frequency) so that the off-duty is reduced.
Protection functions include a current limit function, an UVLO (Under Voltage Lock Out) function, an OVP (Over Voltage Protection) function, a soft-start function, a low-inductor current shutdown function, and so on. Also, a power good function provides the status of output with using a power good (PGOOD) pin.
For EMI reduction, SSCG (Spread-Spectrum Clock Generator) for diffused oscillation frequency at the PWM operation is optionally available.

FEATURES

- Operating Voltage (Maximum Rating) ····· 4.0 V to 34 V (36 V)
- Operating Temperature Range ····· -40°C ≤ Ta ≤ 105°C
  (Usable in high-temperature environment)
- Start-up Voltage ····· 4.5 V
- Output Voltage ····· 5.0 V
- Feedback Voltage Tolerance ····· 0.64 V ± 1%
- Consumption Current at No Load (at VFM mode) ····· Typ.15 µA
- Adjustable Oscillation Frequency····· 500 kHz
- Synchronizable Clock Frequency··· ····· 250 kHz to 1 MHz
- Spreading Rate for SSCG ····· Typ. ±3.6%
- Minimum On-Time ··· ····· Typ.100 ns
- Minimum Off-Time ····· Typ.120 ns (at regulation mode)
  At dropout, actual minimum off-time is reduced.
- Adjustable Soft-start Time (1). ····· Typ.500 µs
- Pre-bias Start-up

(1)500 µs (Typ.) as a lower limit with using an external capacitor. Otherwise, available the tracking function through the application of an external voltage.

- Anti-phase Clock Output
- Thermal Shutdown Function ····· Tj = 160ºC (Typ.)
- Under Voltage Lockout (UVLO) Function····· ····· Typ. 3.3 V
- Over Voltage Detection (OVD) Function ····· FB pin voltage (V_{FB}) + 10% (Typ.)
  Detection/Release Hysteresis ····· FB pin voltage (V_{FB}) x 3% (Typ.)
- Under Voltage Detection (UVD) Function· ····· FB pin voltage (V_{FB}) - 10% (Typ.)
  Detection/Release Hysteresis ····· FB pin voltage (V_{FB}) x 3% (Typ.)
- Over-current Protection ····· Hiccup-mode / Latch mode
- Selectable Current Limit Threshold· ····· 70 mV
- Power Good Output ····· NMOS Open-drain Output
- Package· ····· HSOP-18
- For more details on R1272 IC, please refer to
  https://www.nisshinbo-microdevices.co.jp/en/pdf/datasheet/r1272-ea.pdf.

PART NUMBER INFORMATION

Product Name	Package
R1272S032A050-0500	HSOP-18

03: Combination of processing and function.

Over Current Protection	SSCG
Latch mode	Enable

2: 70 mV, Set Voltage for Current Limit Threshold (Typ.)

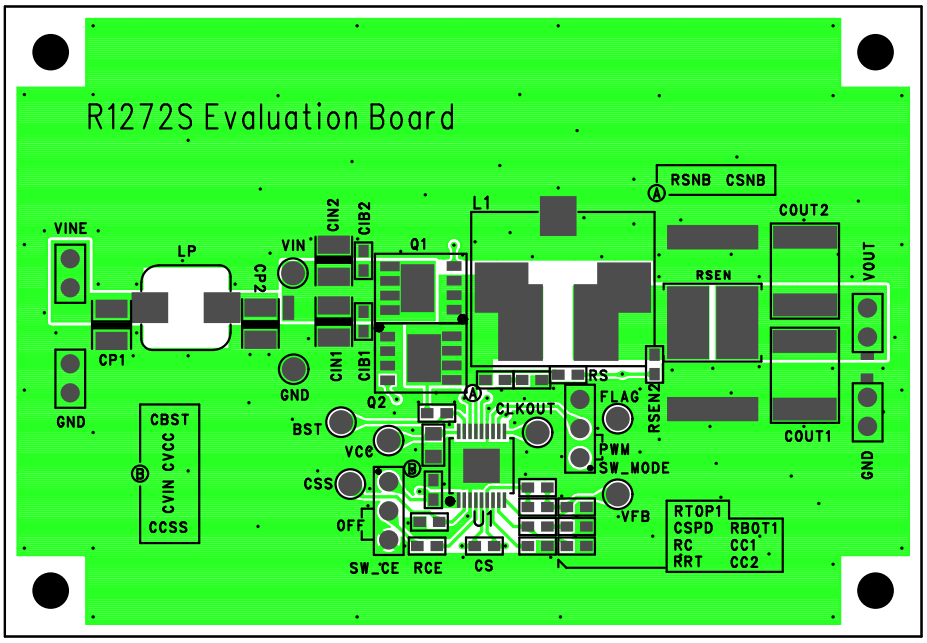
A: Fixed

050: 5.0 V, Output Voltage

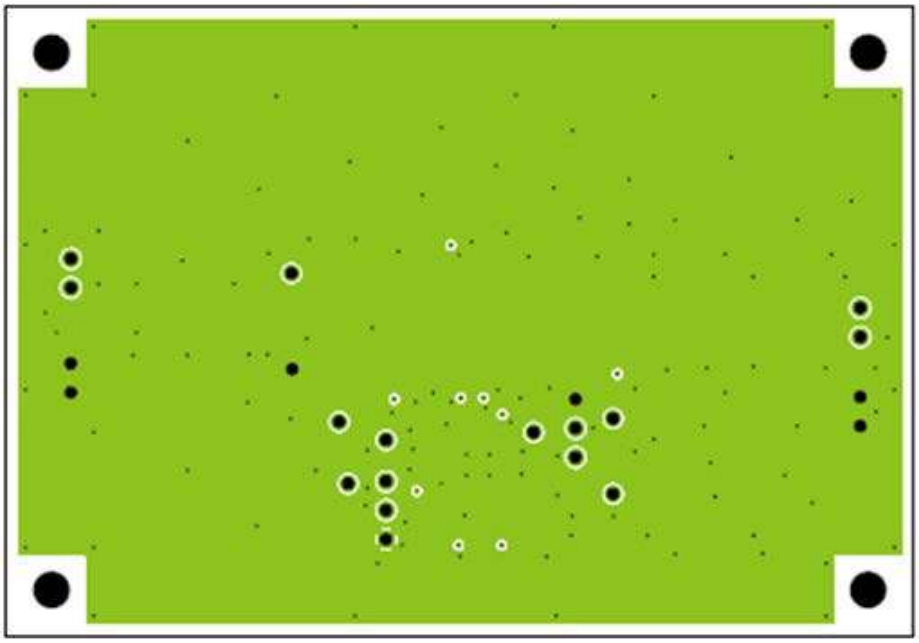
0500: 500 kHz, Frequency

PCB LAYOUT

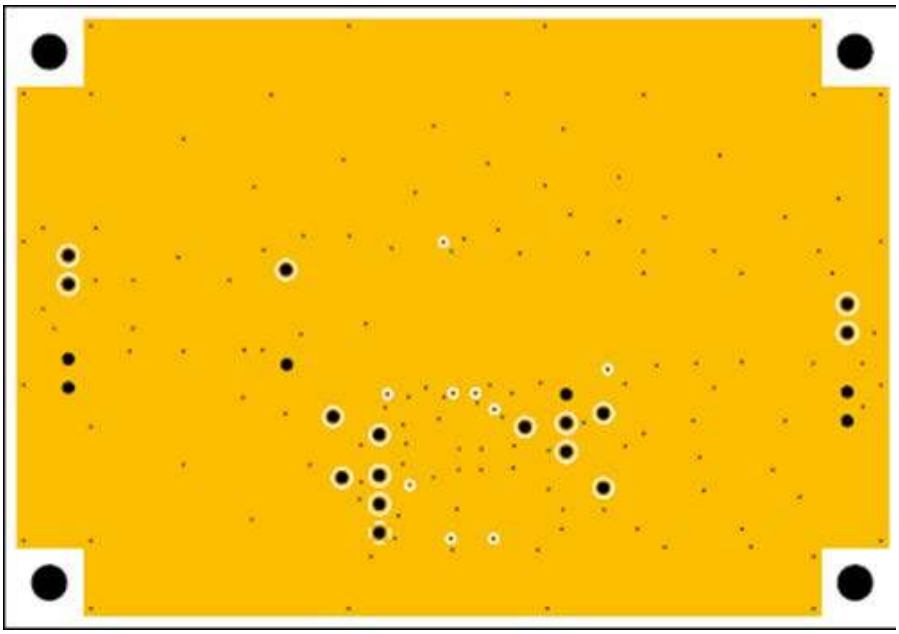
R1272SxxxA PCB Layouts



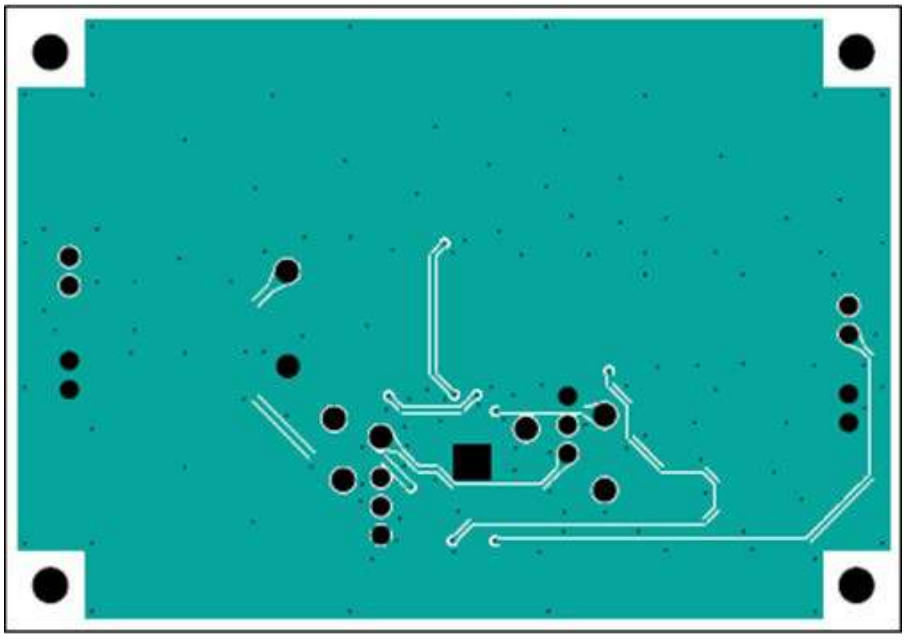
PCB Layout – 1st Layer (Top Layer)



PCB Layout – 2nd Layer



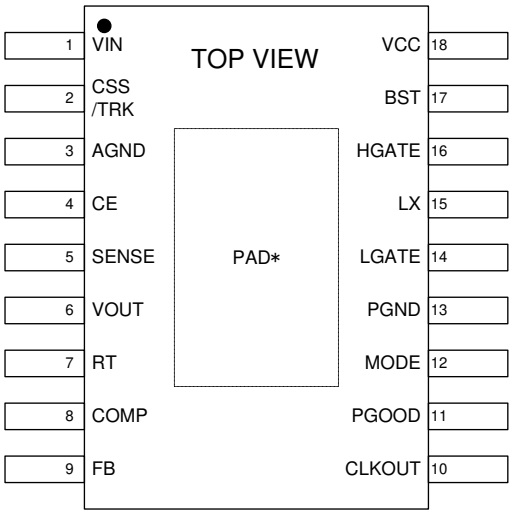
PCB Layout − 3rd Layer



PCB Layout − 4th Layer (Bottom Layer)
R1272SxxxA

PIN DESCRIPTIONS

HSOP-18



HSOP-18 Pin Description

Pin No.	Pin Name	Description
1	VIN	Power supply pin
2	CSS/TRK	Soft-start adjustment pin
3	AGND	Analog GND pin
4	CE	Chip enable pin (Active ”H”)
5	SENSE	Sense pin for inductor current
6	VOUT	Output voltage feedback input pin
7	RT	Oscillation adjustment pin
8	COMP	Capacitor connecting pin for phase compensation of error amplifier
9	FB	Feedback input pin to the error amplifier
10	CLKOUT	Clock output pin
11	PGOOD	Power-good output pin
12	MODE	Mode-set input pin
13	PGND	Power GND pin
14	LGATE	L-side FET control pin
15	LX	Switchingpin
16	HGATE	H-side FET control pin
17	BST	Boostrap pin
18	VCC	VCC output pin

∗ The tab on the bottom of the package must be electrically connected to GND (substrate level) when mounted on the board.

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V_{IN}	VIN pin voltage	-0.3 to 36	V
V_{CE}	CE pin voltage	-0.3 to 36	V
V_{CSS}/V_{TRK}	CSS/TRK pin voltage	-0.3 to 3	V
V_{OUT}	VOUTpin voltage	-0.3 to 6	V
V_{SENSE}	SENSEpin voltage	-0.3 to 6	V
V_{RT}	RT pin voltage	-0.3 to 3	V
V_{COMP}	COMP pin voltage(1)	-0.3 to 6	V
V_{FB}	FB pin voltage	-0.3 to 3	V
V_{CC}	VCC pin voltage	-0.3 to 6	V
	Output current for VCC pin	Internally limited	mA
V_{BST}	BST pin voltage	LX-0.3 to LX+6	V
V_{HGATE}	HGATE pin voltage	LX-0.3 to BST	V
V_{LX}	LX pin voltage(2)	-0.3 to 36	V
V_{LGATE}	LGATE pin voltage(1)	-0.3 to 6	V
V_{MODE}	MODE pin voltage	-0.3 to 6	V
V_{PGOOD}	PGOOD pin voltage	-0.3 to 6	V
V_{CLKOUT}	CLKOUT pin voltage(1)	-0.3 to 6	V
P_D	Power Dissipation(3) (HSOP-18, JEDEC STD.51-7 Test Land Pattern)	3100	mW
Tj	Junction Temperature	−40 to 125	°C
Tstg	Storage Temperature Range	−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field.
The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	4.0 to 34	V
Ta	Operating Temperature Range	−40 to 105	°C
V_{OUT}	Output Voltage Range	0.7 to 5.3	V

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) The pin voltage must be prevented from exceeding V_{CC} +0.3V.
(2) The pin voltage must be prevented from exceeding V_{IN} +0.3V.
(3) Refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, CE = V_{IN}, unless otherwise specified.

The specifications surrounded by [ ] are guaranteed by design engineering at -40°C ≤ Ta ≤ 105°C.

R1272SxxxA (Ta = 25°C)

Symbol	Item		Conditions	Min.	Typ.	Max.	Unit
V_{START}	Start-up Voltage					4.5	V
V_{CC}	VCC Pin Voltage (VCC–AGND)		V_{FB} = 0.672 V	4.9	5.1	5.3	V
$I_{STANDBY}$	Standby Current		V_{IN} = 34 V, CE = 0 V		3	20	µA
I_{VIN1}	VIN Consumption Current 1 at Switching Stop in PWM mode	R1272S0xx	V_{FB} = 0.672 V, MODE = 5 V, V_{OUT} = SENSE = LX = 5 V		1.0	1.3	mA
I_{VIN2}	VIN Consumption Current 2 at Switching Stop in VFM mode	R1272S0xx	V_{FB} = 0.672 V, MODE = 0 V V_{OUT} = SENSE = LX = 5 V		15	75	µA
V_{UVLO2}	UVLO Threshold Voltage		V_{CC} Rising	3.85	4.0	4.2	V
V_{UVLO1}			V_{CC} Falling	3.1	3.3	3.4	V
V_{FB}	FB Voltage Accuracy		Ta = 25°C	0.6336	0.64	0.6464	V
			-40°C ≤ Ta ≤ 105°C	0.6272		0.6528	
f_{OSC0}	Oscillation Frequency 0		RT = 135 kΩ	225	250	275	kHz
f_{OSC1}	Oscillation Frequency 1		RT = 32 kΩ	900	1000	1100	kHz
t_{OFF}	Minimum OFF Time		V_{IN} = 5 V, V_{OUT} = 5 V		120	190	ns
t_{ON}	Minimum ON Time				100	120	ns
f_{SYNC}	Synchronizing Frequency		f_{OSC} as the reference	fosc×0.5		fosc×1.5	kHz
				250		1000	
t_{SS1}	Soft-start Time 1		CSS / TRK = OPEN	0.4		0.75	ms
t_{SS2}	Soft-start Time 2		C_{SS} = 4.7 nF	1.4		2.0	ms
I_{TSS}	Charge Current for Soft-start Pin		CSS / TRK = 0 V	1.8	2	2.2	µA
V_{SSEND}	CSS/TRK Pin Voltage at End of Soft-start			V_{FB}	V_{FB} +0.03	V_{FB}+0.06	V
R_{DIS_CSS}	Discharge Resistance for CSS/TRK Pin		V_{IN} = 4.5 V, CE = 0 V, CSS / TRK = 3 V	2.0	3.0	5.0	kΩ
$R_{UPHGATE}$	On-resistance of Pull-up Transistor (HGATE Pin)		(BST – LX) = 5 V, I_{HGATE} = -100 mA		2.5	5.0	Ω

V_{IN} = 12 V, CE = V_{IN}, unless otherwise specified.

The specifications surrounded by [ ] are guaranteed by design engineering at -40°C ≤ Ta ≤ 105°C.

R1272SxxxA Continued (Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
$R_{DOWNHGATE}$	On-resistance of Pull-down Transistor (HGATE Pin)	(BST – LX) = 5 V, I_{HGATE} = 100 mA		1.5	3.5	Ω
$R_{UPLGATE}$	On-resistance of Pull-up Transistor (LGATE Pin)	(VCC – PGND) = 5 V, I_{LGATE} = -100 mA		4.0	7.0	Ω
$R_{DOWNLGATE}$	On-resistance of Pull-down Transistor (LGATE Pin)	(VCC – PGND) = 5 V, I_{LGATE} = 100 mA		1.5	3.5	Ω
V_{ILIMIT}	Current Limit Threshold Voltage (SENSE – VOUT)		40	50	60	mV
			60	70	80	mV
			90	100	110	mV
$V_{IREVLIMIT}$	Reverse Current Sense Threshold (SENSE – VOUT)	MODE = H / CLK	-35	-25	-15	mV
			-45	-35	-25	mV
			-60	-50	-40	mV
$V_{LXSHORTL}$	LX Shot to GND Detector Threshold Voltage (VIN – LX)		0.345	0.43	0.520	V
$V_{LXSHORTH}$	LX Short to VCC Detector Threshold Voltage (LX – PGND)		0.330	0.43	0.515	V
V_{CEH}	CE "High" Input Voltage		1.27			V
V_{CEL}	CE "Low" Input Voltage				1.14	V
I_{CEH}	CE "High" Input Current	CE = 34 V	0.20		2.45	µA
I_{CEL}	CE "Low" Input Current	CE = 0 V	-1.00	0	1.00	µA
I_{FBH}	FB "High" Input Current	V_{FB} = 3 V	-0.10		0.10	µA
I_{FBL}	FB "Low" Input Current	V_{FB} = 0 V	-0.10		0.10	µA
V_{MODEH}	MODE "High" Input Voltage		1.33			V
V_{MODEL}	MODE "Low" Input Voltage				0.74	V
I_{MODEH}	MODE "High" Input Current	MODE = 6 V	1.00		6.60	µA
I_{MODEL}	MODE "Low" Input Current	MODE = 0 V	-1.00	0	1.00	µA
$V_{CLKOUTH}$	CLKOUT Pin "High" Output Voltage	CLKOUT = Hi-z	4.7		V_{CC}	V
$V_{CLKOUTL}$	CLKOUT Pin "Low" Output Voltage	CLKOUT = Hi-z	0		0.1	V
T_{TSD}	Thermal Shutdown Threshold Temperature	Ta Rising	150	160		°C
T_{TSR}		Ta Falling	125	140		°C

V_{IN} = 12 V, CE = V_{IN}, unless otherwise specified.

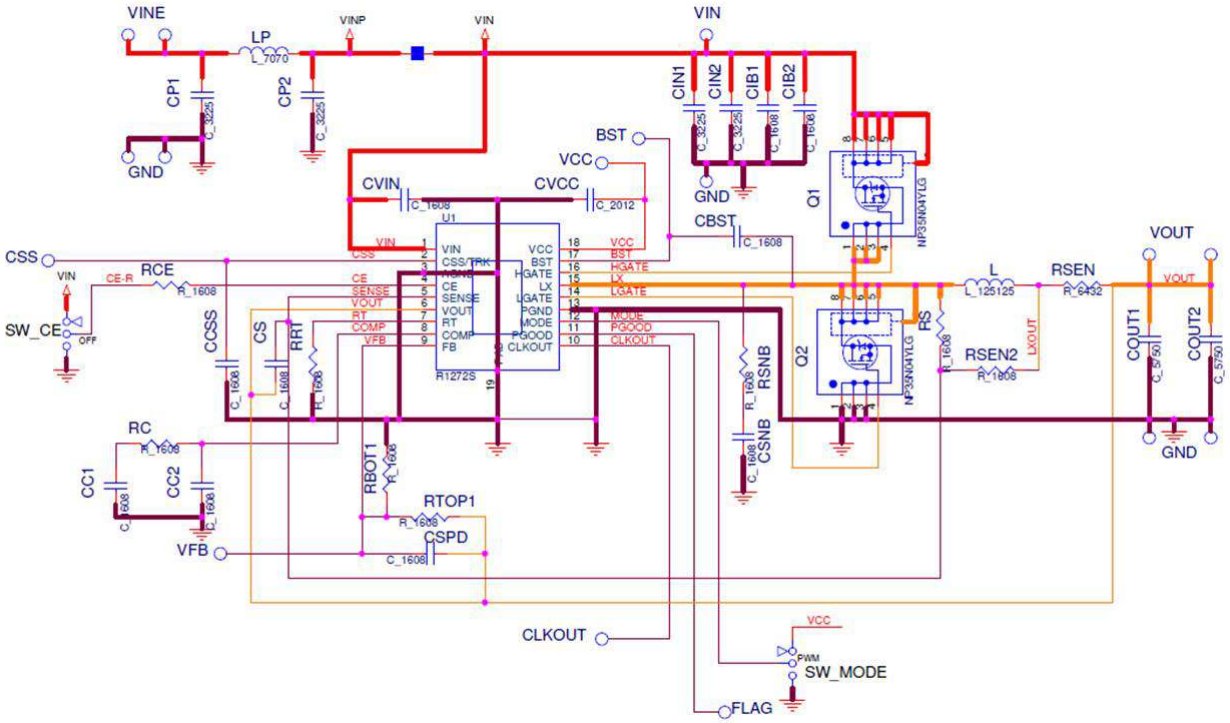
The specifications surrounded by [ ] are guaranteed by design engineering at -40°C ≤ Ta ≤ 105°C.

R1272SxxxA Continued (Ta = 25°C)

Symbol	Item	Conditions	Min..	Typ	Max.	Unit
$V_{PGOODOFF}$	PGOOD Pin "OFF" Voltage	V_{IN} = 4.0 V, PGOOD = 1 mA		0.26	[0.54]	V
$I_{PGOODOFF}$	PGOOD Pin "OFF" Current	V_{IN} = 34 V, CE = 0 V, PGOOD = 6 V	[-0.10]	0	[0.10]	µA
V_{FBOVD1}	FB Pin OVD Threshold Voltage	V_{FB} Rising	[0.680]	V_{FB}×1.10	[0.740]	V
V_{FBOVD2}		V_{FB} Falling	[0.664]	V_{FB}×1.07	[0.712]	V
V_{FBUVD1}	FB Pin UVD Threshold Voltage	V_{FB} Falling	[0.556]	V_{FB}×0.90	[0.604]	V
V_{FBUVD2}		V_{FB} Rising	[0.574]	V_{FB}×0.93	[0.628]	V
gm (EA)	Trans Conductance Amplifier	COMP = 1.5 V	[0.35]	1	[1.55]	mS

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

APPLICATION INFORMAITON



R1272SxxxA Typical Application Circuit at 500 kHz

R1272S032A050-0500 Recommended External Components(1)

CP1 [µF]	LP [µH]	CP2 [µF]	Q1(FET)	Q2(FET)	L [µH]	CIN1 [µF]	CIN2 [µF]
10	1.0	10	—	—	2.2	10	10
CVIN	COUT 1 [µF]	COUT2 [µF]	CBST [µF]	CVCC [µF]	CCSS [nF]	CSPD [pF]	CC1 [nF]
OPEN	100	22*2	0.22	2.2	3.3	150	3.3
CC2 [pF]	RTOP1 [kΩ]	RBOT1 [kΩ]	RC [kΩ]	RRT [kΩ]	RSEN [mΩ]	RSEN2 [kΩ]	RCE [Ω]
47	150	22	15	68	3	1	0

(1) The bill of materials will be attached on the shipment of each purchased evaluation board.

TECHNICAL NOTES

The performance of power source circuits using this IC largely depends on peripheral circuits. When selecting the peripheral components, please consider the conditions of use. Do not allow each component, PCB pattern or the IC to exceed their respected rated values (voltage, current, and power) when designing the peripheral circuits.

- External components must be connected as close as possible to the Ics and make wiring as short as possible. Especially, the capacitor connected in between VIN pin and GND pin must be wiring the shortest. If their impedance is high, internal voltage of the IC may shift by the switching current, and the operating may be unstable. Make the power supply and GND lines sufficient.

- Place a capacitor (C_{OUT}) to keep a distance between C_{IN} and C_{OUT} in order to avoid the high-frequency noise by input.

- AGND and PGND for the controller must be wired to the GND line at the low impedance point of the same layer with C_{IN} and C_{OUT}.

- Place a capacitor (C_{BST}) as close as possible to the LX pin and the BST pin. If controlling slew rate for EMI, a resistor (R_{BST}) should be in series between the BST pin and the capacitor (C_{BST}), but not be in series to FET for HGATE and LGATE pins. Because connecting the resistor in series to the FET becomes a cause of a through-current.

- The tab on the bottom of the HSOP-18 package must be connected to GND when mounted on the board. To improve thermal dissipation on the multilayer board, set via to release the heat to the other layer in the connecting part of the tab on the bottom. Likewise, thermal dissipation for FET is required.

- The MODE pin requires the H / L voltages with the high stability when the forced PWM mode (MODE = “H”) or the VFM mode (MODE = “L”) is enabled. If the voltage with the high stability cannot be applied, connection to the VCC pin as “H” level or the AGND pin as “L” level is recommended. If connecting to the PGND pin as noisy, a malfunction may occur. Avoid the use of the MODE pin being “Open”.

- If V_{OUT} is a minus potential, the setup cannot occur.

- The power for the controller and for the high-side FET must be used on the same power supply, since the internal slope compensation is applied as the power supply voltage of the high-side FET is equal to the controller’s. If applying the other power supply voltage, the controller will become unstable owing to the inappropriate slope compensation.

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