

# SN54LV125, SN74LV125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCES003B – NOVEMBER 1994 – REVISED APRIL 1996

- **EPIC™ (Enhanced-Performance Implanted CMOS) 2- $\mu$  Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$**
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

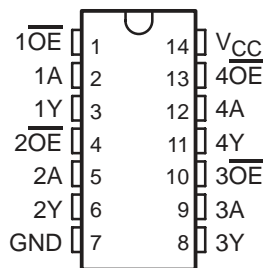
## description

These quadruple bus buffer gates are designed for 2.7-V to 5.5-V  $V_{CC}$  operation.

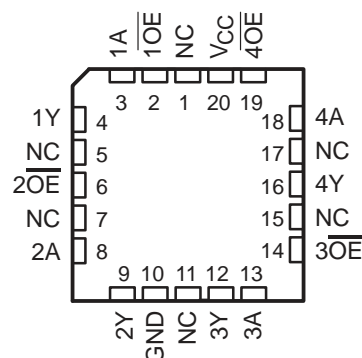
The 'LV125 feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ( $\overline{OE}$ ) input is high.

The SN54LV125 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LV125 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54LV125 . . . J OR W PACKAGE  
SN74LV125 . . . D, DB, OR PW PACKAGE  
(TOP VIEW)



SN54LV125 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z



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 **TEXAS  
INSTRUMENTS**

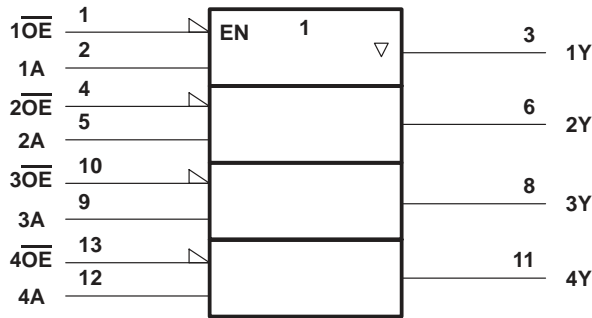
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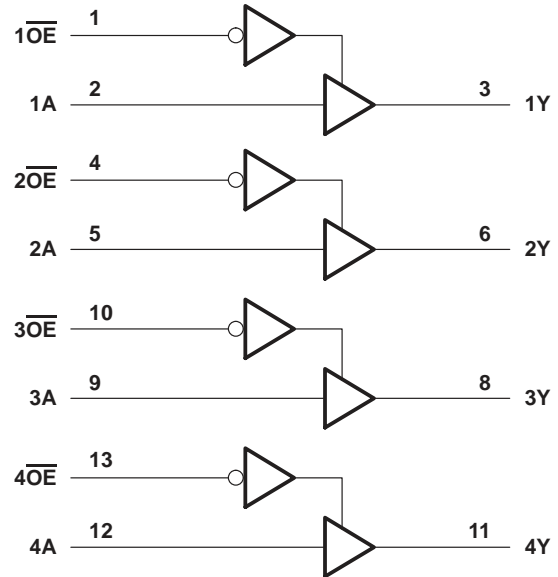
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for D, DB, J, PW, and W packages.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 35$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 70$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3):	
D package .....	1.25 W
DB or PW package .....	0.5 W
Operating free-air temperature range, $T_A$ .....	$-40^\circ\text{C}$ to $85^\circ\text{C}$
Storage temperature range, $T_{stg}$ .....	$-65^\circ\text{C}$ to $150^\circ\text{C}$

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. This value is limited to 7 V maximum.
  3. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils.

# SN54LV125, SN74LV125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 4)

		SN54LV125		SN74LV125		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	5.5	2.7	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		2		V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		3.15		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8		V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		1.65		
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		-8		mA
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		-16		
$I_{OL}$	Low-level output current	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		8		mA
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		16		
$\Delta t/\Delta V$	Input transition rise or fall rate	0	100	0	100	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}^\dagger$	SN54LV125		SN74LV125		UNIT
			MIN	TYP <sup>†</sup> MAX	MIN	TYP <sup>†</sup> MAX	
$V_{OH}$	$I_{OH} = -100\ \mu\text{A}$	MIN to MAX <sup>‡</sup>	$V_{CC}-0.2$		$V_{CC}-0.2$		V
	$I_{OH} = -8\ \text{mA}$	3 V	2.4		2.4		
	$I_{OH} = -16\ \text{mA}$	4.5 V	3.6		3.6		
$V_{OL}$	$I_{OL} = 100\ \mu\text{A}$	MIN to MAX <sup>‡</sup>	0.2		0.2		V
	$I_{OL} = 8\ \text{mA}$	3 V	0.4		0.4		
	$I_{OL} = 16\ \text{mA}$	4.5 V	0.55		0.55		
$I_I$	$V_I = V_{CC}$ or GND	3.6 V	$\pm 1$		$\pm 1$		$\mu\text{A}$
		5.5 V	$\pm 1$		$\pm 1$		
$I_{OZ}$	$V_O = V_{CC}$ or GND	3.6 V	$\pm 5$		$\pm 5$		$\mu\text{A}$
		5.5 V	$\pm 5$		$\pm 5$		
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	20		20		$\mu\text{A}$
		5.5 V	20		20		
$\Delta I_{CC}$	One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND	3 V to 3.6 V	500		500		$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	3.3 V	3.5		3.5		pF
		5 V	3.5		3.5		
$C_o$	$V_O = V_{CC}$ or GND	3.3 V	8		8		pF
		5 V	8		8		

<sup>†</sup> All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

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# SN54LV125, SN74LV125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV125						UNIT		
			$V_{CC} = 5.5 V \pm 0.5 V$			$V_{CC} = 3.3 V \pm 0.3 V$				$V_{CC} = 2.7 V$	
			MIN	TYP†	MAX	MIN	TYP†	MAX		MIN	MAX
$t_{pd}$	A	Y	7	18		9	19		23	ns	
$t_{en}$	$\overline{OE}$	Y	5	19		7	25		31	ns	
$t_{dis}$	$\overline{OE}$	Y	7	17		9	23		28	ns	

† All typical values are at  $V_{CC} = 3.3 V$ ,  $T_A = 25^\circ C$ .

switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV125						UNIT		
			$V_{CC} = 5.5 V \pm 0.5 V$			$V_{CC} = 3.3 V \pm 0.3 V$				$V_{CC} = 2.7 V$	
			MIN	TYP†	MAX	MIN	TYP†	MAX		MIN	MAX
$t_{pd}$	A	Y	7	18		9	19		23	ns	
$t_{en}$	$\overline{OE}$	Y	5	19		7	25		31	ns	
$t_{dis}$	$\overline{OE}$	Y	7	17		9	23		28	ns	

† All typical values are at  $V_{CC} = 3.3 V$ ,  $T_A = 25^\circ C$ .

operating characteristics,  $T_A = 25^\circ C$

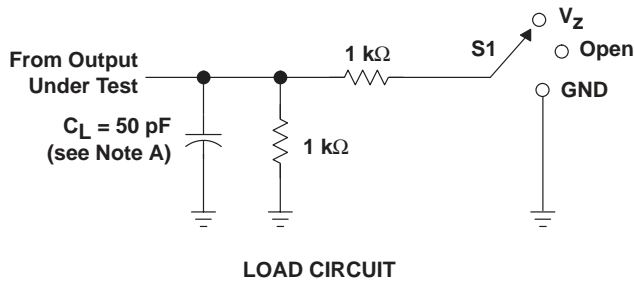
PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50$ pF, $f = 10$ MHz	3.3 V	45	pF
				5	
			5 V	48	pF
				5	

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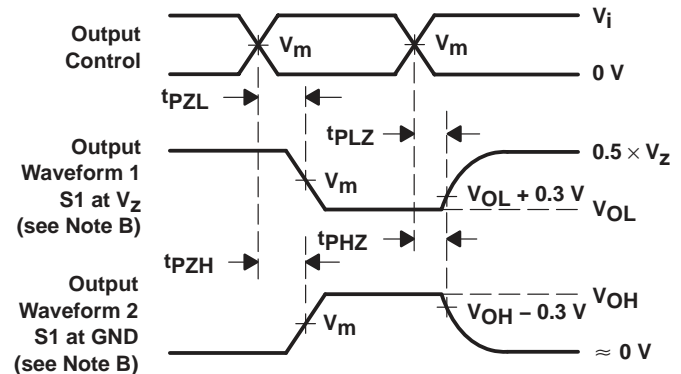
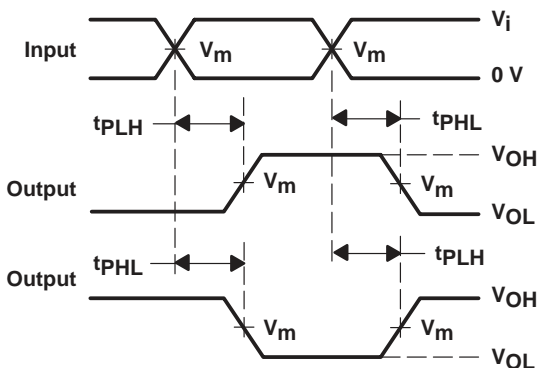
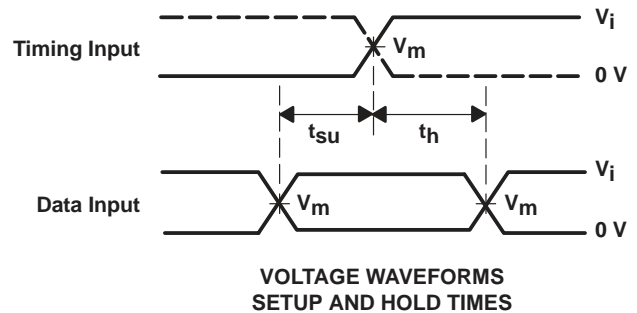
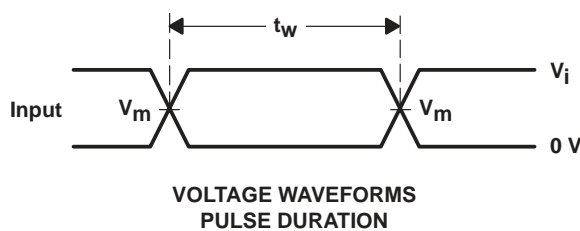
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>Z</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

WAVEFORM CONDITION	V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> = 2.7 V to 3.6 V
V <sub>m</sub>	0.5 × V <sub>CC</sub>	1.5 V
V <sub>i</sub>	V <sub>CC</sub>	2.7 V
V <sub>Z</sub>	2 × V <sub>CC</sub>	6 V



- NOTES:
- C<sub>L</sub> includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - The outputs are measured one at a time with one transition per measurement.
  - t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74LV125D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	Samples Not Available
SN74LV125DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	Samples Not Available
SN74LV125DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	Samples Not Available
SN74LV125PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	Samples Not Available

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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