User's Guide

TPS54620 Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains background information for the TPS54620 as well as support documentation for the TPS54620EVM-374 evaluation module (HPA374). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54620EVM-374.

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1 Introduction

1.1 Background

The TPS54620 dc/dc converter is designed to provide up to a 6 A output. The TPS54620 implements a split input power rails with separate input voltage inputs for the power stage and control circuitry. The power stage input (PVIN) is rated for 1.6 V to 17 V while the control input (VIN) is rated for 4.5 to 17 V. The TPS54620EVM-374 provides both inputs but is designed and tested using the PVIN connected to VIN. Rated input voltage and output current range for the evaluation module are given in Table 1-1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54620 regulator. The switching frequency is externally set at a nominal
480 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS54620 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS54620 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54620 provides adjustable slow start, tracking and undervoltage lockout inputs. The absolute maximum input voltage is 20 V for the TPS54620EVM-374.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54620EVM-374	VIN = 8 V to 17 V (VIN start voltage = 6.521 V)	0 A to 6 A

1.2 Performance Specification Summary

A summary of the TPS54620EVM-374 performance specifications is provided in Table 1-2. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 3.3 V, unless otherwise specified. The TPS54620EVM-374 is designed and tested for V_{IN} = 8 V to 17 V with the VIN and PVIN pins connect together with the J3 jumper. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 1-2. TPS54620EVM-374 Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range (PVIN = VIN)			8	12	17	V
V_{IN} start voltage				6.521		V
V_{IN} stop voltage				6.065		V
Output voltage set point				3.3		V
Output current range	V_{IN} = 8 V to 17 V		0		6	A
Line regulation	I_O = 3 A, V_{IN} = 8 V to 17 V			±0.02%		
Load regulation	V_{IN} = 12 V, I_O = 0 A to 6 A			±0.012%		
Load transient response	I_O = 1.5 A to 4.5 A	Voltage change		–100		mV
		Recovery time		60		µs
	I_O = 4.5 A to 1.5 A	Voltage change		100		mV
		Recovery time		120		µs
Loop bandwidth	V_{IN} = 12 V, I_O = 6 A			43		kHz
Phase margin	V_{IN} = 12 V , I_O = 6 A			52		°
Input ripple voltage	I_O = 6 A			520		mVPP
Output ripple voltage	I_O = 6 A			20		mVPP
Output rise time				4		ms
Operating frequency				480		kHz
Maximum efficiency	TPS54620EVM-374 , V_{IN} = 8 V, I_O = 2 A			95%		

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54620. Some modifications can be made to this module.

1.3.1 Output Voltage Set Point

The output voltage is set by the resistor divider network of R8 and R9. R9 is fixed at 10 kΩ. To change the output voltage of the EVM, it is necessary to change the value of resistor R8. Changing the value of R8 can change the output voltage above 0.8 V. The value of R8 for a specific output voltage can be calculated using Equation 1.

$$R8 = \frac{10\,k\Omega\,(V_{OUT} - 0.8\,V)}{0.8\,V} \tag{1}$$

Table 1-3 lists the R8 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 120 ns, and the maximum duty cycle is less than 95%. The values given in Table 1-3 are standard values, not the exact value calculated using Equation 1.

Table 1-3. Output Voltages Available

Output Voltage (V)	R8 Value (kΩ)
1.8	12.4
2.5	21.5
3.3	31.6
5	52.3

1.3.2 Slow Start Time

The slow start time can be adjusted by changing the value of C7. Use Equation 2 to calculate the required value of C7 for a desired slow start time

$$C7(nF) = \frac{Tss(ms) \times Iss(\mu A)}{Vref(V)} \tag{2}$$

The EVM is set for a slow start time of 4 msec using C7 = 0.01 µF.

1.3.3 Track In

The TPS54620 can track an external voltage during start up. The J5 connector is provided to allow connection to that external voltage. Ratio-metric or simultaneous tracking can be implemented using resistor divider R5 and R6. See the TPS54620 data sheet (SLVS949) for details.

1.3.4 Adjustable UVLO

The under voltage lock out (UVLO) ca be adjusted externally using R1 and R2. The EVM is st for a start voltage of 6.521 V and a stop voltage of 6.065 V using R1 = 35.7 kΩ and R2 = 8.06 kΩ. Use Equation 3 and Equation 4 to calculate required resistor values for different start and stop voltages.

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \tag{3}$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \tag{4}$$

1.3.5 Input Voltage Rails

The EVM is designed to accommodate different input voltage levels for the power stage and control logic. During normal operation, the PVIN and VIN inputs are connected together using a jumper across J3. The single input voltage is supplied at J1. If desired, these to input voltage rails may be separated by removing the jumper across J3. Two input voltages must then be provided at both J1 and J2.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54620EVM-374 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input / Output Connections

The TPS54620EVM-374 is provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying 4 A must be connected to J1 through a pair of 20 AWG wires. The jumper across J3 must be in place. See Section 1.3.5 for split input voltage rail operation. The load must be connected to J7 through a pair of 20 AWG wires. The maximum load current capability must be 6 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP8 is used to monitor the output voltage with TP9 as the ground reference.

Table 2-1. EVM Connectors and Test Points

Reference Designator	Function
J1	PVIN input voltage connector. (see Table 1-1 for V_{IN} range).
J2	VIN input voltage connector. Not normally used.
J3	PVIN to VIN jumper. Normally closed to tie VIN to PVIN for common rail voltage operation.
J24	2-pin header for enable. Connect EN to ground to disable, open to enable.
J5	2-pin header for tracking voltage input and ground.
J6	2-pin header for tracking output and ground.
J7	V_{OUT}, 3.3 V at 6 A maximum.
TP1	PVIN test point at PVIN connector.
TP2	GND test point at PVIN connector.
TP3	VIN test point at VIN connector.
TP4	GND test point at VIN connector.
TP5	PH test point.
TP6	Slow start / track in test point.
TP7	Test point between voltage divider network and output. Used for loop response measurements.
TP8	Output voltage test point at VOUT connector
TP9	GND test point at VOUT connector
TP10	PWRGD test point.

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 2 A and then decreases as the load current increases towards full load. Figure 2-1 shows the efficiency for the TPS54620EVM-374 at an ambient temperature of 25°C.

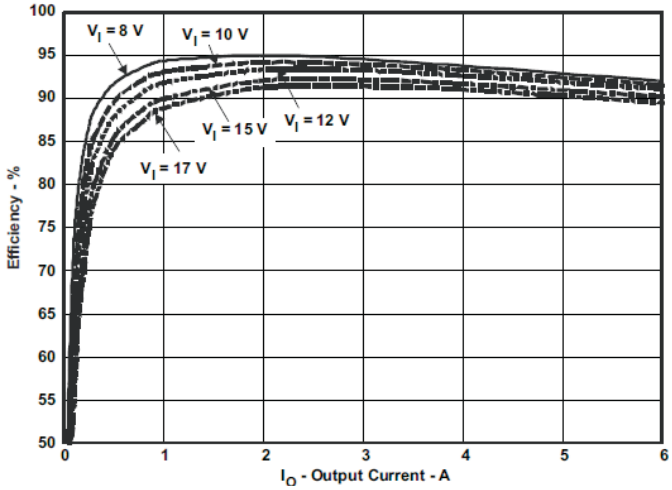

Figure 2-1. TPS54620EVM-374 Efficiency

Figure 2-2 shows the efficiency for the TPS54620EVM-374 at lower output currents below 0.10 A at an ambient temperature of 25°C.

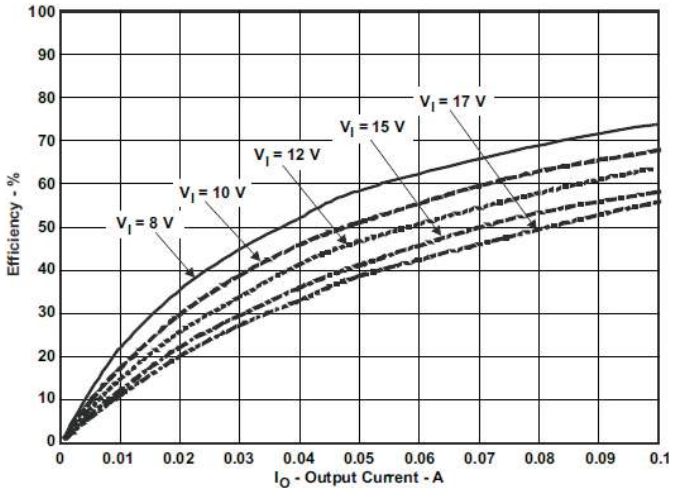

Figure 2-2. TPS54620EVM-374 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

Figure 2-3 shows the load regulation for the TPS54620EVM-374.

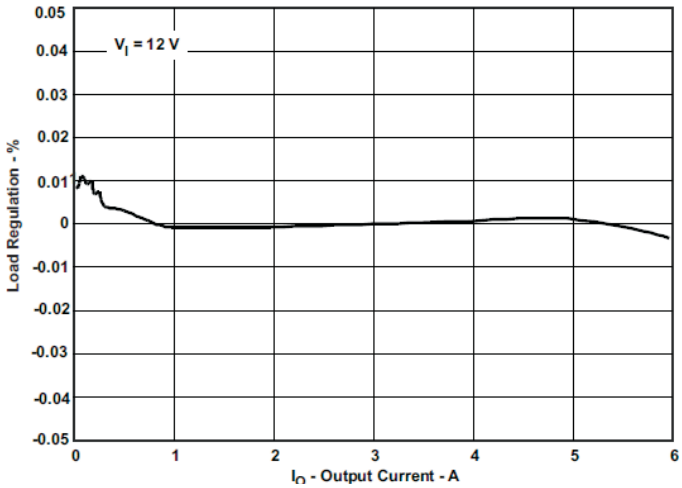

Figure 2-3. TPS54620EVM-374 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

Figure 2-4 shows the line regulation for the TPS54620EVM-374.

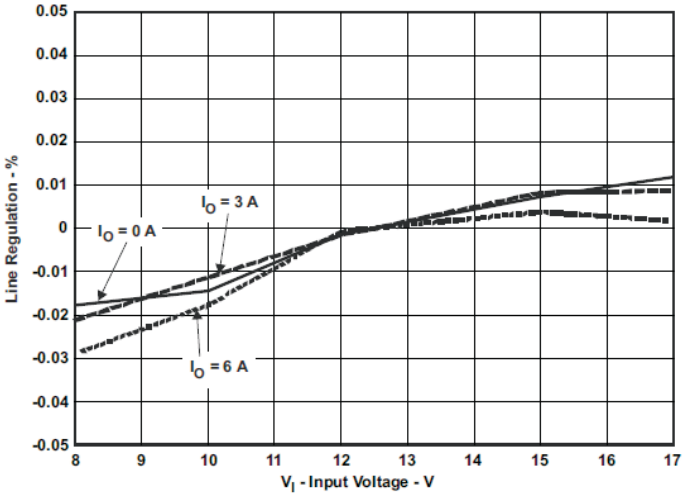

Figure 2-4. TPS54620EVM-374 Line Regulation

2.5 Load Transients

Figure 2-5 shows the TPS54620EVM-374 response to load transients. The current step is from 25% to 75% of maximum rated load at 12 V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

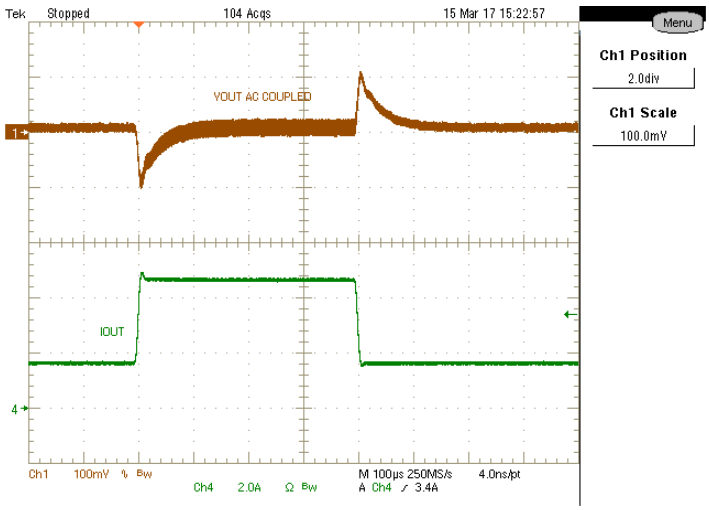

Figure 2-5. TPS54620EVM-374 Transient Response

2.6 Loop Characteristics

Figure 2-6 shows the TPS54620EVM-374 loop-response characteristics. Gain and phase plots are shown for V_{IN} voltage of 12 V. Load current for the measurement is 6 A.

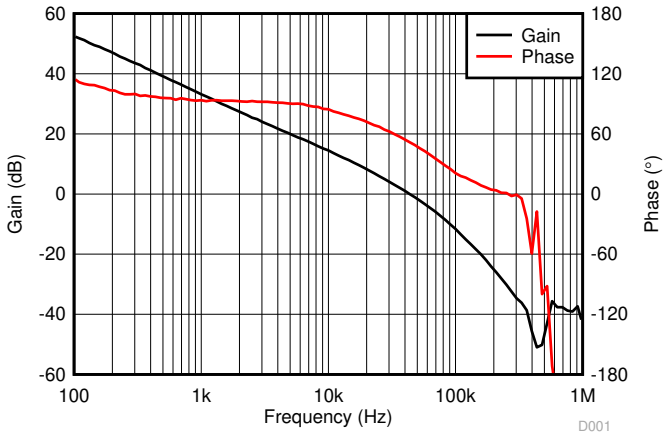

Figure 2-6. TPS54620EVM-374 Loop Response

2.7 Output Voltage Ripple

Figure 2-7 shows the TPS54620EVM-374 output voltage ripple. The output current is the rated full load of 6 A and V_{IN} = 12 V. The ripple voltage is measured directly across the output capacitors.

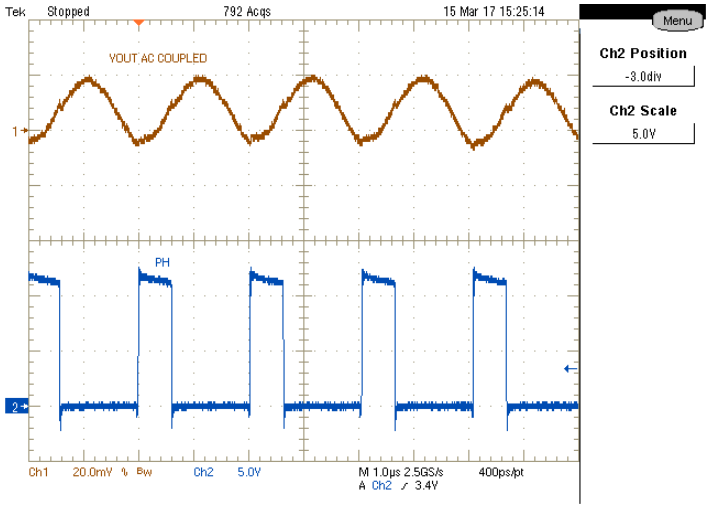

Figure 2-7. TPS54620EVM-374 Output Ripple

2.8 Input Voltage Ripple

Figure 2-8 shows the TPS54620EVM-374 input voltage. The output current is the rated full load of 4 A and V_{IN} = 12 V. The ripple voltage is measured directly across the input capacitors.

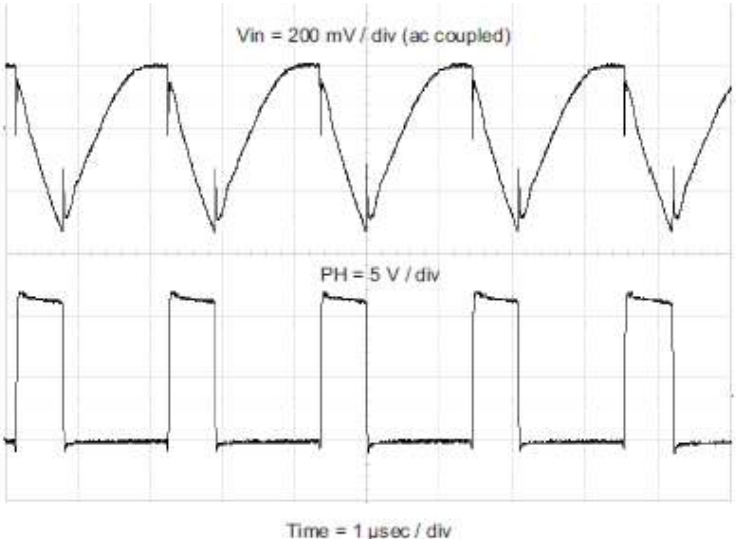

Figure 2-8. TPS54620EVM-374 Input Ripple

2.9 Powering Up

Figure 2-9 and Figure 2-10 show the start-up waveforms for the TPS54620EVM-374 . In Figure 2-9, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R1 and R2 resistor divider network. In Figure 2-10, the input voltage is initially applied and the output is inhibited by using a jumper at J2 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 3.3 V. The input voltage for these plots is 12 V and the load is 1Ω.

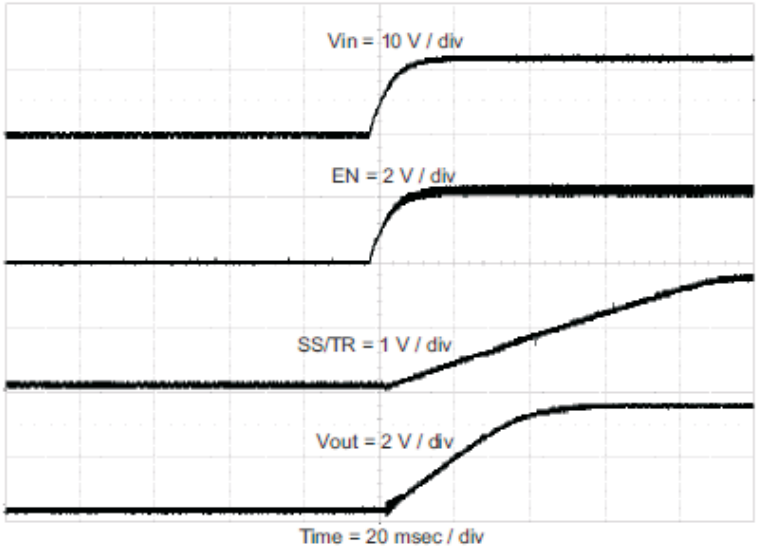

Figure 2-9. TPS54620EVM-374 Start-Up Relative to V_{IN}

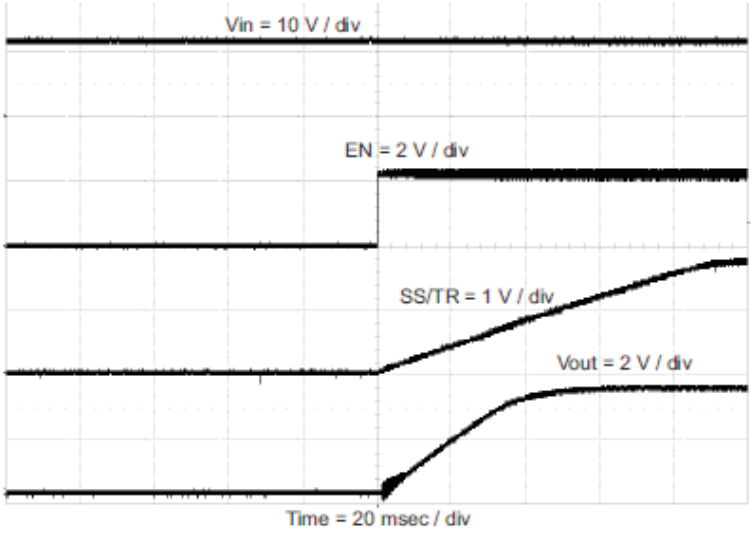

Figure 2-10. TPS54620EVM-374 Start-up Relative to Enable

2.10 Thermal Characteristics

This section shows a thermal image of the TPS54620EVM-374 running at 12 V input and 6 A load. there is no air flow and the ambient temperature is 25°C. The peak temperature of the IC (70°C) is well below the maximum recommended operating condition listed in the data sheet of 150°C.

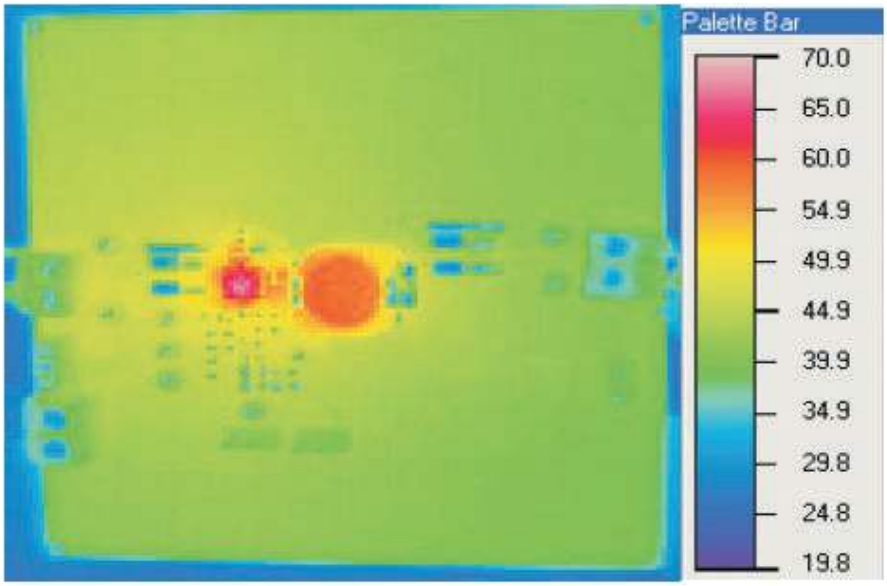

Figure 2-11. TPS54620EVM-374 Thermal Image

3 Board Layout

This section provides a description of the TPS54620EVM-374 , board layout, and layer illustrations.

3.1 Layout

The board layout for the TPS54620EVM-374 is shown in Figure 3-1 through Figure 3-5. The topside layer of the EVM is laid out in a manner typical of a user application. The top, bottom and internal layers are 2-oz. copper.

The top layer contains the main power traces for PVIN, VIN, V_{OUT}, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54620 and a large area filled with ground. The bottom and internal ground layers contains ground planes only. The top side ground traces are connected to the bottom and internal ground planes with multiple vias placed around the board including two vias directly under the TPS54620 device to provide a thermal path from the top-side ground plane to the bottom-side ground plane.

The input decoupling capacitors (C2, and C3) and bootstrap capacitor (C5) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace at the J7 output connector. For the TPS54620, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply. Critical analog circuits such as the voltage setpoint divider, frequency set resistor, slow start capacitor and compensation components are terminated to ground using a wide ground trace separate from the power ground pour.

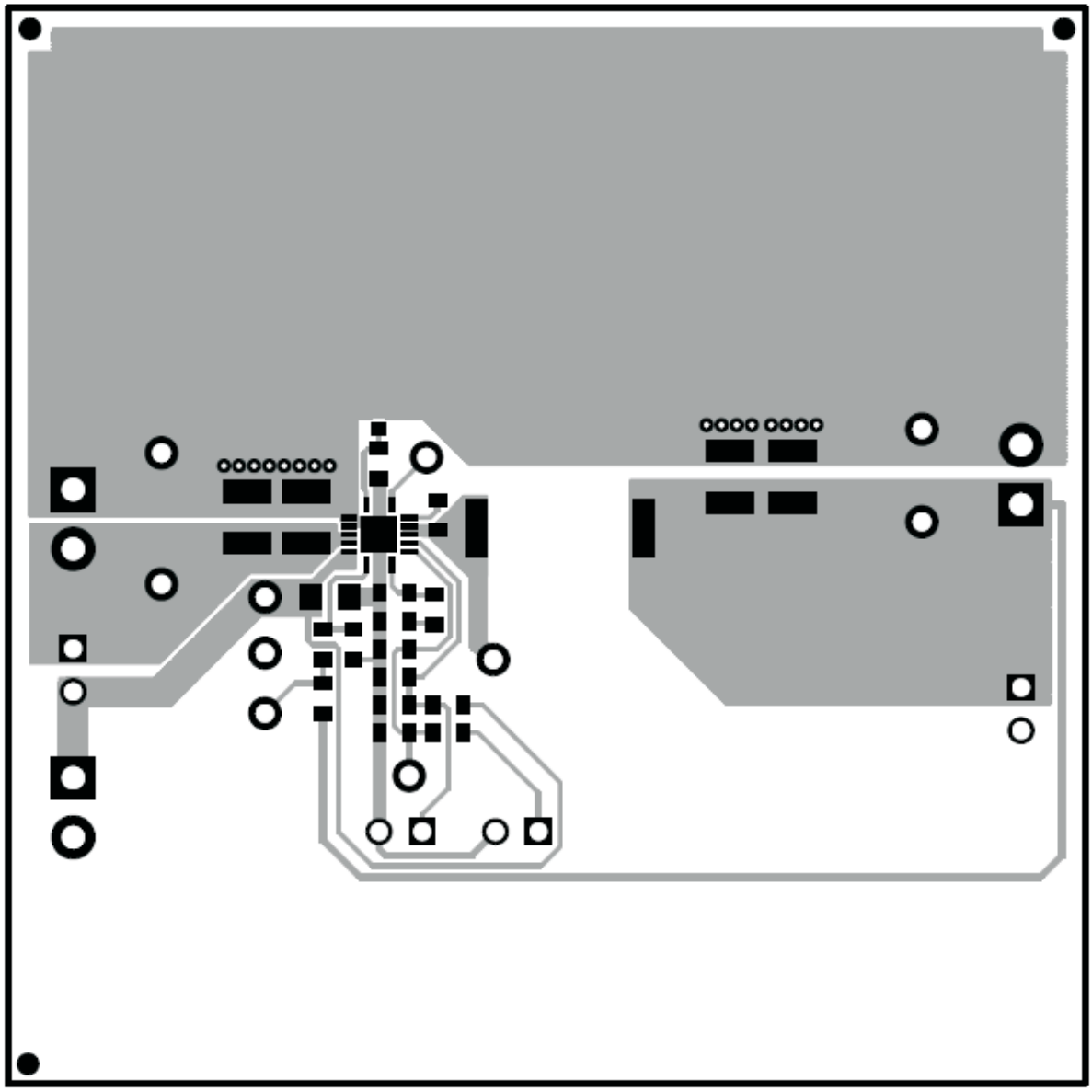

Figure 3-1. TPS54620EVM-374 Top-Side Layout

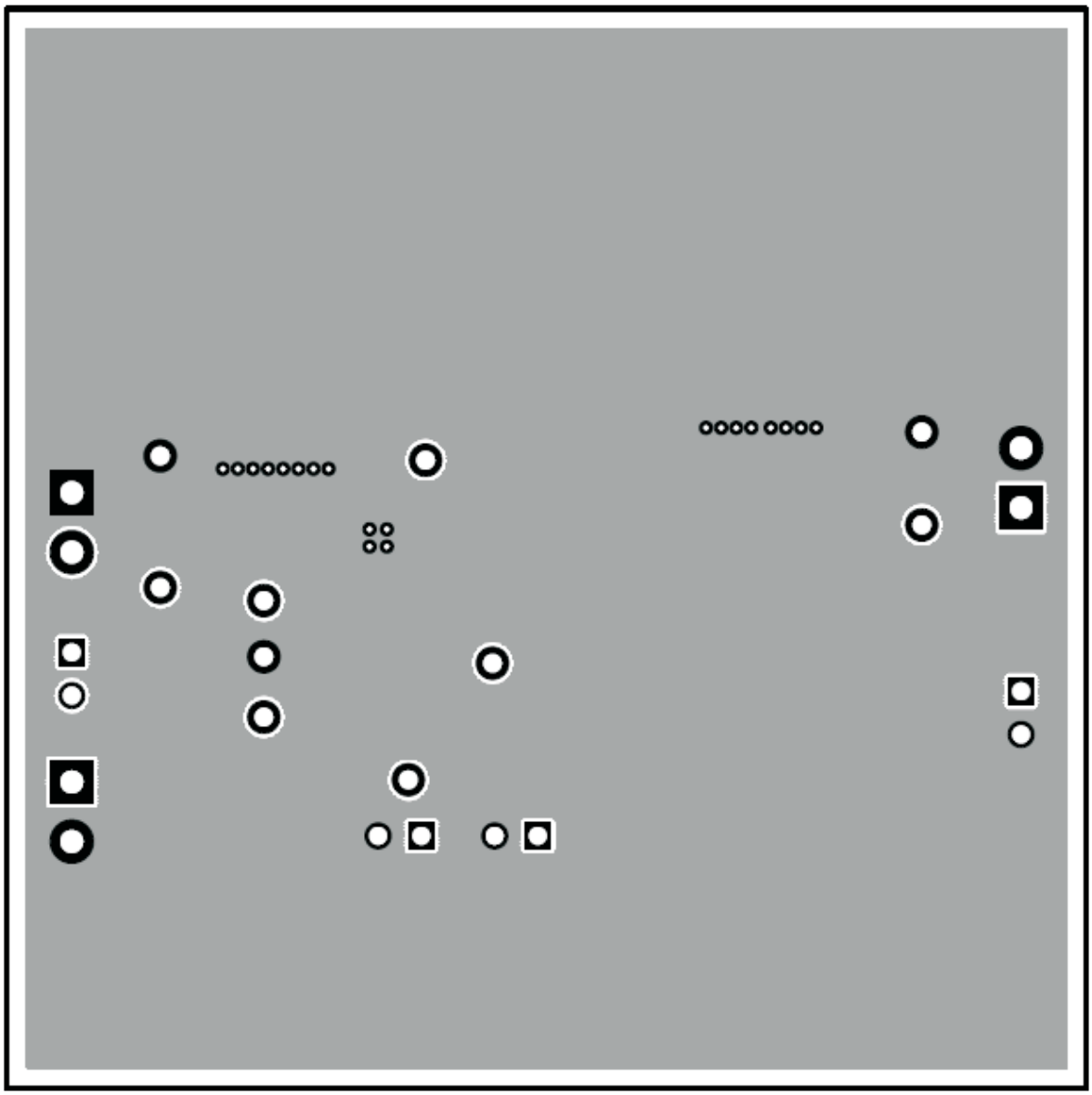

Figure 3-2. TPS54620EVM-374 Layout 2

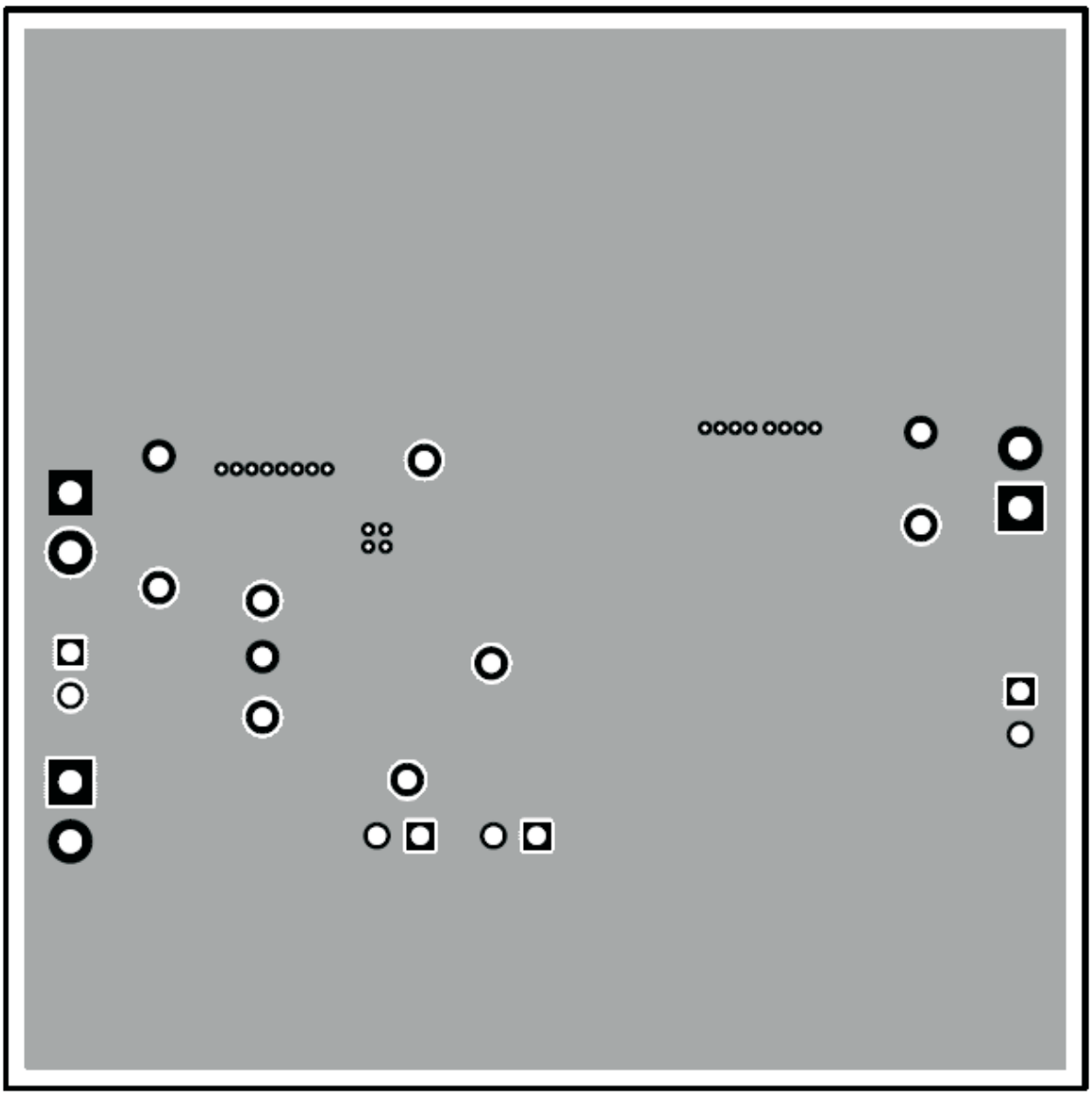

Figure 3-3. TPS54620EVM-374 Layout 3

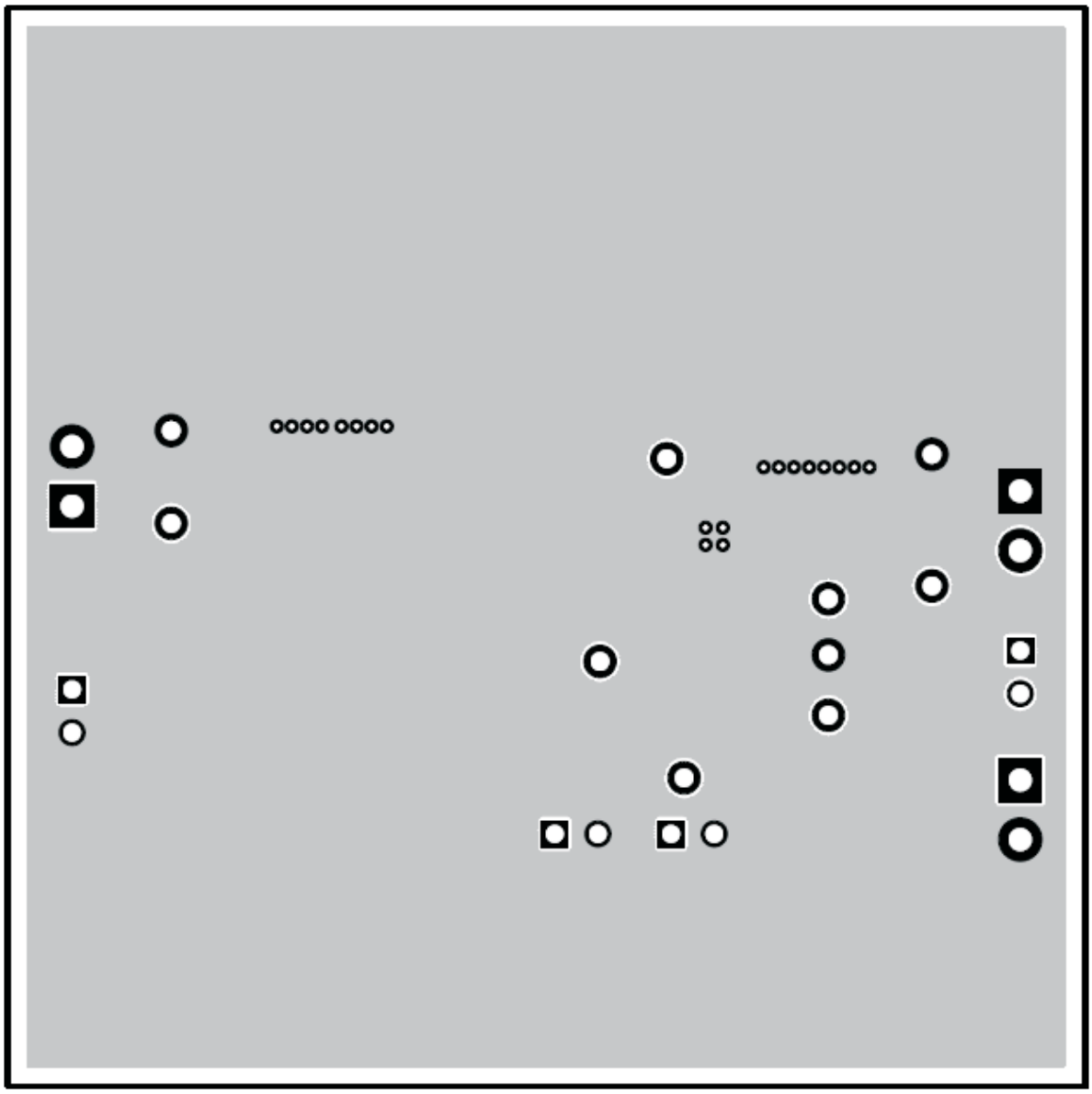

Figure 3-4. TPS54620EVM-374 Bottom-Side layout

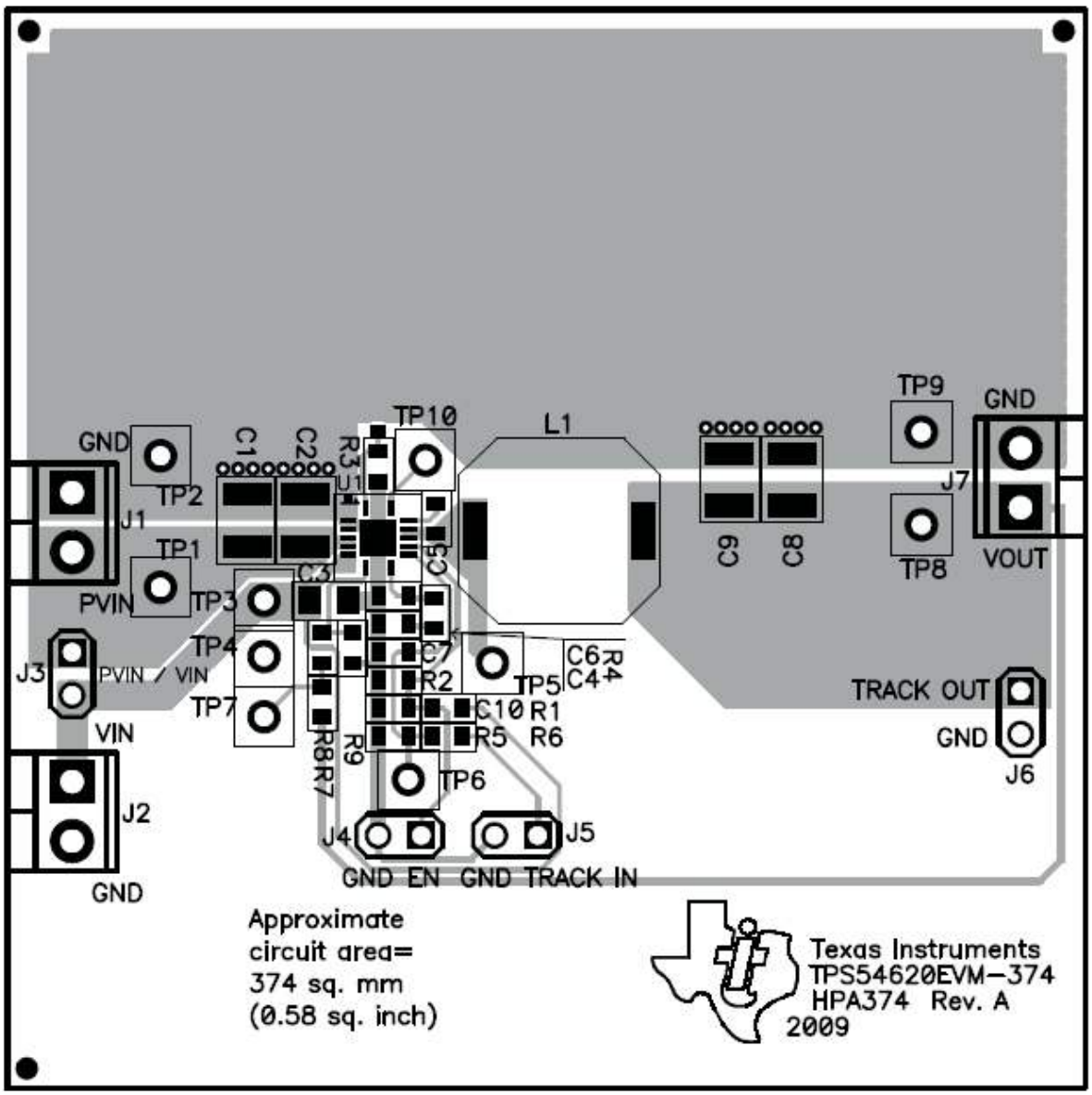

Figure 3-5. TPS54620EVM-374 Top-Side Assembly

3.2 Estimated Circuit Area

The estimated printed circuit board area for the components used in this design is 0.58 in^2 (374 mm^2). This area does not include test point or connectors.

4 Schematic and Bill of Materials

This section presents the TPS54620EVM-374 schematic and bill of materials.

4.1 Schematic

Figure 4-1 is the schematic for the TPS54620EVM-374.

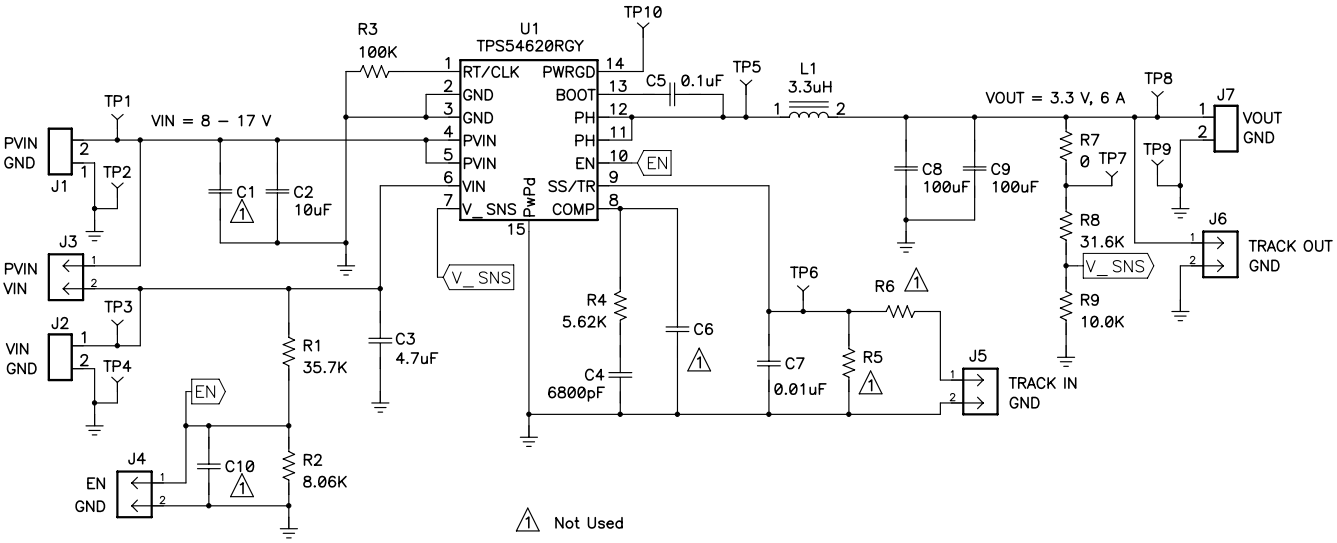

Figure 4-1. TPS54620EVM-374 Schematic

4.2 Bill of Materials

Table 4-1 presents the bill of materials for the TPS54620EVM-374 .

Table 4-1. TPS54620EVM-374 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
0	C1	Open	Capacitor, Ceramic, 25V, X5R, 20%	1210	Std	Std
1	C2	10µF	Capacitor, Ceramic, 25V, X5R, 20%	1210	Std	Std
1	C3	4.7µF	Capacitor, Ceramic, 25V, X5R, 10%	0805	Std	Std
1	C4	6800pF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
1	C5	0.1µF	Capacitor, Ceramic, 50V, X7R, 10%	0603	Std	Std
0	C6, C10	Open	Capacitor, Ceramic	0603	Std	Std
1	C7	0.01µF	Capacitor, Ceramic, 25V, X7R, 10%	0603	Std	Std
2	C8, C9	100µF	Capacitor, Ceramic, 6.3V, X5R, 20%	1210	Std	Std
3	J1, J2, J7	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
4	J3, J4, J5, J6	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	L1	3.3µH	Inductor, SMT, 7.2A, 10.4milliohm	0.402 sq inch	MSS1048-332NL_	Coilcraft
1	R1	35.7K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	8.06K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	100K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	5.62K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
0	R5, R6	Open	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R8	31.6K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R9	10.0K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
6	TP1, TP3, TP5, TP6, TP7, TP8	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone
4	TP2, TP4, TP9, TP10	5001	Test Point, Black, Thru Hole Color Keyed	0.100 x 0.100 inch	5001	Keystone
1	U1	TPS54620RGY	IC, 4.5V-17V Synchronous Step Down Converter with Integrated MOSFETs	3.5mm x 3.5mm QFN14	TPS54620RGY	TI
2	—		Shunt, 100-mil, Black	0.100	929950-00	3M
1	—		PCB, 2.5” x 2.5” x 0.062”		HPA374	Any

Notes

1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk (‘**’) cannot be substituted. All other components can be substituted with equivalent MFG's components.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2017) to Revision B (August 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2
- Updated the user's guide title..... 2

Changes from Revision * (May 2009) to Revision A (March 2017) **Page**

- Changed the Load transient response TYP values in Table 1-2 2
- Changed the Loop bandwidth TYP value From: 45 To 43 kHz in Table 1-2 2
- Changed the Phase margin TYP value From: 46 To 52° in Table 1-2 2
- Changed the Output ripple voltage TYP value From: 18 To 20 mVPP in Table 1-2 2
- Replaced Figure 2-5 8
- Replaced Figure 2-6 8
- Replaced Figure 2-7 9

- Replaced Figure 4-1 18
- Changed values of C8, C9, R4, C4, and the Description of U1 in Table 4-1 19

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