# CD54HC4538, CD74HC4538, CD54HCT4538, CD74HCT4538

## High-Speed CMOS Logic Dual Retriggerable Precision Monostable Multivibrator

Data sheet acquired from Harris Semiconductor
SCHS123E

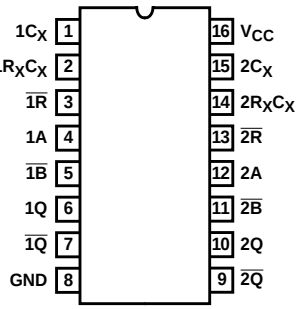
June 1998 - Revised October 2003

### Features

- **Retriggerable/Resettable Capability**
- **Trigger and Reset Propagation Delays Independent of $R_X$, $C_X$**
- **Triggering from the Leading or Trailing Edge**
- **Q and $\overline{Q}$ Buffered Outputs Available**
- **Separate Resets**
- **Wide Range of Output Pulse Widths**
- **Schmitt Trigger Input on A and $\overline{B}$ Inputs**
- **Retrigger Time is Independent of $C_X$**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, $V_{IL}$= 0.8V (Max), $V_{IH}$ = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\propto A$ at $V_{OL}$, $V_{OH}$**

### Pinout

**CD54HC4538, CD54HCT4538**
**(CERDIP)**
**CD74HC4538**
**(PDIP, SOIC, SOP, TSSOP)**
**CD74HCT4538**
**(PDIP, SOIC)**
TOP VIEW




### Description

The ’HC4538 and ’HCT4538 are dual retriggerable/resettable monostable precision multivibrators for fixed voltage timing applications. An external resistor ($R_X$) and an external capacitor ($C_X$) control the timing and the accuracy for the circuit. Adjustment of $R_X$ and $C_X$ provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The propagation delay from trigger input-to-output transition and the propagation delay from reset input-to-output transition are independent of $R_X$ and $C_X$.

Leading-edge triggering (A) and trailing edge triggering ($\overline{B}$) inputs are provided for triggering from either edge of the input pulse. An unused “A” input should be tied to GND and an unused $\overline{B}$ should be tied to $V_{CC}$. On power up the IC is reset. Unused resets and sections must be terminated. In normal operation the circuit retriggers on the application of each new trigger pulse. To operate in the non-triggerable mode $\overline{Q}$ is connected to $\overline{B}$ when leading edge triggering (A) is used or Q is connected to A when trailing edge triggering ($\overline{B}$) is used. The period ($\tau$) can be calculated from $\tau = (0.7) R_X, C_X$; $R_{MIN}$ is 5kΩ. $C_{MIN}$ is 0pF.

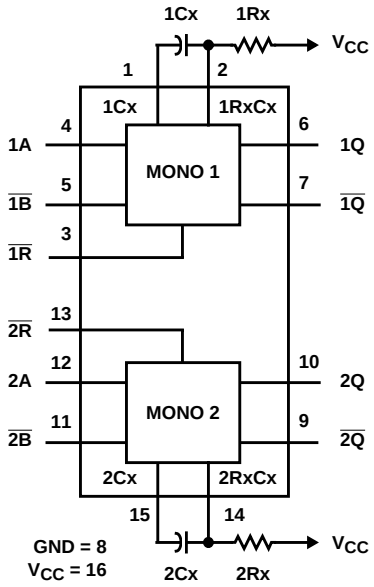
### Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE |
|---|---|---|
| CD54HC4538F3A | -55 to 125 | 16 Ld CERDIP |
| CD54HCT4538F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC4538E | -55 to 125 | 16 Ld PDIP |
| CD74HC4538M | -55 to 125 | 16 Ld SOIC |
| CD74HC4538MT | -55 to 125 | 16 Ld SOIC |
| CD74HC4538M96 | -55 to 125 | 16 Ld SOIC |
| CD74HC4538NSR | -55 to 125 | 16 Ld SOP |
| CD74HC4538PW | -55 to 125 | 16 Ld TSSOP |
| CD74HC4538PWR | -55 to 125 | 16 Ld TSSOP |
| CD74HC4538PWT | -55 to 125 | 16 Ld TSSOP |
| CD74HCT4538E | -55 to 125 | 16 Ld PDIP |
| CD74HCT4538M | -55 to 125 | 16 Ld SOIC |
| CD74HCT4538MT | -55 to 125 | 16 Ld SOIC |
| CD74HCT4538M96 | -55 to 125 | 16 Ld SOIC |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

## Functional Diagram




**TRUTH TABLE**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{R}$ | A | $\overline{B}$ | Q | $\overline{Q}$ |
| L | X | X | L | H |
| X | H | X | L | H |
| X | X | L | L | H |
| H | L | ↓ | ⎍ | ⎍ |
| H | ↑ | H | ⎍ | ⎍ |

H = High Level, L = Low Level, ↑ = Transition from Low to High, ↓ = Transition from High to Low, ⎍ One High Level Pulse, ⎍ One Low Level Pulse, X = Irrelevant.

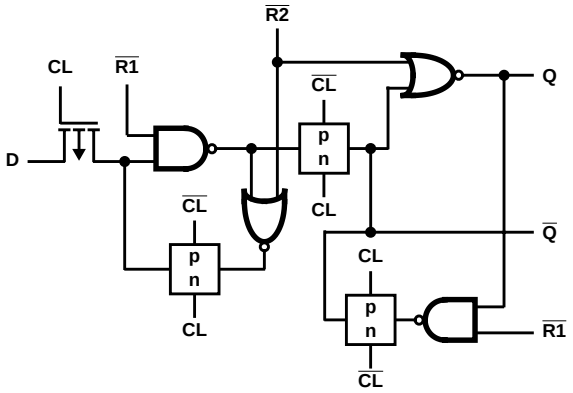



**FIGURE 1. FF DETAIL**

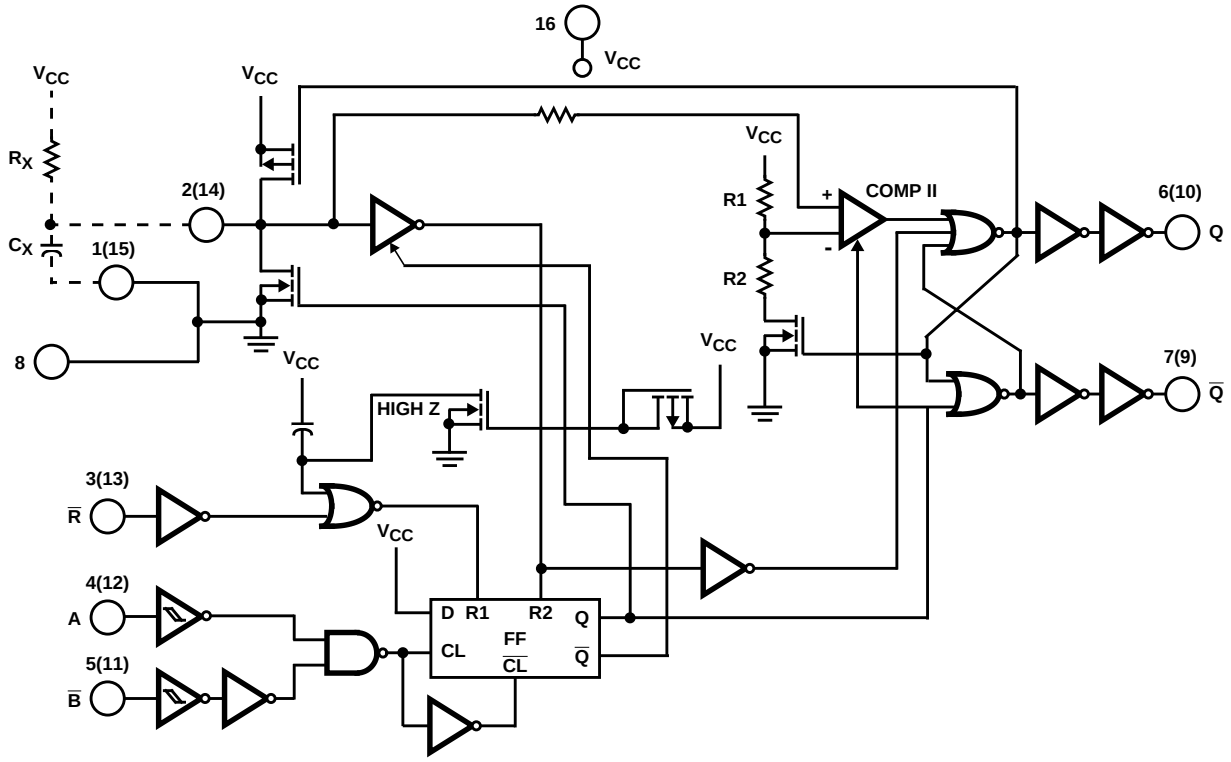



**FIGURE 2. LOGIC DIAGRAM (1 MONO)**

**FUNCTIONAL TERMINAL CONNECTIONS**

| FUNCTION | $V_{CC}$ TO TERMINAL NUMBER | | GND TO TERMINAL NUMBER | | INPUT PULSE TO TERMINAL NUMBER | | OTHER CONNECTIONS | |
|---|---|---|---|---|---|---|---|---|
| | $MONO_1$ | $MONO_2$ | $MONO_1$ | $MONO_2$ | $MONO_1$ | $MONO_2$ | $MONO_1$ | $MONO_2$ |
| Leading-Edge Trigger/Retriggerable | 3, 5 | 11, 13 | | | 4 | 12 | | |
| Leading-Edge Trigger/Non-Retriggerable | 3 | 13 | | | 4 | 12 | 5-7 | 11-9 |
| Trailing-Edge Trigger/Retriggerable | 3 | 13 | 4 | 12 | 5 | 11 | | |
| Trailing-Edge Trigger/Non-Retriggerable | 3 | 13 | | | 5 | 11 | 4-6 | 12-10 |

NOTES:

1. A retriggerable one-shot multivibrator has an output pulse width which is extended one full time period (T) after application of the last trigger pulse.
2. A non-triggerable one-shot multivibrator has a time period (T) referenced from the application of the first trigger pulse.

**FIGURE 3. INPUT PULSE TRAIN**

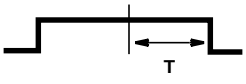



**FIGURE 4. RETRIGGERABLE MODE PULSE WIDTH (A MODE)**

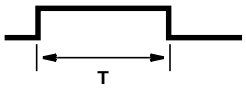



**FIGURE 5. NON-RETRIGGERABLE MODE PULSE WIDTH (A MODE)**

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . -0.5V to 7V
DC Input Diode Current, $I_{IK}$
For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, $I_O$
For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ . . . . . ±50mA

## Operating Conditions

Temperature Range, $T_A$ . . . . . $-55^oC$ to $125^oC$
Supply Voltage Range, $V_{CC}$ (Note 3)
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . 0V to $V_{CC}$
Input Rise and Fall Times, $t_r$, $t_f$
Reset Input:
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)
Trigger Inputs A or $\overline{B}$:
2V . . . . . Unlimited (Max)
4.5V. . . . . Unlimited (Max)
6V . . . . . Unlimited (Max)
External Timing Resistor, $R_X$ (Note 4) . . . . . 5kΩ (Min)
External Timing Capacitor, $C_X$ (Note 4) . . . . . 0 (Min)

## Thermal Information

Package Thermal Impedance, $\theta_{JA}$ (see Note 5):
E (PDIP) Package . . . . . $67^oC/W$
M (SOIC) Package. . . . . $73^oC/W$
NS (SOP) Package . . . . . $64^oC/W$
PW (TSSOP) Package . . . . . $108^oC/W$
Maximum Junction Temperature . . . . . $150^oC$
Maximum Storage Temperature Range . . . . . $-65^oC$ to $150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^oC$
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

3. Unless otherwise specified, all voltages are referenced to ground.
4. The maximum allowable values of $R_X$ and $C_X$ are a function of leakage of capacitor $C_X$, the leakage of the 'HC4538, and leakage due to board layout and surface resistance. Values of $R_X$ and $C_X$ should be chosen so that the maximum current into pin 2 or pin 14 is 30mA. Susceptibility to externally induced noise signals may occur for $R_X$ > 1MΩ.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | | | - | - | - | - | - | - | - | - | - | V |
| | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |

## DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | - | - | - | - | - | - | - | - | - | V |
| | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current A, $\overline{B}$, R | $I_I$ | $V_{CC}$ or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | ∝A |
| Input Leakage Current $R_XC_X$ (Note 6) | | | - | 6 | - | - | ±0.05 | - | ±0.5 | - | ±0.5 | ∝A |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | ∝A |
| Active Device Current Q = High & Pins 2, 14 at $V_{CC}/4$ | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | - | 0.6 | - | 0.8 | - | 1 | mA |
| **HCT TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ and GND | - | 5.5 | - | | ±0.1 | - | ±1 | - | ±1 | ∝A |
| Input Leakage Current $R_XC_X$ (Note 6) | | | - | 5.5 | - | - | ±0.05 | - | ±0.5 | - | ±0.5 | ∝A |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | ∝A |
| Active Device Current Q = High & Pins 2, 14 at $V_{CC}/4$ | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | - | 0.6 | - | 0.8 | - | 1 | mA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note 7) | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | ∝A |

NOTES:

6. When testing $I_{IL}$ the Q output must be high. If Q is low (device not triggered) the pull-up P device will be ON and the low resistance path from $V_{DD}$ to the test pin will cause a current far exceeding the specification.
7. For dual-supply systems theoretical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

### HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| All | 0.5 |

NOTE: Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Table, e.g. 360∞A max at 25$^{O}$C.

### Prerequisite for Switching Specifications

| PARAMETER | SYMBOL | $V_{CC}$ (V) | 25$^{O}$C | | | -40$^{O}$C TO 85$^{O}$C | | | -55$^{O}$C TO 125$^{O}$C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **HC TYPES** | | | | | | | | | | | | |
| Input Pulse Widths A, $\overline{B}$ | $t_{WH}$, $t_{WL}$ | 2 | 80 | - | - | 100 | - | - | 120 | - | - | ns |
| | | 4.5 | 16 | - | - | 20 | - | - | 24 | - | - | ns |
| | | 6 | 14 | - | - | 17 | - | - | 20 | - | - | ns |
| $\overline{R}$ | $t_{WL}$ | 2 | 80 | - | - | 100 | - | - | 120 | - | - | ns |
| | | 4.5 | 16 | - | - | 20 | - | - | 24 | - | - | ns |
| | | 6 | 14 | - | - | 17 | - | - | 20 | - | - | ns |
| Reset Recovery Time | $t_{REC}$ | 2 | 5 | - | - | 5 | - | - | 5 | - | - | ns |
| | | 4.5 | 5 | - | - | 5 | - | - | 5 | - | - | ns |
| | | 6 | 5 | - | - | 5 | - | - | 5 | - | - | ns |
| Retrigger Time (Figure 11) | $t_{rT}$ | 5 | - | 175 | - | - | - | - | - | - | - | ns |
| **HCT TYPES** | | | | | | | | | | | | |
| Input Pulse Widths A, $\overline{B}$ | $t_{WH}$, $t_{WL}$ | 4.5 | 16 | - | - | 20 | - | - | 24 | - | - | ns |
| $\overline{R}$ | $t_{WL}$ | 4.5 | 20 | - | - | 25 | - | - | 30 | - | - | ns |
| Reset Recovery Time | $t_{REC}$ | 4.5 | 5 | - | - | 5 | - | - | 5 | - | - | ns |
| Retrigger Time (Figure 11) | $t_{rT}$ | 5 | - | 175 | - | - | - | - | - | - | - | ns |

**Switching Specifications** $C_L$ = 50pF, Input $t_r$, $t_f$ = 6ns, $R_X$ = 10KΩ, $C_X$ = 0

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | |
| Propagation Delay A, $\overline{B}$ to Q | $t_{PLH}$ | $C_L$ = 50pF | 2 | - | - | 250 | - | 315 | - | 375 | ns |
| | | | 4.5 | - | - | 50 | - | 63 | - | 75 | ns |
| | | $C_L$ = 15pF | 5 | - | 21 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 43 | - | 54 | - | 64 | ns |
| A, $\overline{B}$ to $\overline{Q}$ | $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 250 | - | 315 | - | 375 | ns |
| | | | 4.5 | - | - | 50 | - | 63 | - | 75 | ns |
| | | $C_L$ = 15pF | 5 | - | 21 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 43 | - | 54 | - | 64 | ns |
| $\overline{R}$ to Q | $t_{PHL}$ | $C_L$ = 50pF | 2 | - | - | 250 | - | 315 | - | 375 | ns |
| | | | 4.5 | - | - | 50 | - | 63 | - | 75 | ns |
| | | $C_L$ = 15pF | 5 | - | 21 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 43 | - | 54 | - | 64 | ns |
| $\overline{R}$ to $\overline{Q}$ | $t_{PLH}$ | $C_L$ = 50pF | 2 | - | - | 250 | - | 315 | - | 375 | ns |
| | | | 4.5 | - | - | 50 | - | 63 | - | 75 | ns |
| | | $C_L$ = 15pF | 5 | - | 21 | - | - | - | - | - | ns |
| | | $C_L$ = 50pF | 6 | - | - | 43 | - | 54 | - | 64 | ns |
| Output Transition Time | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | - | - | 75 | - | 95 | - | 110 | ns |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns |
| Output Pulse Width $R_X$ = 10k, $C_X$ = 0.1∝F | τ | $C_L$ = 50pF | 3 | 0.64 | - | 0.78 | 0.612 | 0.812 | 0.605 | 0.819 | ms |
| | | | 5 | 0.63 | - | 0.77 | 0.602 | 0.798 | 0.595 | 0.805 | ms |
| Output Pulse Width Match, Same Package | - | - | | - | ±1 | - | - | - | - | - | % |
| Power Dissipation Capacitance (Notes 8, 9) | $C_{PD}$ | $C_L$ = 15pF | 5 | - | 136 | - | - | - | - | - | pF |
| Input Capacitance | $C_I$ | $C_L$ = 50pF | - | 10 | - | 10 | - | 10 | - | 10 | pF |
| **HCT TYPES** | | | | | | | | | | | |
| Propagation Delay A, $\overline{B}$ to Q | $t_{PLH}$ | $C_L$ = 50pF | 4.5 | - | - | 55 | - | 69 | - | 83 | ns |
| | | $C_L$ = 15pF | 5 | - | 23 | - | - | - | - | - | ns |
| A, $\overline{B}$ to $\overline{Q}$ | $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 55 | - | 69 | - | 83 | ns |
| | | $C_L$ = 15pF | 5 | - | 23 | - | - | - | - | - | ns |

**Switching Specifications** $C_L$ = 50pF, Input $t_r$, $t_f$ = 6ns, $R_X$ = 10KΩ, $C_X$ = 0 **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $\overline{R}$ to Q | $t_{PHL}$ | $C_L$ = 50pF | 4.5 | - | - | 40 | - | 50 | - | 60 | ns |
| | | $C_L$ = 15pF | 5 | - | 17 | - | - | - | - | - | ns |
| $\overline{R}$ to $\overline{Q}$ | $t_{PLH}$ | $C_L$ = 50pF | 4.5 | - | - | 50 | - | 63 | - | 75 | ns |
| | | $C_L$ = 15pF | 5 | - | 21 | - | - | - | - | - | ns |
| Output Transition Time | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | - | - | 15 | - | 19 | - | 22 | ns |
| Output Pulse Width $R_X$ = 10k, $C_X$ = 0.1∝F | τ | $C_L$ = 50pF | 5 | 0.63 | - | 0.77 | 0.602 | 0.798 | 0.595 | 0.805 | ms |
| Output Pulse Width Match, Same Package | - | - | - | - | ±1 | - | - | - | - | - | % |
| Power Dissipation Capacitance (Notes 8, 9) | $C_{PD}$ | $C_L$ = 15pF | 5 | - | 134 | - | - | - | - | - | pF |
| Input Capacitance | $C_I$ | $C_L$ = 50pF | - | 10 | - | 10 | - | 10 | - | 10 | pF |

NOTES:

8. $C_{PD}$ is used to determine the dynamic power consumption, per one shot.
9. $P_D = (C_{PD} + C_X) V_{CC}^2 f_i \Sigma(C_L V_{CC}^2 f_O)$ where $f_i$ = input frequency, $f_O$ = output frequency, $C_L$ = output load capacitance, $C_X$ = external capacitance $V_{CC}$ = supply voltage assuming $f_i \ll \frac{1}{\tau}$

## Test Circuits and Waveforms

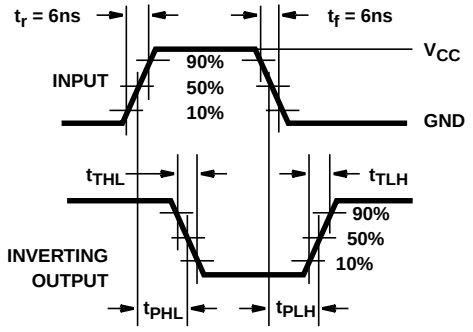



**FIGURE 6. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

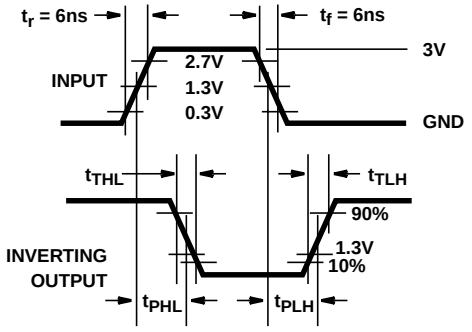



**FIGURE 7. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

## Typical Performance Curves

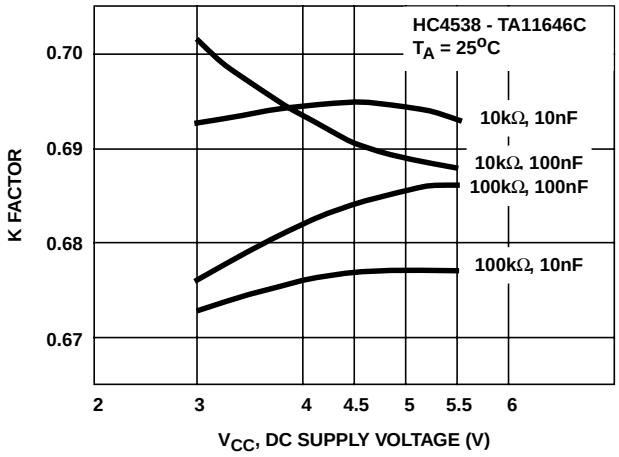



FIGURE 8. K FACTOR vs DC SUPPLY VOLTAGE ($V_{CC}$) - V

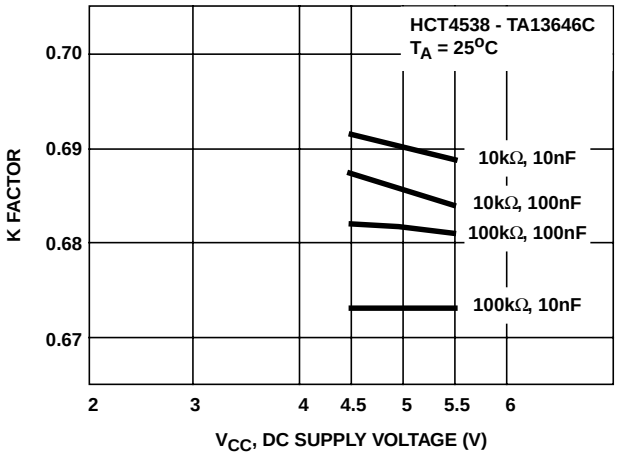



FIGURE 9. K FACTOR vs DC SUPPLY VOLTAGE ($V_{CC}$) - V

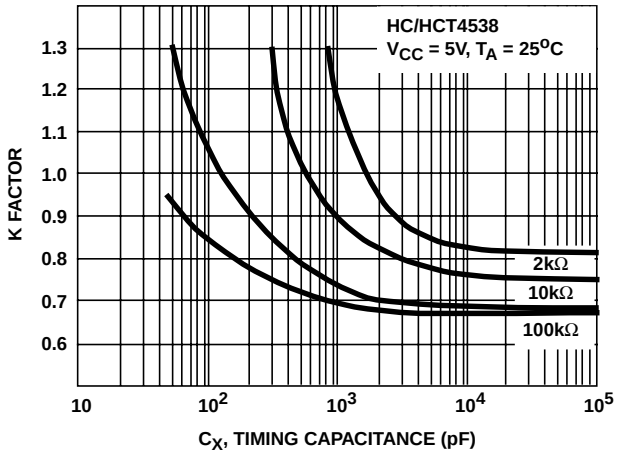



FIGURE 10. K FACTOR vs $C_X$

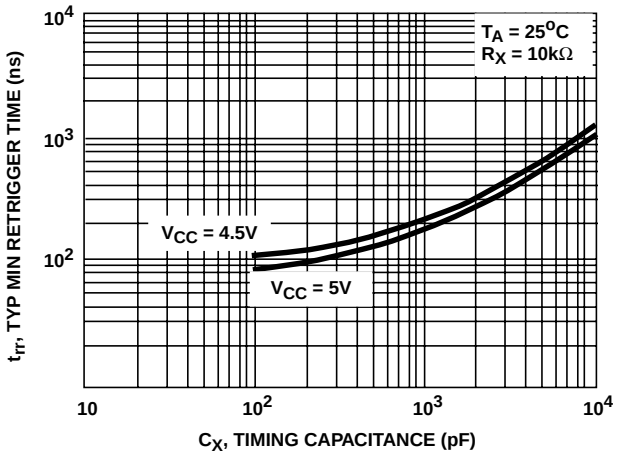



FIGURE 11. MINIMUM RETRIGGER TIME vs TIMING CAPACITANCE

## Power-Down Mode

During a rapid power-down condition, as would occur with a power-supply short circuit with a poorly filtered power supply, the energy stored in $C_X$ could discharge into Pin 2 or 14. To aviod possible device damage in this mode, when $C_X$ is ≥ 0.5∝F, a protection diode with a 1 ampere or higher rating (1N5395 or equivalent) and a separate ground return for $C_X$ should be provided as shown in Figure 12.

An alternate protection method is shown in Figure 13, where a 51Ω current-limiting resistor is inserted in series with $C_X$. Note that a small pulse width decrease will occur however, and $R_X$ must be appropriately increased to obtain the originally desired pulse width.

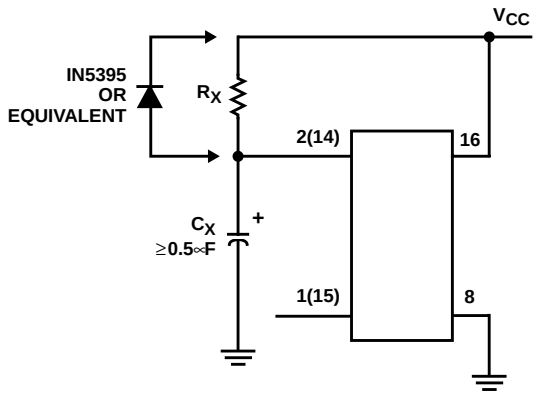



FIGURE 12. RAPID POWER-DOWN PROTECTION CIRCUIT

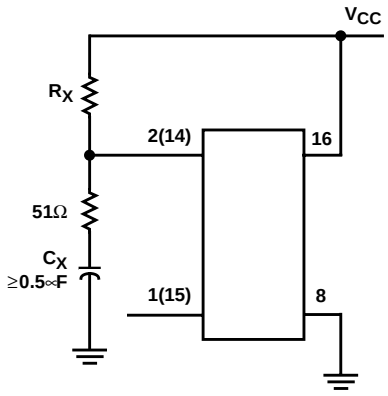



FIGURE 13. ALTERNATE RAPID POWER-DOWN PROTECTION CIRCUIT

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-8688601EA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8688601EA CD54HC4538F3A | Samples |
| CD54HC4538F | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54HC4538F | Samples |
| CD54HC4538F3A | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8688601EA CD54HC4538F3A | Samples |
| CD54HCT4538F3A | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54HCT4538F3A | Samples |
| CD74HC4538E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC4538E | Samples |
| CD74HC4538EE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC4538E | Samples |
| CD74HC4538M | LIFEBUY | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4538M | |
| CD74HC4538M96 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4538M | Samples |
| CD74HC4538M96E4 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4538M | Samples |
| CD74HC4538M96G4 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4538M | Samples |
| CD74HC4538ME4 | LIFEBUY | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4538M | |
| CD74HC4538MG4 | LIFEBUY | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4538M | |
| CD74HC4538MT | LIFEBUY | SOIC | D | 16 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4538M | |
| CD74HC4538NSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4538M | Samples |
| CD74HC4538PW | LIFEBUY | TSSOP | PW | 16 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ4538 | |
| CD74HC4538PWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ4538 | Samples |
| CD74HC4538PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ4538 | Samples |
| CD74HC4538PWT | LIFEBUY | TSSOP | PW | 16 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ4538 | |
| CD74HCT4538E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT4538E | Samples |
| CD74HCT4538M | LIFEBUY | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT4538M | |
| CD74HCT4538M96 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT4538M | Samples |
| CD74HCT4538MT | LIFEBUY | SOIC | D | 16 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT4538M | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF CD54HC4538, CD54HCT4538, CD74HC4538, CD74HCT4538 :**

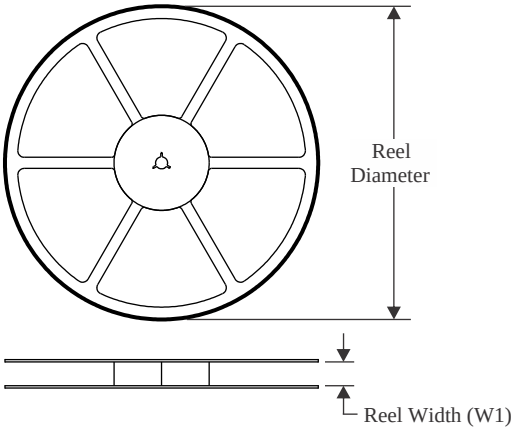
- Catalog : CD74HC4538, CD74HCT4538
- Automotive : CD74HC4538-Q1, CD74HC4538-Q1
- Military : CD54HC4538, CD54HCT4538

NOTE: Qualified Version Definitions:

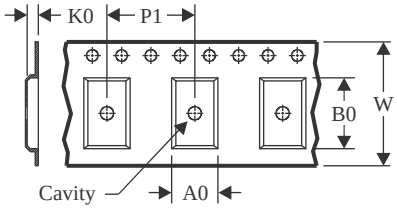
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

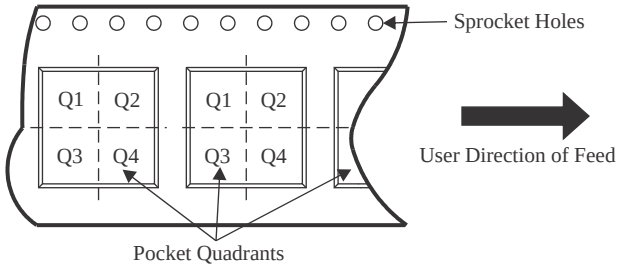



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

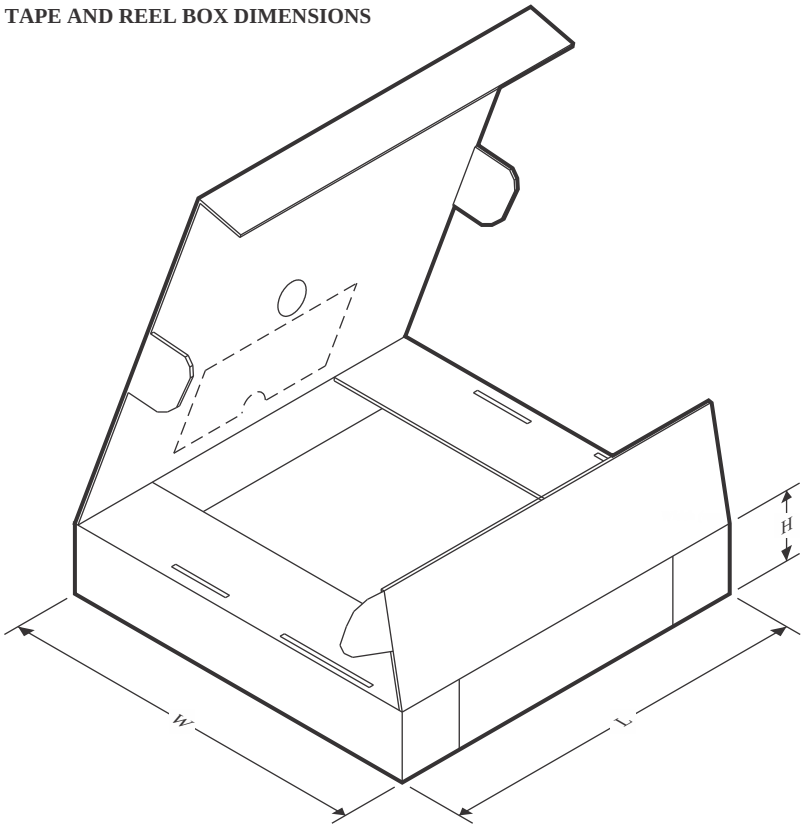
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HC4538M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC4538NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD74HC4538PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HC4538PWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HCT4538M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

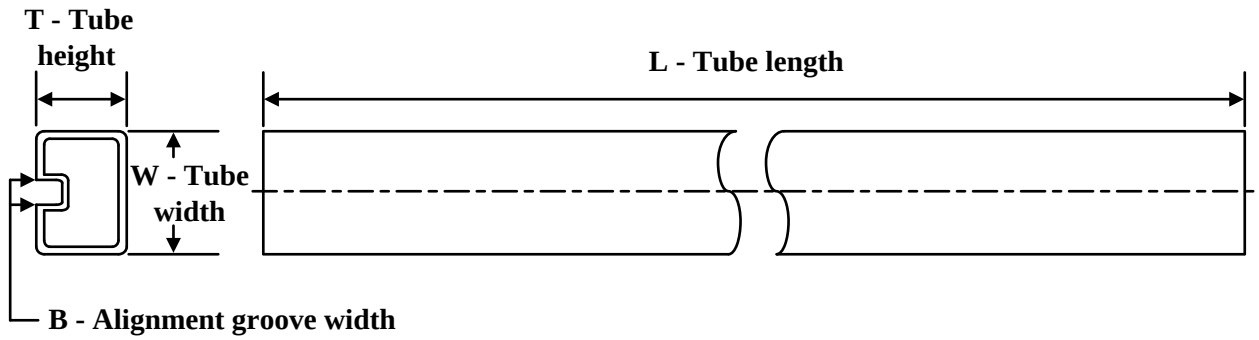
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HC4538M96 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| CD74HC4538NSR | SO | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| CD74HC4538PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| CD74HC4538PWT | TSSOP | PW | 16 | 250 | 356.0 | 356.0 | 35.0 |
| CD74HCT4538M96 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |

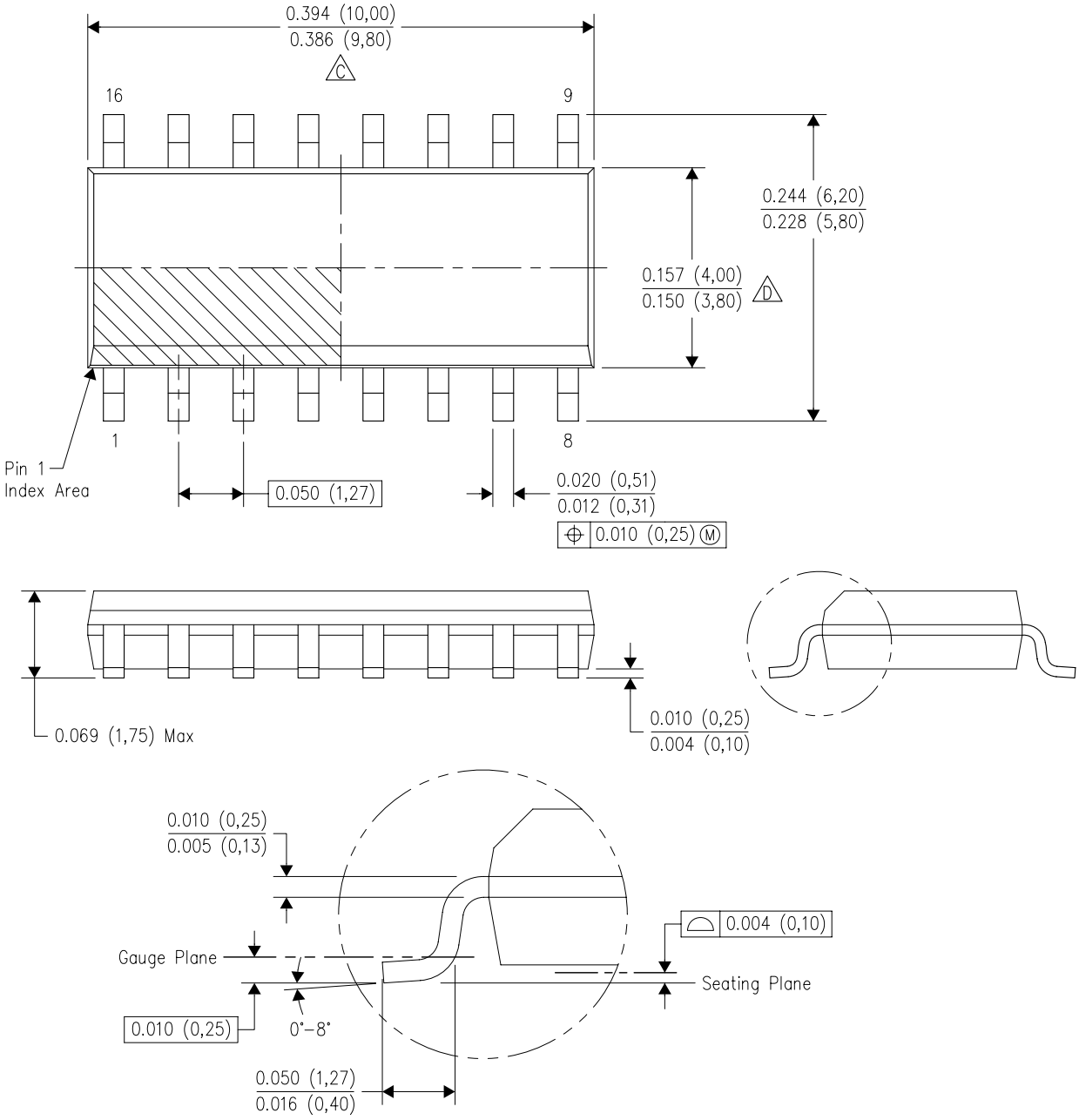
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD74HC4538E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC4538E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC4538EE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC4538EE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HC4538M | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| CD74HC4538ME4 | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| CD74HC4538MG4 | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| CD74HC4538PW | PW | TSSOP | 16 | 90 | 530 | 10.2 | 3600 | 3.5 |
| CD74HCT4538E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT4538E | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74HCT4538M | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |

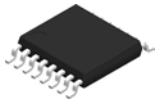
D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

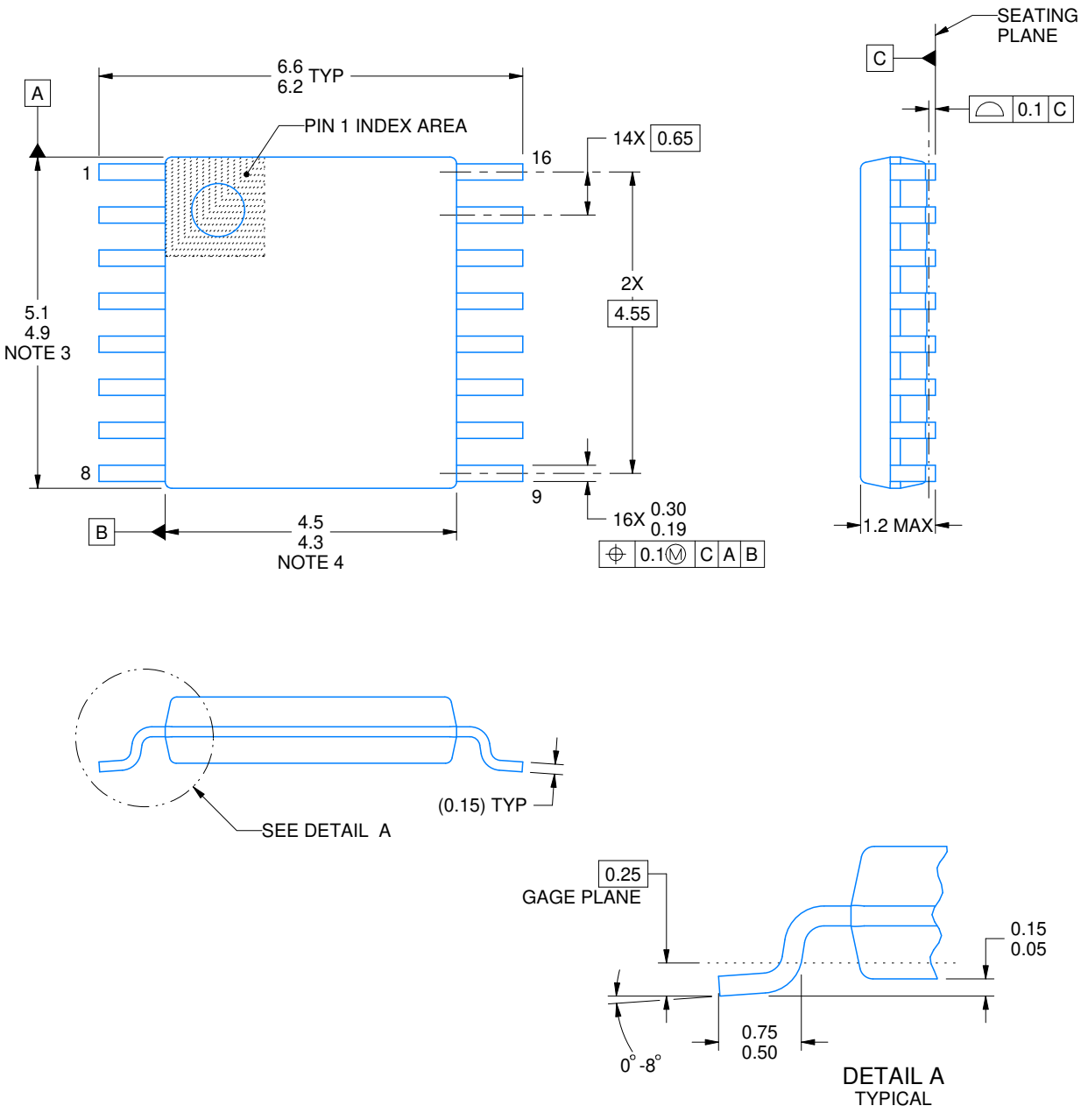
# PACKAGE OUTLINE

## PW0016A



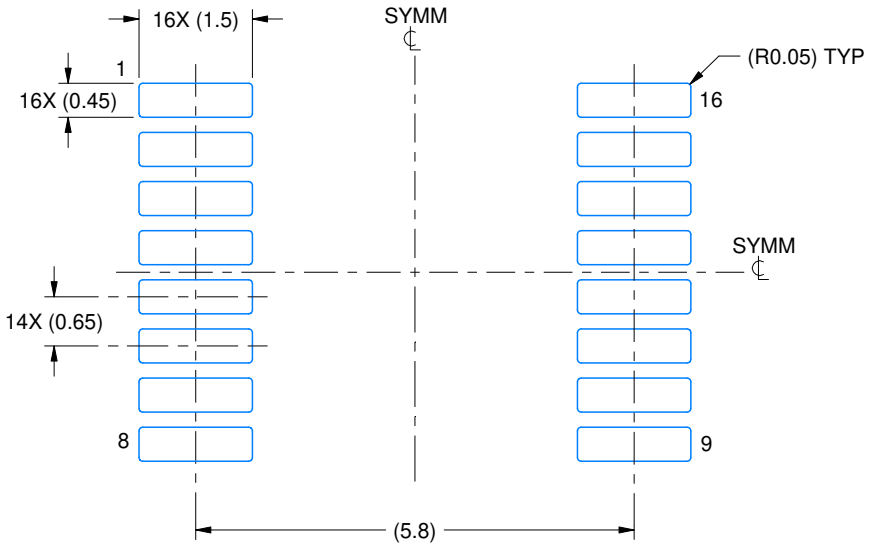
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

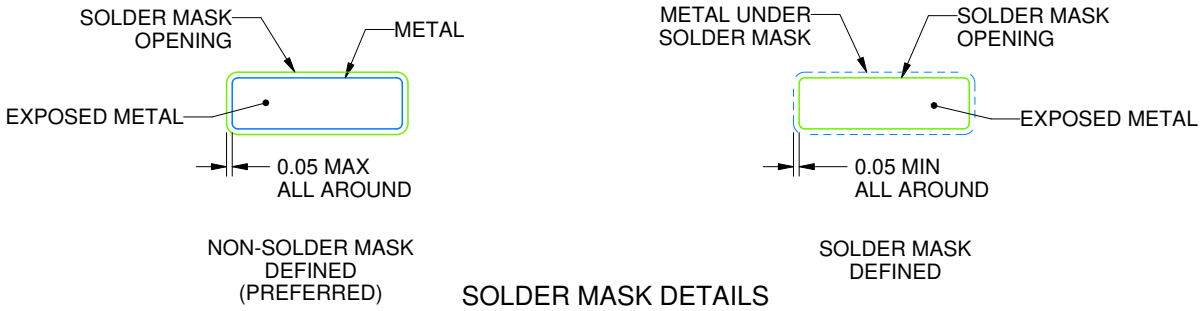



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

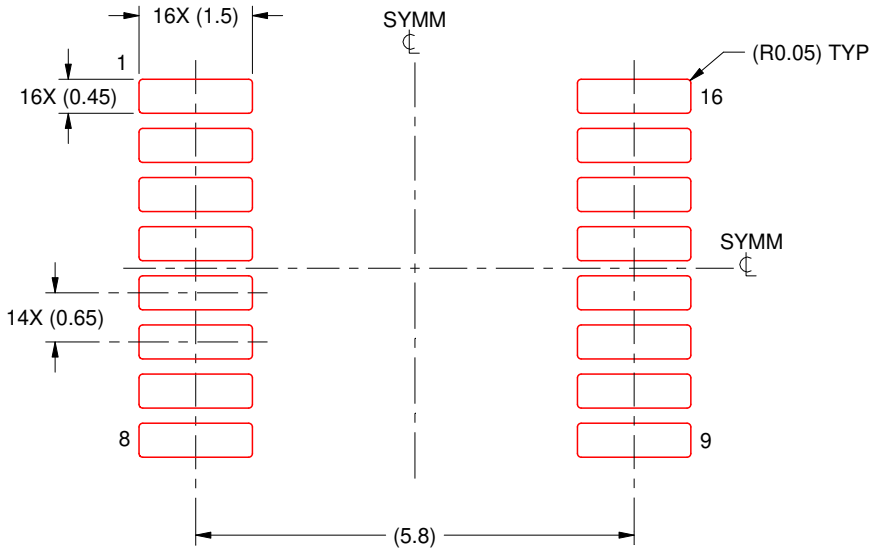



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

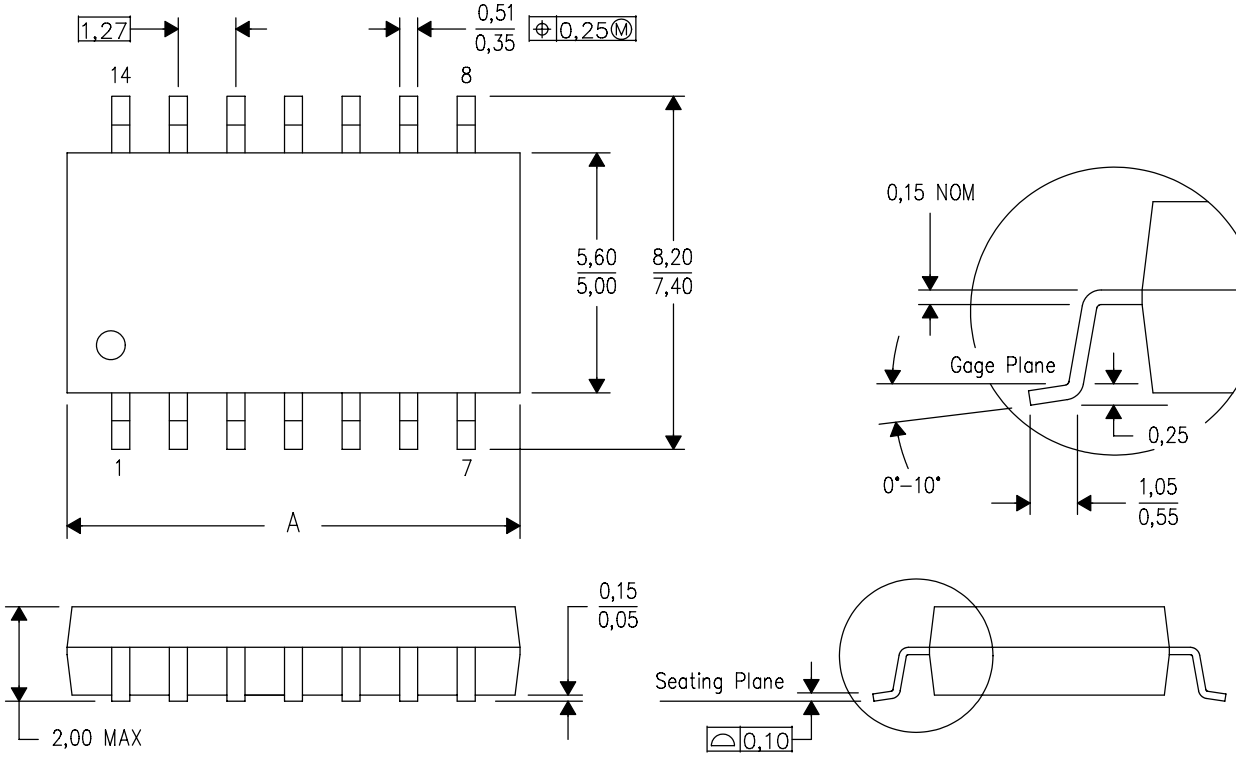
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

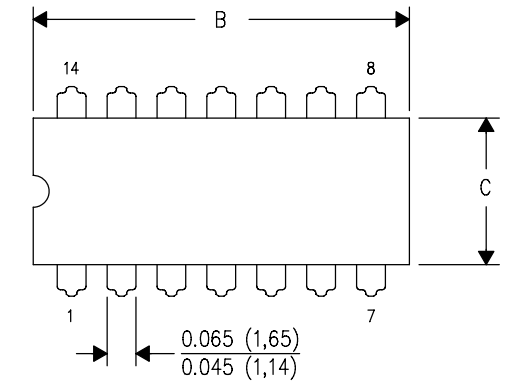
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

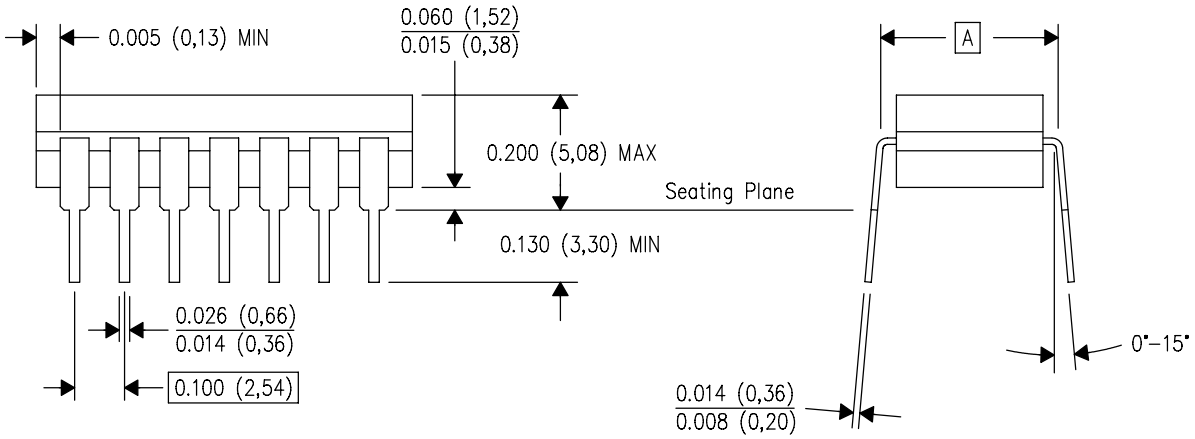
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



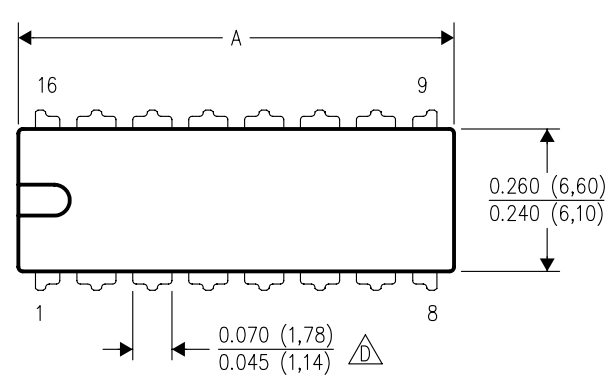

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

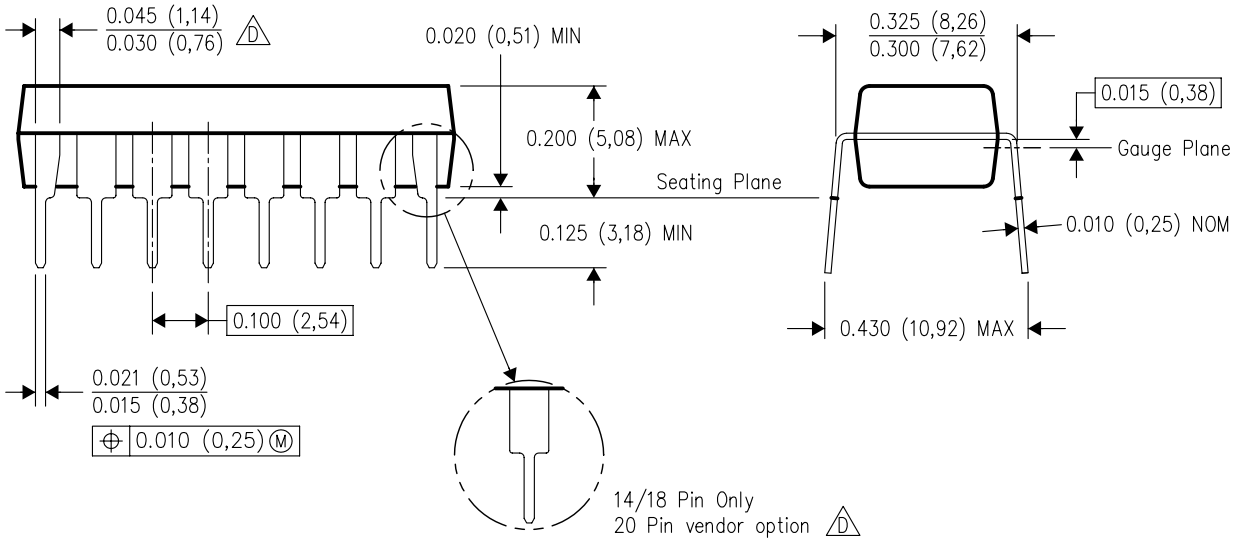
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

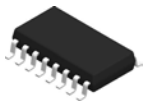



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

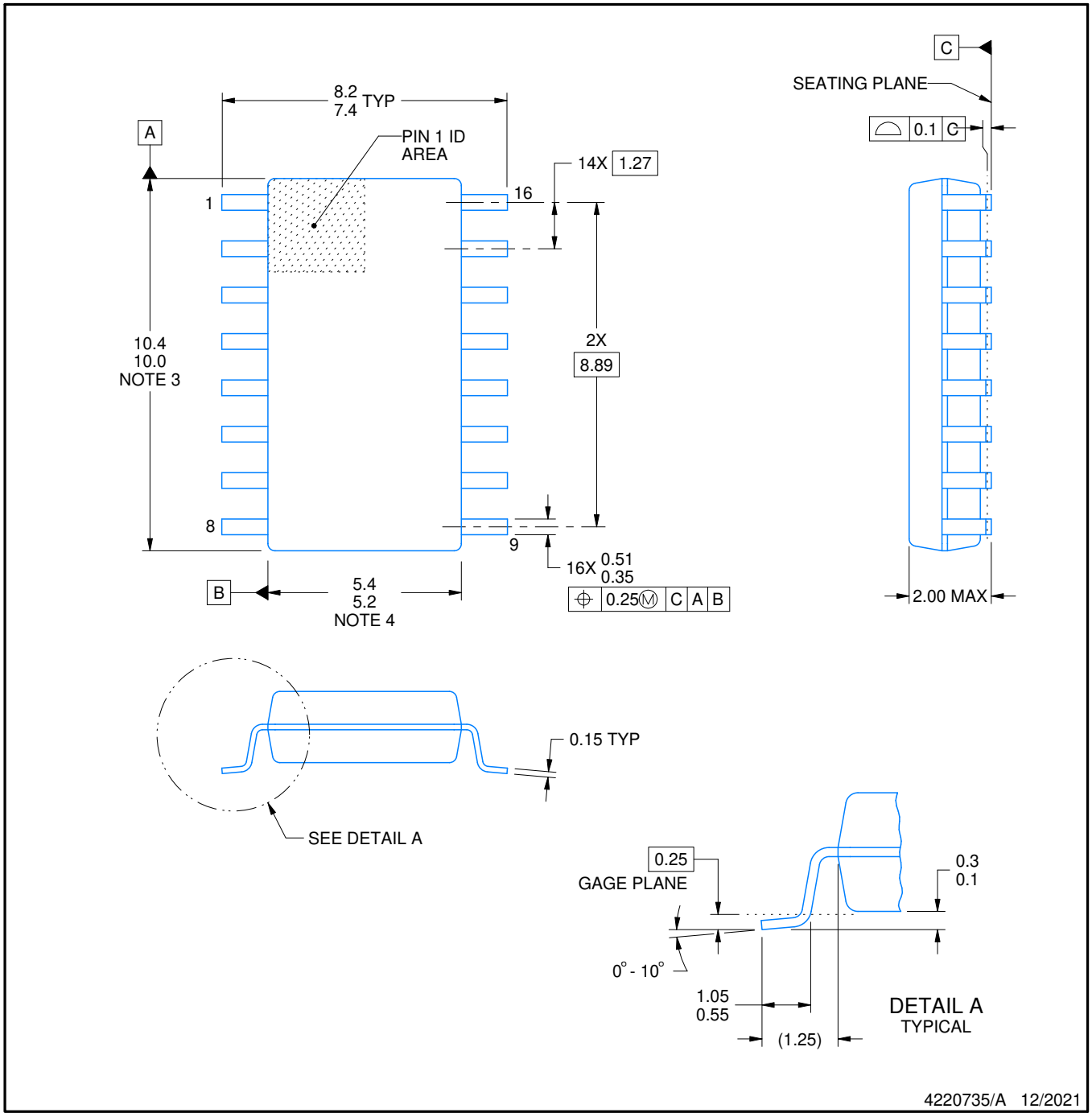


# PACKAGE OUTLINE

## NS0016A

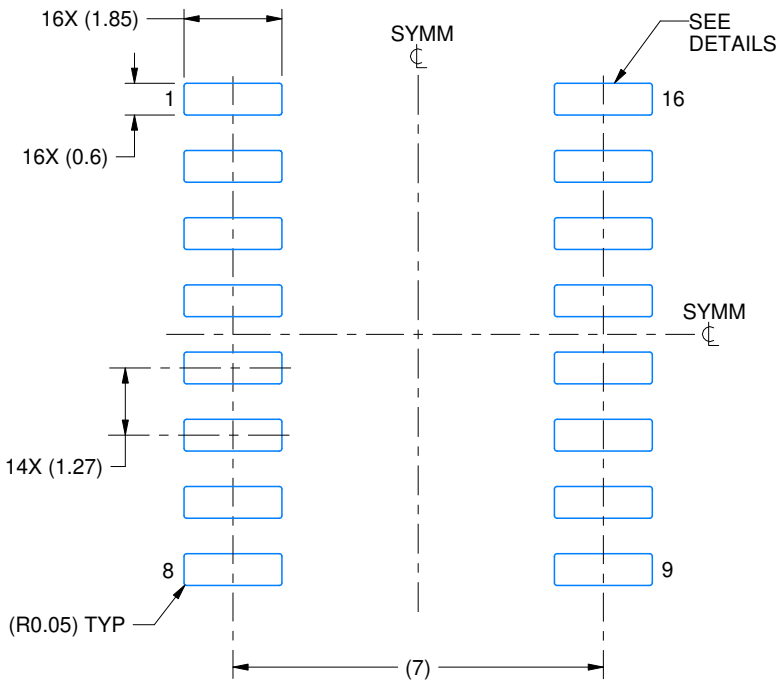
## SOP - 2.00 mm max height

SOP

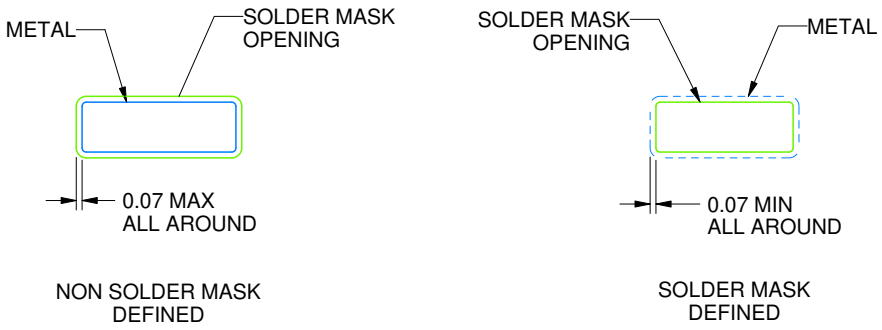



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
SCALE:7X




SOLDER MASK DETAILS

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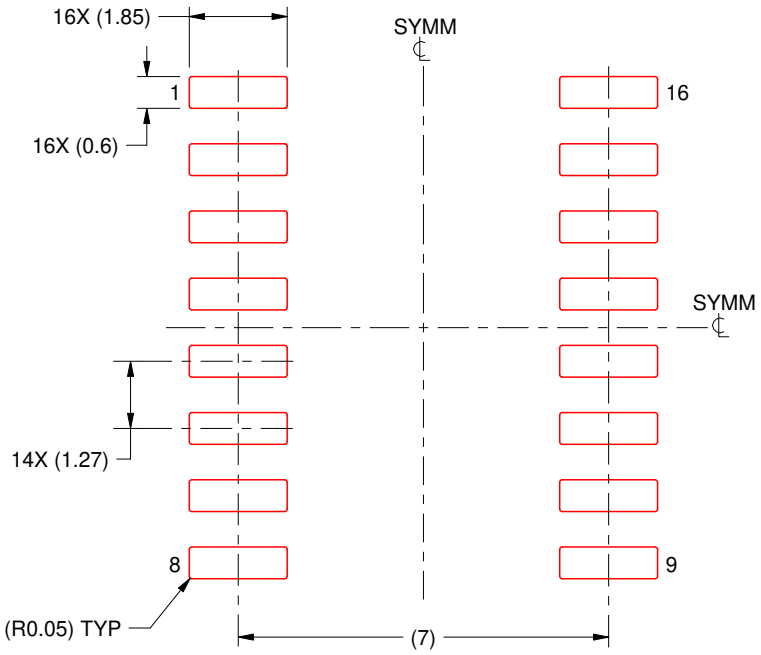
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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