User's Guide
SLAU695A–November 2016–Revised February 2019

ISO77xxD/ISO70xxD Single- and Dual-Digital Isolator Evaluation Module

This user's guide describes the ISO77xxD/ISO70xxD single- and dual-digital isolator evaluation module (EVM). This EVM lets designers evaluate device performance for fast development and analysis of isolated systems. The EVM supports evaluation of any of the TI single- or dual-channel digital isolators in an 8-pin SOIC (D) package.

CAUTION

This evaluation module is made available for isolator parameter performance evaluation only and is not intended for isolation voltage testing. To prevent damage to the EVM, any voltage applied as a supply or digital input/output must be maintained within the 0 V to 5.5 V recommended operating range.

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Trademarks

1 Introduction

This user's guide describes EVM operation with respect to the ISO77xxD/ISO70xxD single- and dual-channel digital isolators. However, the EVM may be reconfigured for evaluation of any of TI's single- or dual-channel digital isolators in an 8-pin SOIC (D) package. This guide also describes the available channel configurations within the ISO77xxD/ISO70xxD family, the EVM schematic, and typical laboratory setup. A typical input and output waveform is also presented.

2 Overview

The ISO77xxD/ISO70xxD is TI's new digital isolator family capable of galvanic isolations up to 4242 V_{PK}. The devices are certified to meet reinforced isolation requirements by VDE and CSA. These isolators provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. The ISO77xxD/ISO70xxD digital isolators have logic input and output buffers separated by a silicon oxide (SiO_2) insulation barrier. Used with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with, or damaging sensitive circuitry.

3 Pin Configurations of the ISO77xxD/ISO70xxD Single- and Dual-Channel Digital Isolators

Figure 1 shows the ISO7710/ISO701x single-channel digital isolator pin configuration.

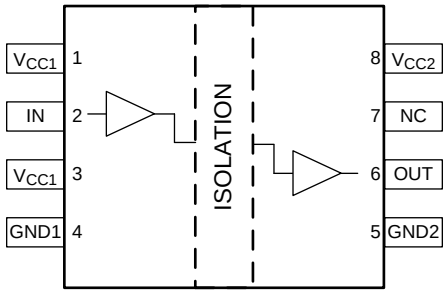

Figure 1. ISO7710/ISO701x Single-Channel Digital Isolator Pin Configuration

Figure 2 shows the ISO772x dual-channel digital isolator pin configurations.

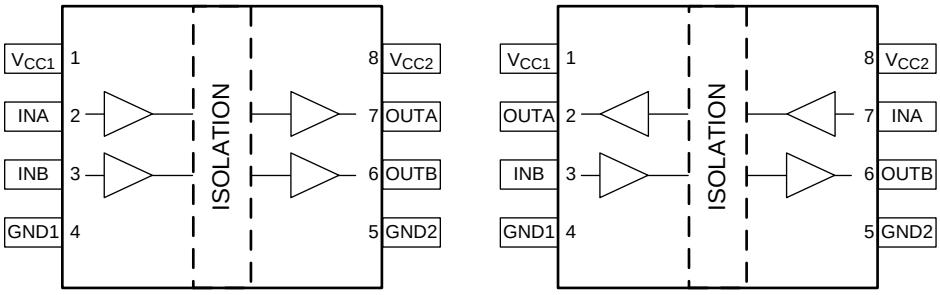

Figure 2. ISO772x/ISO702x Dual-Channel Digital Isolator Pin Configurations

4 ISO7721DEVM Board Block Diagram and Image

Figure 3 shows the board configuration for evaluation of the ISO7721/ISO7021 dual-channel digital isolator.

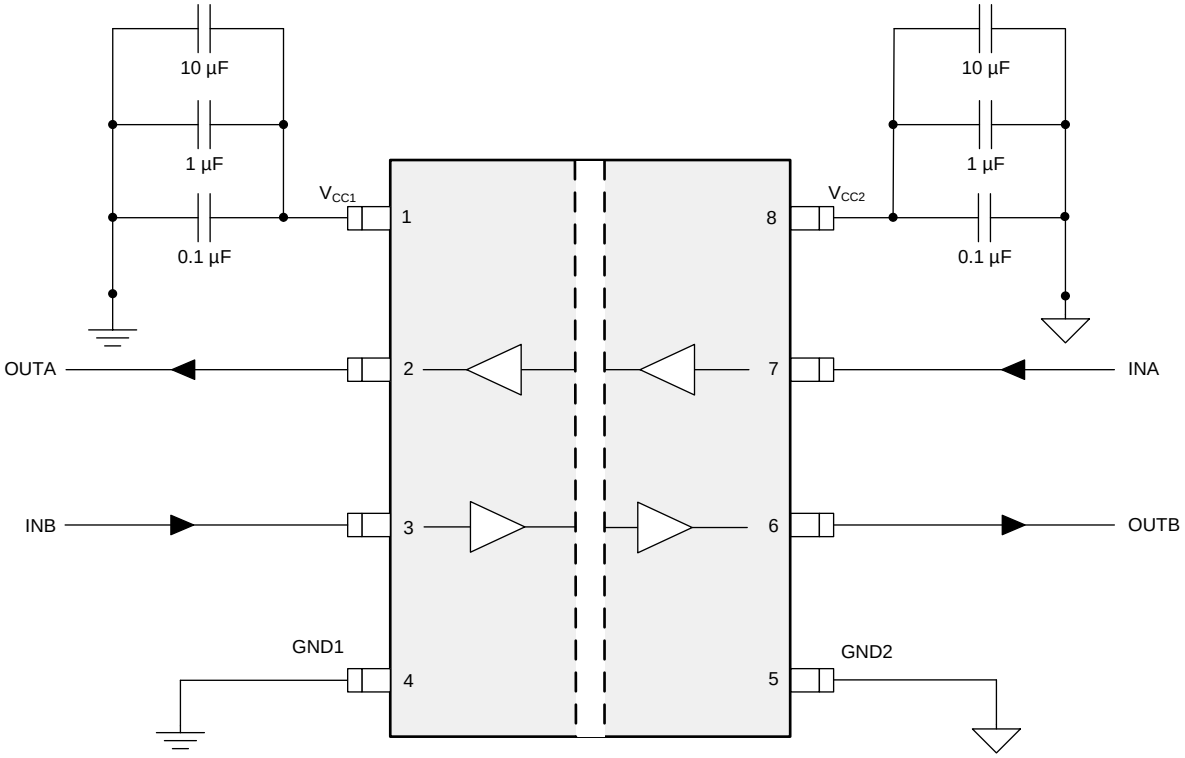

Figure 3. ISO7721/ISO7021 EVM Configuration

Figure 4 shows the photograph of the EVM.

Figure 4. ISO77xxD/ISO70xxD-EVM Photograph

5 EVM Setup and Operation

This section describes the setup and operation of the EVM for parameter performance evaluation. Figure 5 shows the configuration for operating the ISO77xxD/ISO70xxD single- and dual-digital isolator EVM using two power supplies.

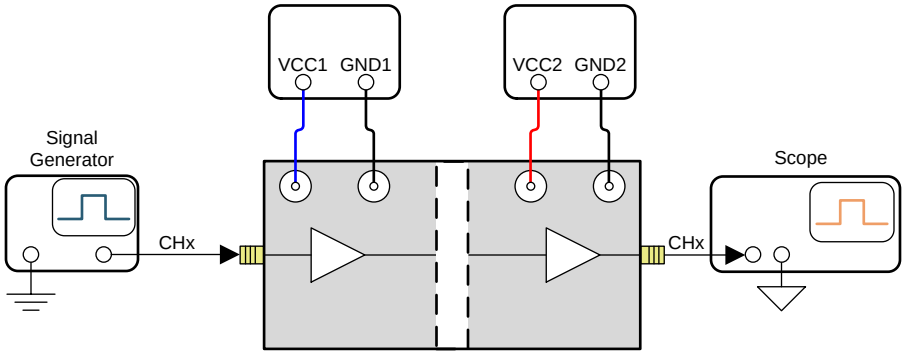

Figure 5. Basic EVM Operation

Figure 6 shows typical input and output waveforms of the EVM for a 1-MHz clock. The input is shown as channel 1, and the output is shown as channel 2.

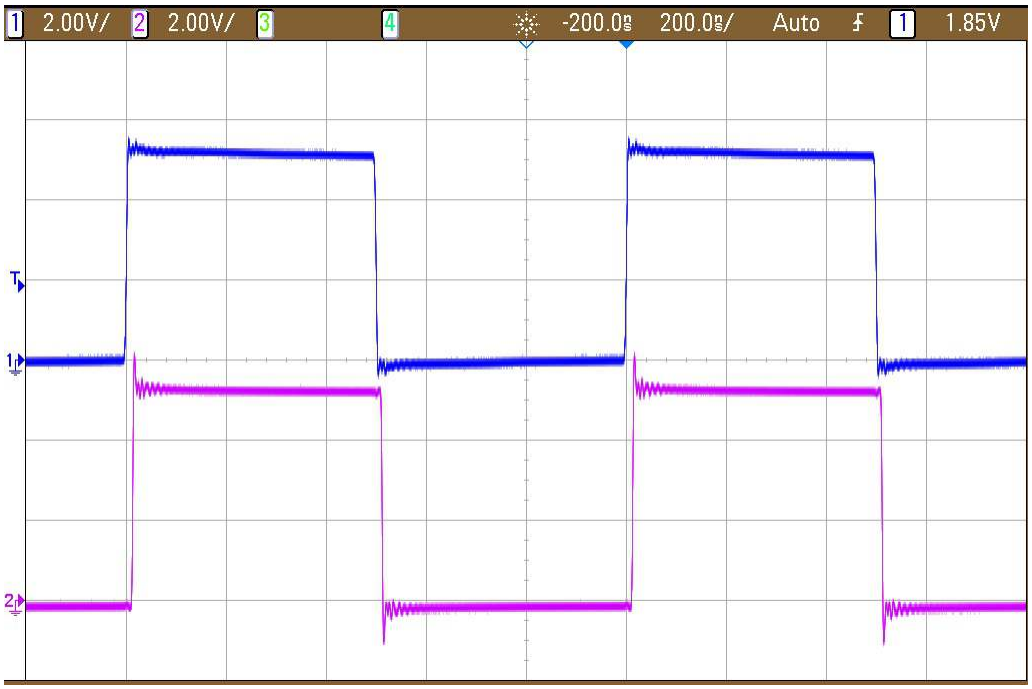

Figure 6. Typical Input and Output Waveform

6 Bill of Materials

Table 1 shows the bill of materials (BOM) for this EVM.

Table 1. Bill of Materials

Item	Designator	Description	Manufacturer	Part Number	Quantity
1	C1, C4	CAP, CERM, 10 µF, 35 V, ± 10%, X5R, 0805	MuRata	GRM21BR6YA106KE43L	2
2	C2, C5	CAP, CERM, 1 µF, 50 V, ± 10%, X5R, 0603	MuRata	GRM188R61H105KAALD	2
3	C3, C6	CAP, CERM, 0.1 µF, 25 V, ± 5%, X7R, 0603	AVX	06033C104JAT2A	2
4	H1, H2, H3, H4	Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)	4
5	J1, J2	Header, 100mil, 4x2, Gold, SMT	Molex	15910080	2
6	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	Test Point, Miniature, SMT	Keystone	5019	8
7	U1	Robust EMC, Low Power, Dual-Channel Digital Isolators, D0008B (SOIC-8)	Texas Instruments	ISO7721DR	1

7 EVM Schematics and Layout

The ISO7721DEVM is designed to accommodate any of the ISO77xxD/ISO70xxD single- and dual-channel devices in an 8-pin D package. To evaluate any of the ISO77xxD/ISO70xxD single- and dual-channel devices in an 8-pin D package, replace ISO7721D with the device of interest on the ISO7721DEVM PCB. No other component requires any modification. Figure 7 shows the ISO77xxD/ISO70xxD EVM schematic and Figure 8 shows the printed-circuit board (PCB) layout.

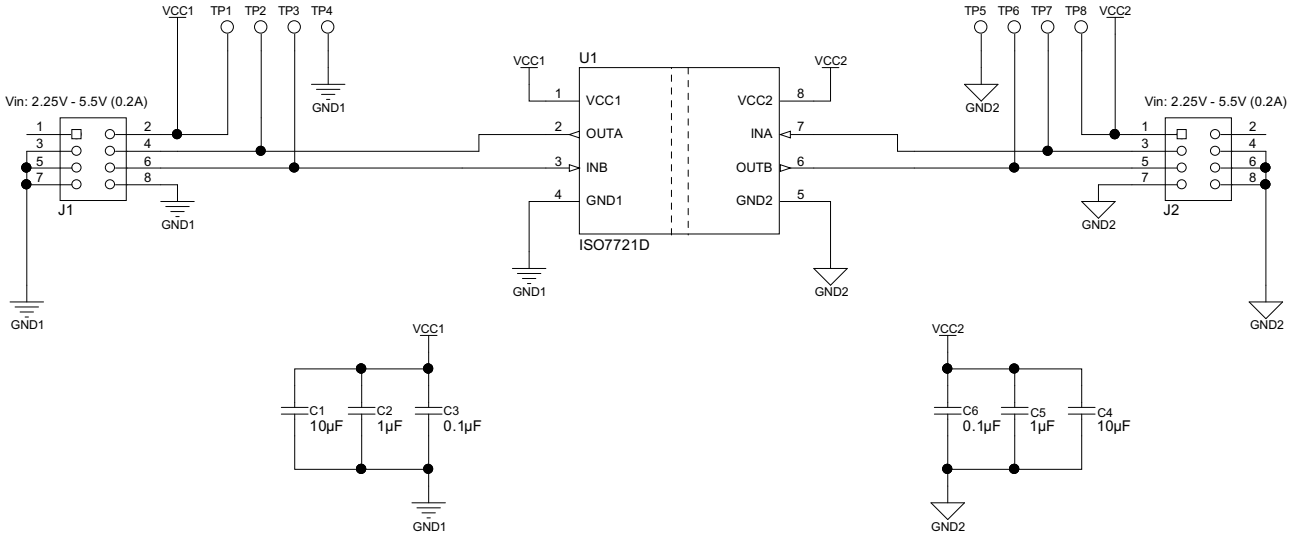

Figure 7. ISO77xxD/ISO70xxD EVM Schematic

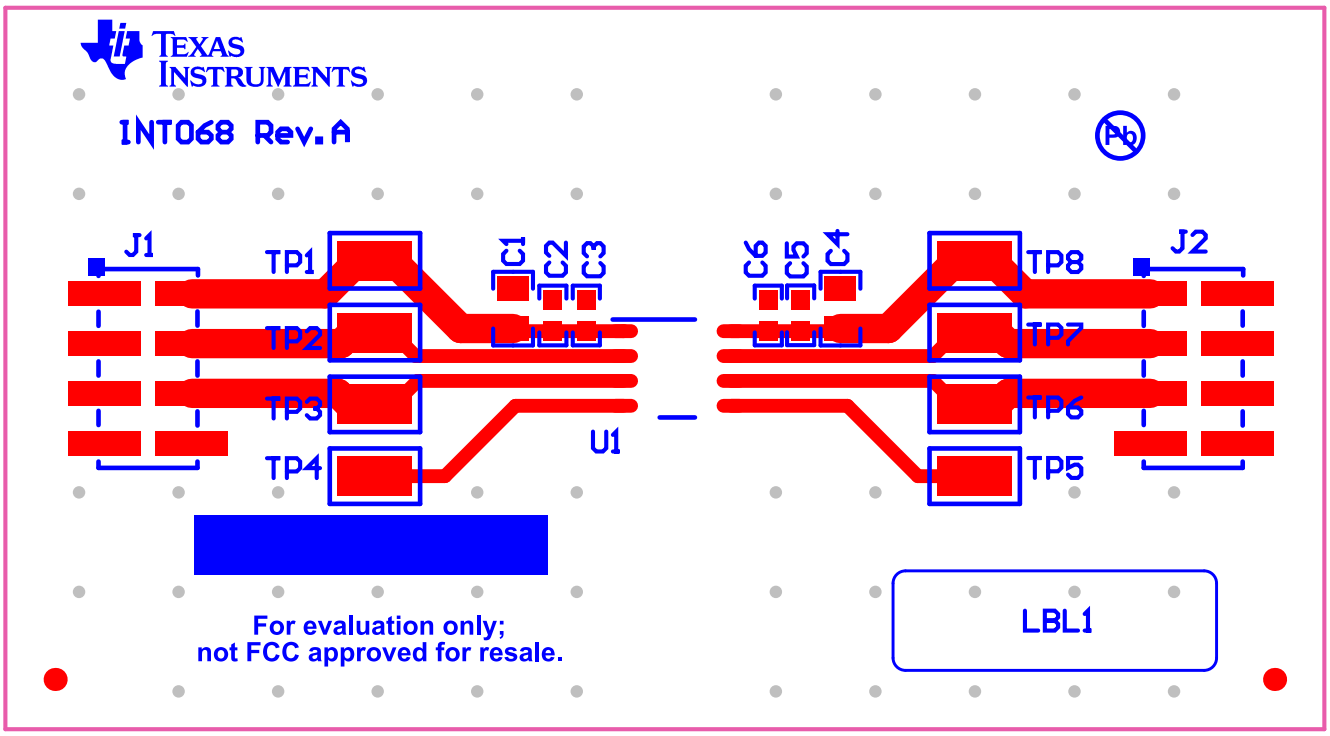

Figure 8. ISO77xxD/ISO70xxD PCB Layout

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