PCK953

20 MHz to 125 MHz PECL input, 9 CMOS output, 3.3 V PLL clock driver

Rev. 05 — 9 October 2008 Product data sheet

1. General description

The PCK953 is a 3.3 V compatible, PLL-based clock driver device targeted for high performance clock tree designs. With output frequencies of up to 125 MHz, and output skews of 100 ps, the PCK953 is ideal for the most demanding clock tree designs. The devices employ a fully differential PLL design to minimize cycle-to-cycle and phase jitter.

The PCK953 has a differential LVPECL reference input, along with an external feedback input. These features make the PCK953 ideal for use as a zero delay, low skew fan-out buffer. The device performance has been tuned and optimized for zero delay performance. The MR/$\overline{OE}$ input pin will reset the internal counters and 3-state the output buffers when driven HIGH.

The PCK953 is fully 3.3 V compatible and requires no external loop filter components. All control inputs accept LVCMOS or LVTTL compatible levels, while the outputs provide LVCMOS levels with the ability to drive terminated 50 Ω transmission lines. For series terminated 50 Ω lines, each of the PCK953 outputs can drive two traces, giving the device an effective fan-out of 1 : 18. The device is packaged in a 7 mm × 7 mm 32-lead LQFP package to provide the optimum combination of board density and performance.

2. Features

- Fully integrated PLL
- Output frequency up to 125 MHz in PLL mode
- Outputs disable in high-impedance
- LQFP32 packaging
- 55 ps cycle-to-cycle jitter typical
- 9 mA quiescent current typical
- 60 ps static phase offset typical

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCK953BD	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
PCK953BD/G			

Also refer to Table 8 “Packing information”.

4. Functional diagram

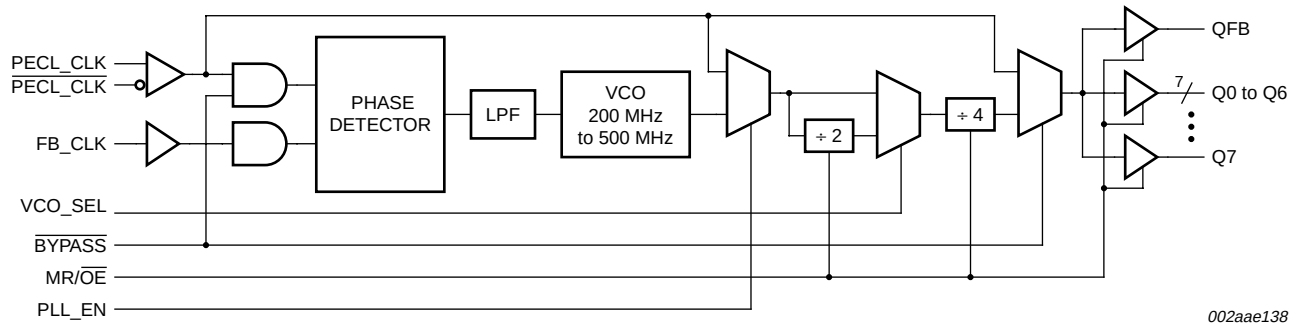


Fig 1. Functional diagram

5. Pinning information

5.1 Pinning

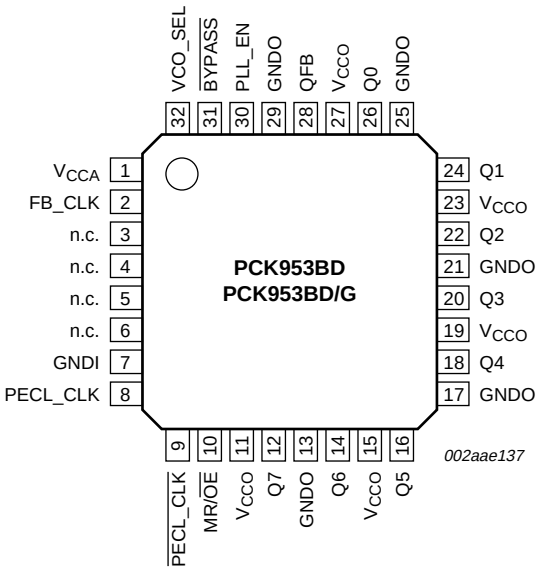


Fig 2. Pin configuration for LQFP32

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{CCA}	1	Analog supply voltage. See Section 11 “Application information” for design and layout considerations.
FB_CLK	2	Feedback clock input (CMOS) to comparator/phase detector.
n.c.	3, 4, 5, 6	Not connected.
GNDI	7	Ground pin associated with input circuitry.
PECL_CLK	8	LVPECL reference clock input, true.
$\overline{\text{PECL\_CLK}}$	9	LVPECL reference clock input, complementary.
MR/$\overline{\text{OE}}$	10	Master reset/output enable input. See Table 3 “Function selection”.
V_{CCO}	11, 15, 19, 23, 27	Supply voltage pins associated with output driver circuitry.
Q7	12	Buffered clock outputs (CMOS).
Q6	14	
Q5	16	
Q4	18	
Q3	20	
Q2	22	
Q1	24	
Q0	26	
GNDO	13, 17, 21, 25, 29	Ground pins associated with output driver circuitry.
QFB	28	Buffered clock output intended to be fed to feedback pin FB_CLK.
PLL_EN	30	PLL enable input pin. See Table 3 “Function selection”.
$\overline{\text{BYPASS}}$	31	Bypass input pin. See Table 3 “Function selection”.
VCO_SEL	32	VCO select input pin. See Table 3 “Function selection”.

6. Functional description

Refer to Figure 1 “Functional diagram”.

6.1 Function selection

Table 3. Function selection

Pin	Value	Function
$\overline{\text{BYPASS}}$	1	PLL enabled
	0	PLL bypass
MR/$\overline{\text{OE}}$	1	outputs disabled
	0	outputs enabled
VCO_SEL	1	divide-by-2
	0	divide-by-1
PLL_EN	1	select VCO
	0	select PECL_CLK

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.3	+4.6	V
V_I	input voltage		–0.3	V_{DD} + 0.3	V
I_I	input current		-	±20	mA
T_{stg}	storage temperature		–40	+125	°C

8. Static characteristics

Table 5. Static characteristics

T_{amb} = 0 °C to 70 °C; V_{CC} = 3.3 V ± 5 %, unless specified otherwise.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	LVCMOS inputs		2.0	-	3.6	V
V_{IL}	LOW-level input voltage	LVCMOS inputs		-	-	0.8	V
$V_{i(p-p)}$	peak-to-peak input voltage	PECL_CLK		300	-	1000	mV
V_{cm}	common-mode voltage	PECL_CLK	[1]	V_{CC} – 1.5	-	V_{CC} – 0.6	mV
V_{OH}	HIGH-level output voltage	I_{OH} = –20 mA	[2]	2.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 20 mA	[2]	-	-	0.5	V
I_I	input current			-	-	±75	µA
C_i	input capacitance			-	-	4	pF
C_{PD}	power dissipation capacitance	per output		-	25	-	pF
I_{CC}	maximum quiescent supply current	all V_{CC} pins		-	9	20	mA
I_{CCPLL}	maximum PLL supply current	V_{CCA} pin only		-	9	20	mA

[1] V_{cm} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the HIGH input is within the V_{cm} range and the input swing lies within the $V_{i(p-p)}$ specification.

[2] The PCK953 outputs can drive series or parallel terminated 50 Ω (or 50 Ω to 0.5V_{CC}) transmission lines on the incident edge (see Section 11 “Application information”).

9. Dynamic characteristics

Table 6. Dynamic characteristics

T_{amb} = 0 °C to 70 °C; V_{CC} = 3.3 V ± 5 %; unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{r(o)}$	output rise time	0.8 V to 2.0 V	0.30	0.55	0.8	ns
$t_{f(o)}$	output fall time	0.8 V to 2.0 V	0.30	0.55	0.8	ns
δ_o	output duty cycle		45	50	55	%
$t_{sk(o)}$	output skew time	output-to-output; relative to QFB	-	-	100	ps
f_{VCO}	PLL VCO lock range		120	-	500	MHz
$f_{o(max)}$	maximum output frequency	PLL mode; VCO_SEL = 1	20	-	100	MHz
		PLL mode; VCO_SEL = 0	35	-	125	MHz
		Bypass mode	-	-	225	MHz
t_{pd}(lock)	input to EXT_FB delay (with PLL locked)	f_{ref} = 50 MHz	−75	-	+125	ps
t_{pd}(bypass)	input to Qn delay	PLL bypassed	3	5.2	7	ns
t_{PLZ-HZ}	output disable time		-	-	7	ns
t_{PZL}	output enable time		-	-	6	ns
$t_{jit(cc)}$	cycle-to-cycle jitter time	peak-to-peak	-	55	100	ps
t_{lock}	maximum PLL lock time		-	0.01	10	ms

10. PLL input reference characteristics

Table 7. PLL input reference characteristics

T_{amb} = 0 °C to 70 °C.

Maximum and minimum input reference is limited by the VCO lock range and the feedback divider.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ref}	reference input frequency		20	-	125	MHz
f_{refDC}	reference input duty cycle		25	-	75	%

11. Application information

11.1 Power supply filtering

The PCK953 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The PCK953 provides separate power supplies for the output buffers (V_{CCO}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to try to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the PCK953.

Figure 3 illustrates a typical power supply filter scheme. The PCK953 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the PCK953. The current sourced though the V_{CCA} pin is typically 15 mA (20 mA maximum), assuming that a minimum of 3.0 V must be maintained on the V_{CCA} pin, very little DC voltage drop can be tolerated when a 3.3 V V_{CC} supply is used. The resistor shown in Figure 3 must have a resistance of 10 Ω to 15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100 : 1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive, and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8 Ω to 10 Ω resistor to avoid potential V_{CC} drop problems, and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

Although the PCK953 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

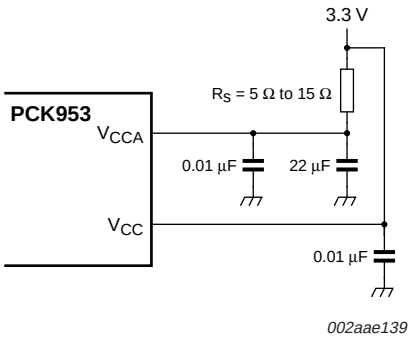


Fig 3. Power supply filter

11.2 Driving transmission lines

The PCK953 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω, the drivers can drive either parallel or series terminated transmission lines.

In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $0.5V_{CC}$. This technique draws a fairly high level of DC current, and thus only a single terminated line can be driven by each output of the PCK953 clock driver. For the series terminated case, however, there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fan-out of the PCK953 clock driver is effectively doubled due to its capability to drive multiple lines.

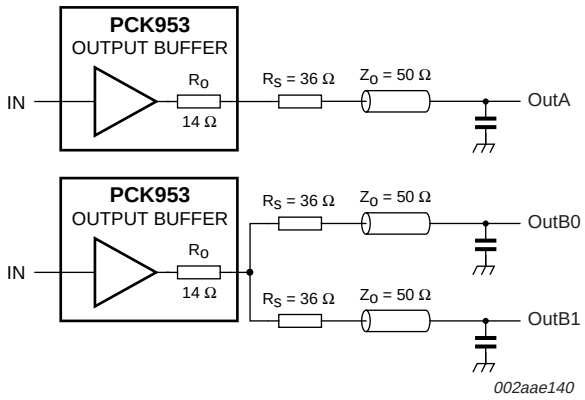


Fig 4. Single versus dual transmission lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the PCK953 output buffers is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations, a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the PCK953. The output waveform in Figure 5 shows a step in the waveform; this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S\left(\frac{Z_o}{R_s + R_o + Z_o}\right) \quad (1)$$

Z_o = 50 Ω || 50 Ω

R_s = 36 Ω || 36 Ω

R_o = 14 Ω

$$V_L = 3.0\left(\frac{25}{18 + 14 + 25}\right) = 3.0\left(\frac{25}{57}\right) = 1.31\ V \quad (2)$$

At the load end, the voltage will double due to the near unity reflection coefficient, to 2.62 V. It will then increment towards the quiescent 3.0 V in steps separated by one round-trip delay (in this case, 4.0 ns).

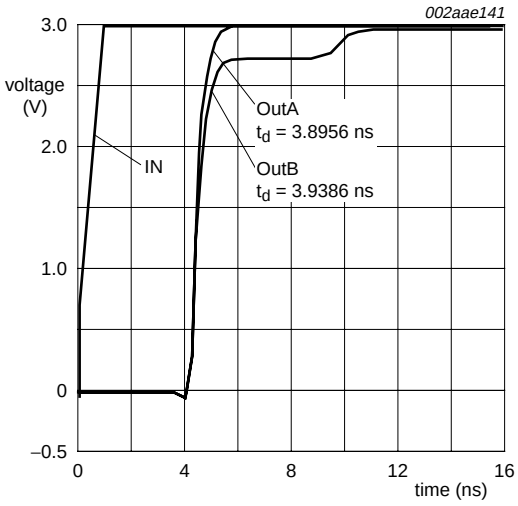
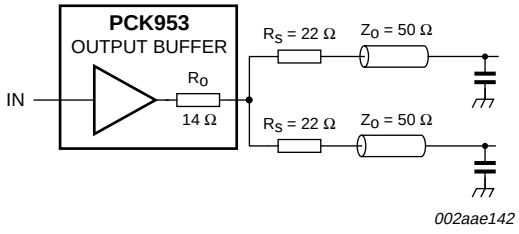


Fig 5. Single versus dual waveforms

Since this step is well above the threshold region, it will not cause any false clock triggering, however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 6 should be used. In this case, the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance, the line impedance is perfectly matched.



14 Ω + 22 Ω || 22 Ω = 50 Ω || 50 Ω

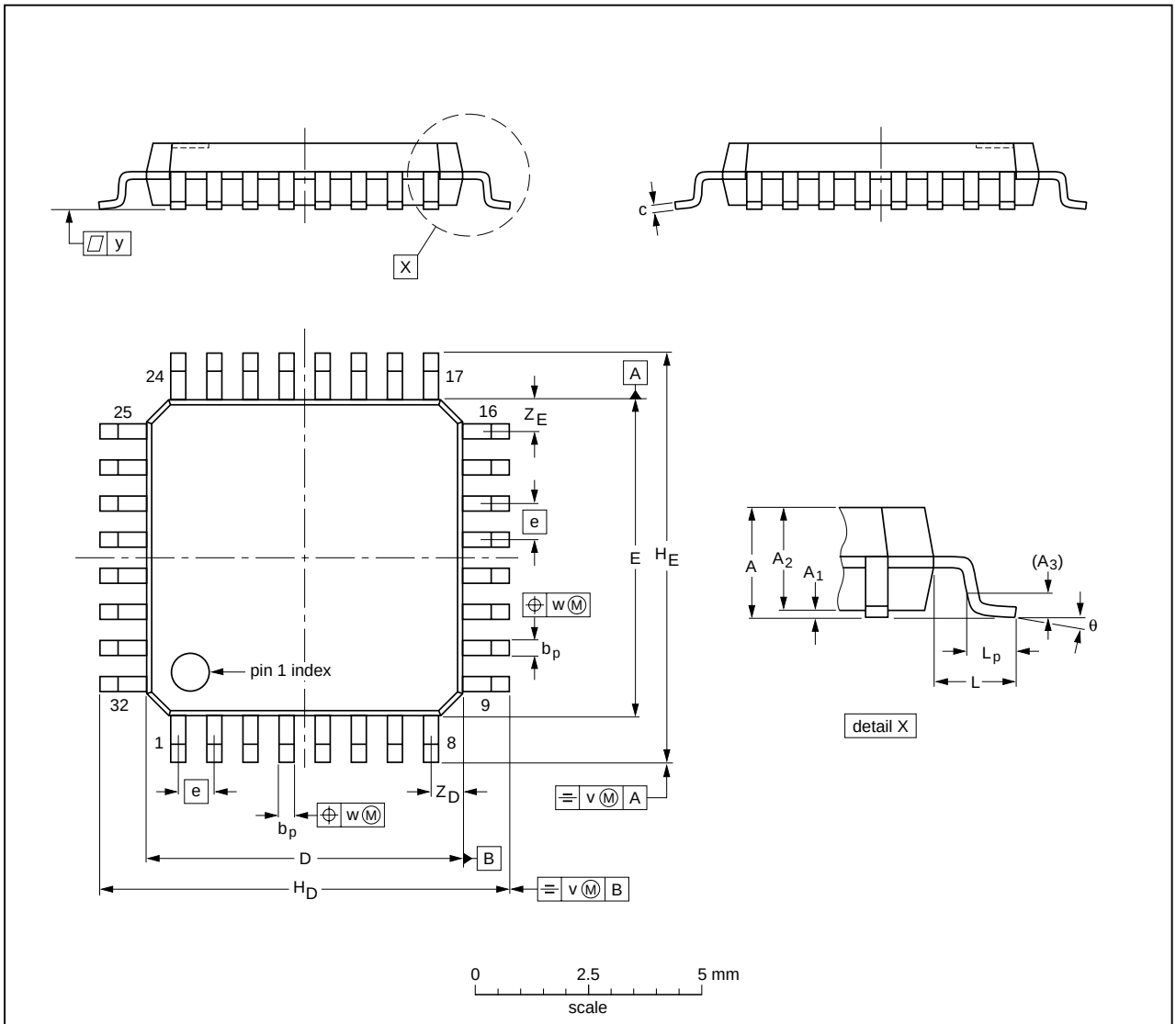
25 Ω = 25 Ω

Fig 6. Optimized dual line termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition, IV characteristics are in the process of being generated to support the other board-level simulators in general use.

12. Package outline

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT358 -1	136E03	MS-026				~~03-02-25~~ 05-11-09

Fig 7. Package outline SOT358-1 (LQFP32)

13. Packing information

Table 8. Packing information

Type number	Ordering code (12NC)	Package	Packing	Description
PCK953BD	9352 679 41118	SOT358-1 (LQFP32)	reel pack, SMD, 13”	180° rotation package orientation in reel
PCK953BD	9352 679 41128	SOT358-1 (LQFP32)	reel pack, SMD, 13”, turned	JEDEC standard package orientation in reel
PCK953BD	9352 679 41151	SOT358-1 (LQFP32)	tray pack, bakeable, single	
PCK953BD	9352 679 41157	SOT358-1 (LQFP32)	tray pack, bakeable, multiple	
PCK953BD/G	9352 761 22128	SOT358-1 (LQFP32)	reel pack, SMD, 13”, turned	JEDEC standard package orientation in reel

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias

- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 8) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020C)

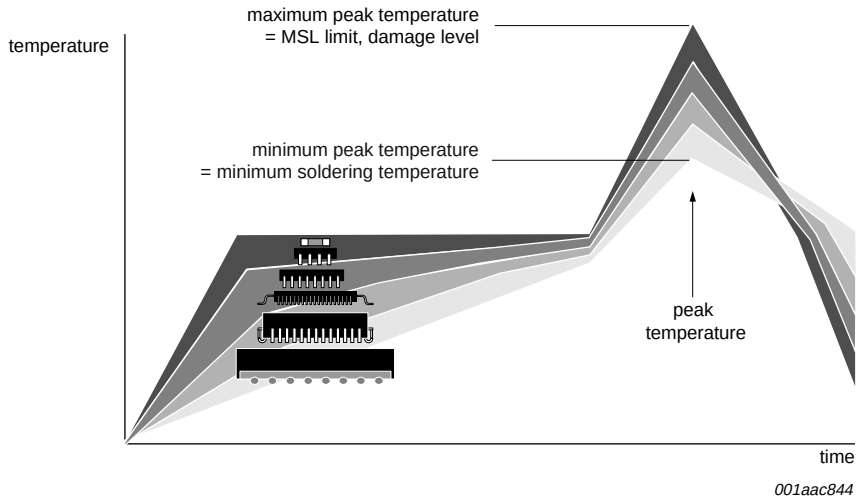
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 8.



MSL: Moisture Sensitivity Level

Fig 8. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
LPF	Low-Pass Filter
LVCMOS	Low Voltage Complementary Metal-Oxide Semiconductor
LVPECL	Low Voltage Positive Emitter-Coupled Logic
LVTTL	Low Voltage Transistor-Transistor Logic
PECL	Positive Emitter-Coupled Logic
PLL	Phase-Locked Loop
RC	Resistor-Capacitor network
SPICE	Simulation Program with Integrated Circuit Emphasis
VCO	Voltage Controlled Oscillator

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCK953_5	20081009	Product data sheet	-	PCK953_4
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 2 “Features”, deleted (old) 8th bullet item • Section 3 “Ordering information”: – added Type number PCK953BD/G – added paragraph following Table 1 • Table 4 “Limiting values”: removed (old) table note 1(now covered under Section 17.3 “Disclaimers”) • Table 5 “Static characteristics”: – changed title of this table from “DC characteristics” to “Static characteristics” – changed symbol “V_{p-p}” to “$V_{i(p-p)}$” – changed symbol/parameter “V_{CMR}, Common mode range” to “V_{cm}, common-mode voltage” – changed symbol “I_{IN}” to “I_I” – changed symbol “C_{IN}” to “C_i” • Table 6 “Dynamic characteristics”: – changed title of this table from “AC characteristics” to “Dynamic characteristics” – split “t_r, t_f” specification into 2 separate items, “$t_{r(o)}$, output rise time” and “$t_{f(o)}$, output fall time” – changed symbol “t_{pw}, output duty cycle” to “δ_o, output duty cycle” – changed symbol “f_{MAX}” to “$f_{o(max)}$” – changed symbol “t_{jitter}” to “$t_{jit(cc)}$” – deleted (old) table note 1 • Added Section 13 “Packing information” • Added soldering information			
PCK953_4 (9397 750 11762)	20030731	Product data	ECN 853-2222 30050 dated 18 June 2003	PCK953_3
PCK953_3 (9397 750 11465)	20030502	Product data	ECN 853-2222 29827 dated 02 May 2003	PCK953_2
PCK953_2 (9397 750 08062)	20010208	Product data	ECN 853-2222 25600 dated 08 Feb 2001	PCK953_1
PCK953_1	20001025	Product data	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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19. Contents

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