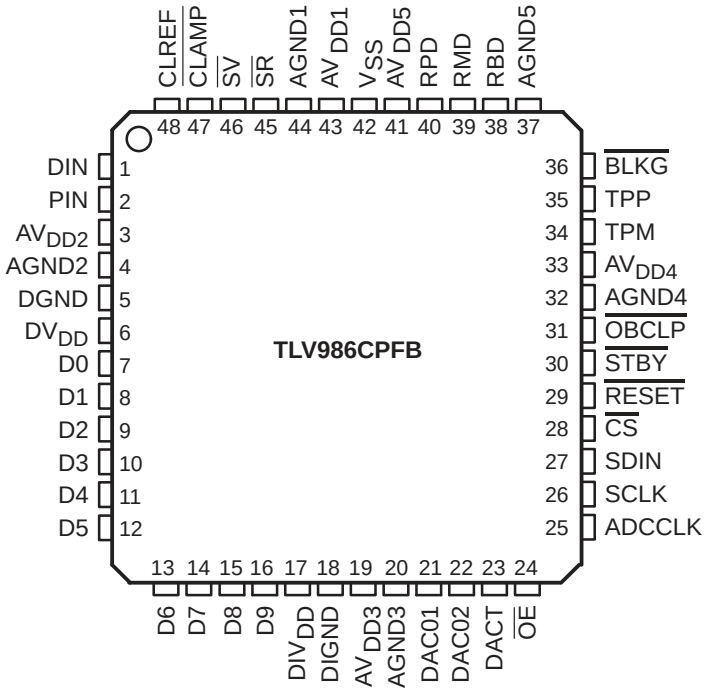
- **10-bit, 12.5 MSPS, A/D Converter**
- **Single 3 V Supply Operation**
- **Low Power: 140 mW Typical at 3-V, 2 mW Power-Down Mode**
- **Full Channel Differential Nonlinearity Error: <±0.5 LSB Typical**
- **Full Channel Integral Nonlinearity Error: <±1 LSB Typical**
- **Programmable Gain Amplifier (PGA) With 0 dB to 36 dB Gain Range (0.1 dB/Step)**
- **Automatic or Programmable Black Level and Offset Calibration**
- **Additional DACs for External Analog Setting**
- **Serial Interface for Register Configuration**
- **Internal Reference Voltages**
- **48-pin TQFP Package**

PFB PACKAGE
(TOP VIEW)



applications

- **PC Camera**
- **Digital Still Camera**
- **Digital Video Camera**

description

The TLV986 is a highly integrated monolithic analog signal processor/digitizer designed to interface the area charge-coupled device (CCD) sensors in digital camera applications. The TLV986 performs all the analog processing functions necessary to maximize the dynamic range, corrects various errors associated with the CCD sensor, and then digitizes the results with an on-chip high-speed analog-to-digital converter (ADC). The key components of the TLV986 include: input clamp circuitry and a correlated double sampler (CDS), a programmable gain amplifier (PGA) with 0 to 36 dB gain range, two internal digital-to-analog converters (DAC) for automatic or programmable optical black level and offset calibration, a 10-bit, 12.5 MSPS pipeline ADC, a parallel data port for easy microprocessor interface, a serial port for configuring internal control registers, two additional DACs for external system control, and internal reference voltages.

Designed in advanced CMOS process, the TLV986 operates from a single 3-V power supply with a normal power consumption of 140 mW and a 2 mW power-down mode.

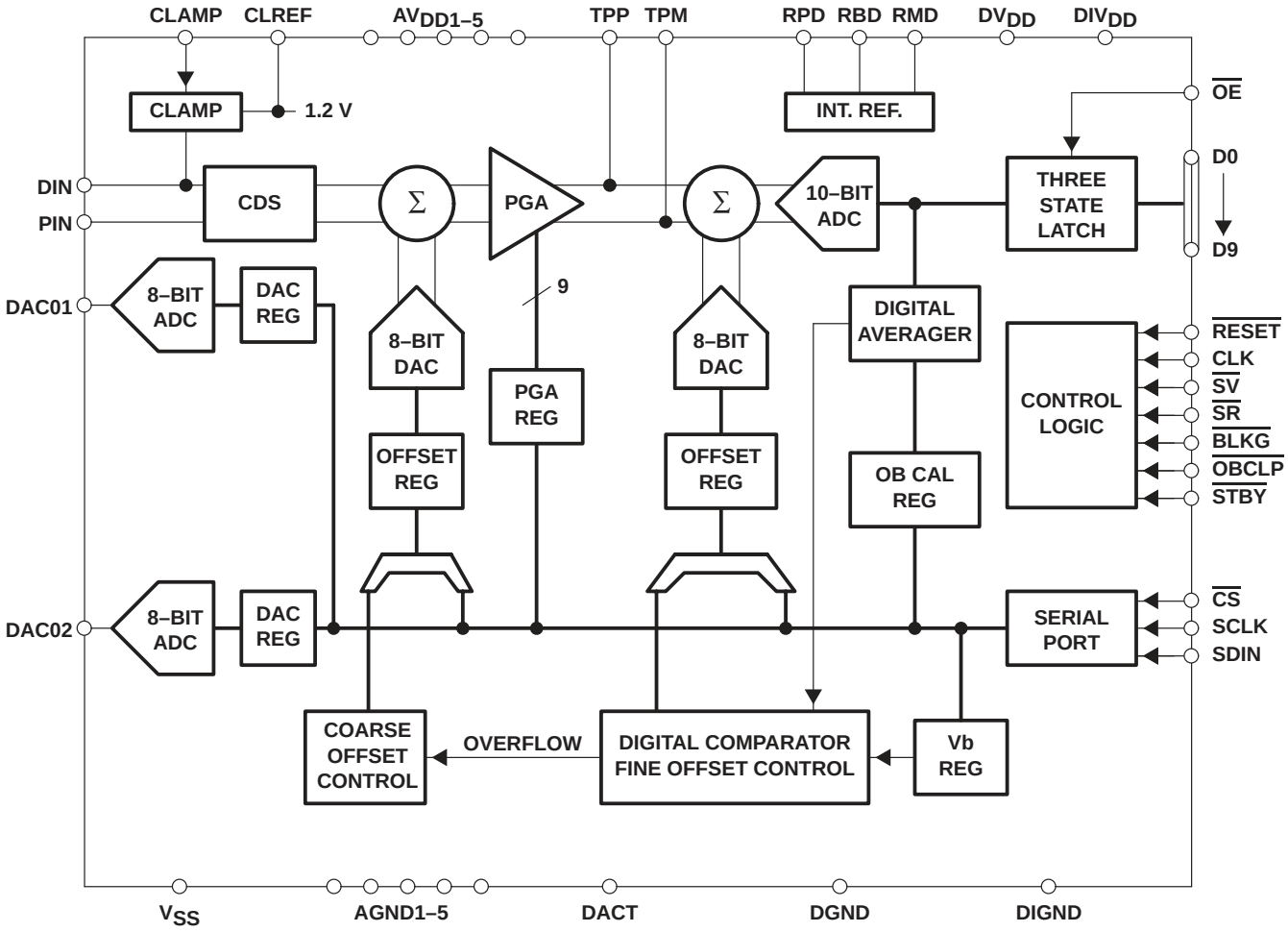
Single 3-V operation, low power consumption, and fully integrated analog processing circuitry make the TLV986 an ideal CCD sensor interfacing solution for the digital camera applications.

The part is available in a 48-pin TQFP package and is specified over 0°C to 70°C operating temperature range.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TQFP (PFB)
–0°C to 70°C	TLV986CPFB

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADCCLK	25	I	ADC clock input
AGND1	44		Analog ground for internal CDS circuits
AGND2	4		Analog ground for internal PGA circuits
AGND3	20		Analog ground for internal DAC circuits
AGND4	32		Analog ground for internal ADC circuits
AGND5	37		Analog ground for internal REF circuits
AV_{DD1}	43		Analog supply voltage for internal CDS circuits, 3 V
AV_{DD2}	3		Analog supply voltage for internal PGA circuits, 3 V
AV_{DD3}	19		Analog supply voltage for internal DAC circuits, 3 V
AV_{DD4}	33		Analog supply voltage for internal ADC circuits, 3 V
AV_{DD5}	41		Analog supply voltage for internal ADC circuits, 3 V
$\overline{BLKG}$	36		Control input. The CDS operation is disabled when the BLKG is pulled low.
$\overline{CLAMP}$	47	I	CCD signal clamp control input
CLREF	48	O	Clamp reference voltage output
$\overline{CS}$	28	I	Chip Select. A logic low on this input enables the TLV986.
D0–D9	7–16	O	10-bit 3-state ADC output data or offset DACs test data
DACO1	21	O	Digital-to-analog converter output1
DACO2	22	O	Digital-to-analog converter output2
DACT	23	O	MUXed test output for internal offset DACs
DGND	5		Digital ground
DIGND	18		Digital interface circuit ground
DIN	1	I	Input signal from CCD
DIV_{DD}	17		Digital interface circuit supply voltage, 1.8 V – 4.4 V
DV_{DD}	6		Digital supply voltage, 3-V
$\overline{OBCLP}$	31	I	Optical black level and offset calibration control input, active low
$\overline{OE}$	24	I	Output data enable, active low
PIN	2	I	Input signal from CCD
$\overline{RESET}$	29	I	Hardware reset input, active low. This signal forces a reset of all internal registers.
RBD	38	O	Internal bandgap reference for external decoupling
RMD	39	O	Ref– output for external decoupling
RPD	40	O	Ref+ output for external decoupling
SCLK	26	I	Serial clock input. This clock synchronizes the serial data transfer.
SDIN	27	I	Serial data input to configure the internal registers
$\overline{SR}$	45	I	CCD reference level sample clock input
$\overline{STBY}$	30	I	Hardware power-down control input, active low
$\overline{SV}$	46	I	CCD signal level sample clock input
TPM	34	O	Muxed test output: PGA noninverting output or inverted PGA clock
TPP	35	O	Muxed test output: PGA inverting output or inverted CDS clock
V_{SS}	42		Silicon substrate, normally connected to analog ground

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, AV_{DD}, DV_{DD}, DIV_{DD} . . . . . –0.3 V to 6.5 V
Analog input voltage range . . . . . –0.3 V to AV_{DD}+0.3 V
Digital input voltage range . . . . . –0.3 V to AV_{DD}+0.3 V
Operating virtual junction temperature range, T_J . . . . . –40°C to 150°C
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{STG} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

power supplies

	MIN	NOM	MAX	UNIT
Analog supply voltage, AV_{DD}	2.7	3	3.3	V
Digital supply voltage, DV_{DD}	2.7	3	3.3	V
Digital interface supply voltage, DIV_{DD}	1.8		4.4	V

digital inputs

		MIN	NOM	MAX	UNIT
High–level input voltage, V_{IH}	DIV_{DD} = 3 V	0.8DIV_{DD}			V
Low–level input voltage, V_{IL}	DIV_{DD} = 3 V			0.2DIV_{DD}	V
Input ADCCLK frequency	DV_{DD} = 3 V			12.5	MHz
ADCCLK pulse duration, clock high, $t_{w(MCLK)}$	DV_{DD} = 3 V	40			ns
ADCCLK pulse duration, clock low, $t_{w(MCLKL)}$	DV_{DD} = 3 V	40			ns
Input SCLK frequency	DV_{DD} = 3 V			40	MHz
SCLK pulse duration, clock high, $t_{w(SCLKH)}$	DV_{DD} = 3 V	12.5			ns
SCLK pulse duration, clock low, $t_{w(SCLKL)}$	DV_{DD} = 3 V	12.5			ns

electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, AV_{DD} = DV_{DD} = 3 V, ADCCLK = 12.5 MHz (unlessotherwise noted)

total device

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	AV_{DD} operating current			41		mA
	DV_{DD} operation current			6		mA
	Device power consumption			140		mW
	Power consumption in power–down mode			2		mW
INL	Full channel integral nonlinearity	AV_{DD} = DV_{DD} = 2.7 V – 3.3 V		±1	±2	LSB
DNL	Full channel differential nonlinearity		–1	±0.5	1.5	LSB
	No missing code			Assured		
	Full channel output latency			4.5		CLK cycles

analog-to-digital converter (ADC)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	ADC resolution				10	Bits
	Full scale input span			2		V_{P-P}
	Conversion rate				12.5	MHz

correlated double sampler (CDS) and programmable gain amplifier (PGA)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	CDS and PGA sample rate				12.5	MHz
	CDS full scale input span	Single-ended input			1	V
	Input capacitance of CDS			4		pF
	Minimum PGA gain			0	1	dB
	Maximum PGA gain		35	36	37	dB
	PGA gain resolution			0.1		dB
	PGA programming code resolution	8-bit monotonic gain control		9		Bits

internal digital-to-analog converters (DAC) for offset correction

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	DAC resolution				8	Bits
INL	Integral nonlinearity			±0.5	±1.2	LSB
DNL	Differential nonlinearity			±0.5	±0.9	LSB
	Output settling time	To 1% accuracy		80		ns

user digital-to-analog converters (DAC)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	DAC resolution				8	Bits
INL	Integral nonlinearity			±0.5	±1.2	LSB
DNL	Differential nonlinearity			±0.6	±0.9	LSB
	Output voltage range		0		3	V
	Output settling time	10 pF external load. Settle to 1 mV.		4		µs

electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, AV_{DD} = DV_{DD} = 3 V, ADCCLK = 12.5 MHz (unlessotherwise noted) (continued)

reference voltages

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Internal bandgap voltage reference		1.43	1.50	1.58	V
	Temperature coefficient			100		ppm/°C
	ADC Reference+	Externally decoupled	1.8	2	2.2	V
	ADC Reference–		0.9	1	1.1	V

digital specifications

logic inputs

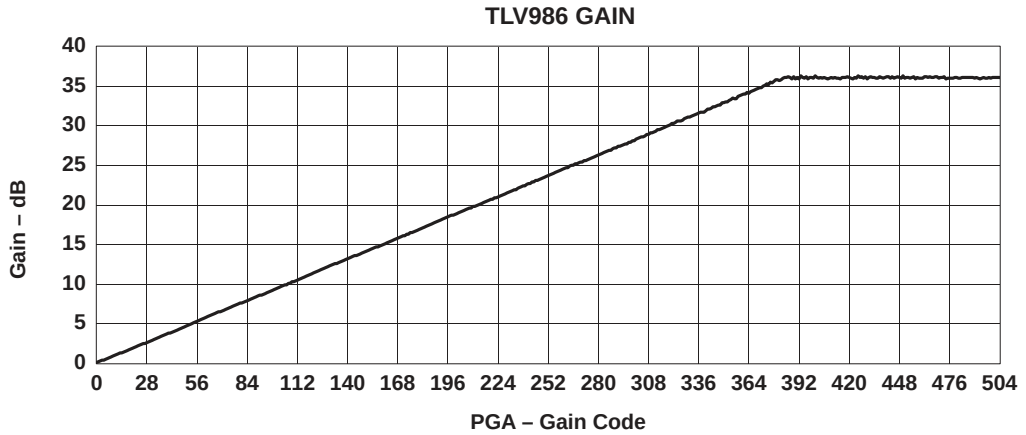
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	DIV_{DD} = 3 V	–10		10	µA
I_{IL}	Low-level input current		–10		10	µA
C_i	Input capacitance			5		pF

logic outputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 50 µA, DIV_{DD} = 3 V		DIV_{DD}–0.4		V
V_{OL}	Low-level output voltage	I_{OL}= 50 µA, DIV_{DD} = 3 V		0.4		V
I_{OZ}	High-impedance-state output current		–10		10	µA
C_O	Output capacitance			5		pF

key timing requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(SRW)}$	SR pulse width	Measured at 50% of pulse height	10			ns
$t_{(SVW)}$	SV pulse width		10			ns
$t_{(OBS)}$	OBCLP falling edge to ADCCLK rising edge	Minimum 0.25 × one ADCCLK cycle				
$t_{(OBE)}$	ADCCLK falling edge to OBCLP rising edge	Not critical, but should not exceed 2^N pixels				
$t_{(OD)}$	ADCCLK to output data delay		4		9	ns
$t_{(CSF)}$	CS falling edge to SCLK rising edge		0			ns
$t_{(CSR)}$	SCLK falling edge to CS rising edge		5			ns



TYPICAL CHARACTERISTICS

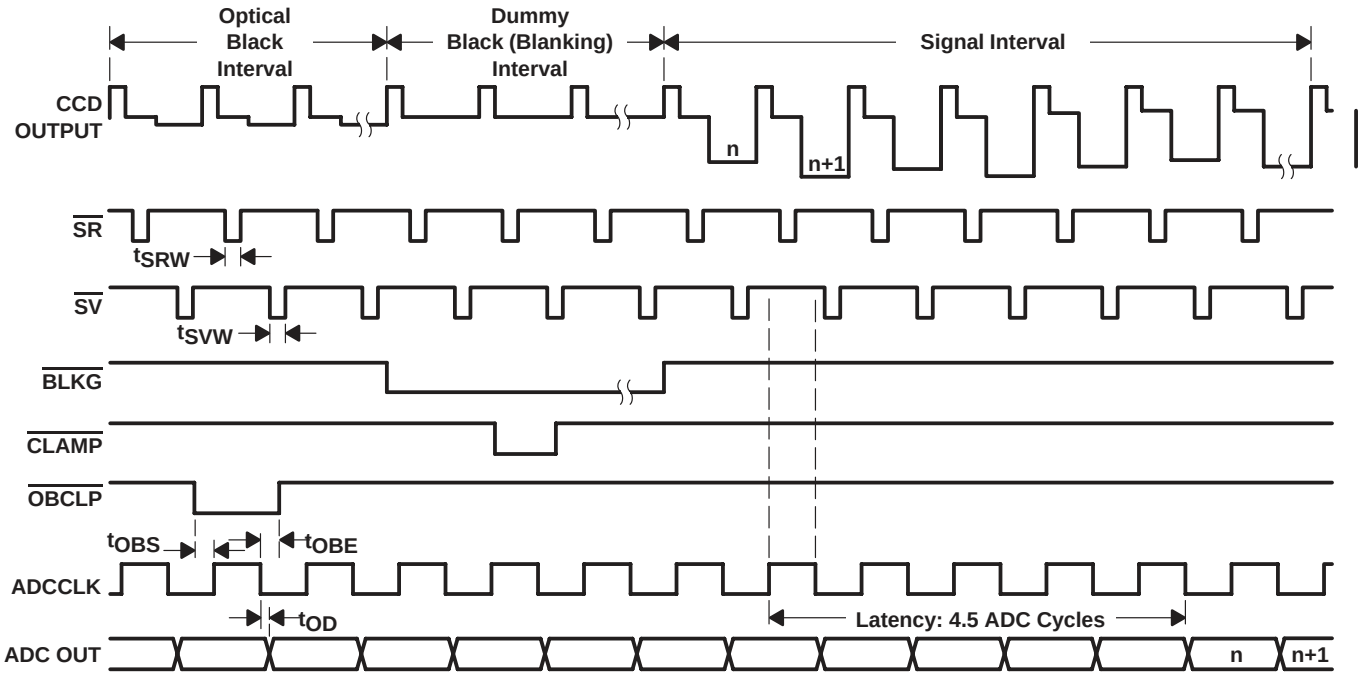


Figure 1. System Operation Timing Diagram

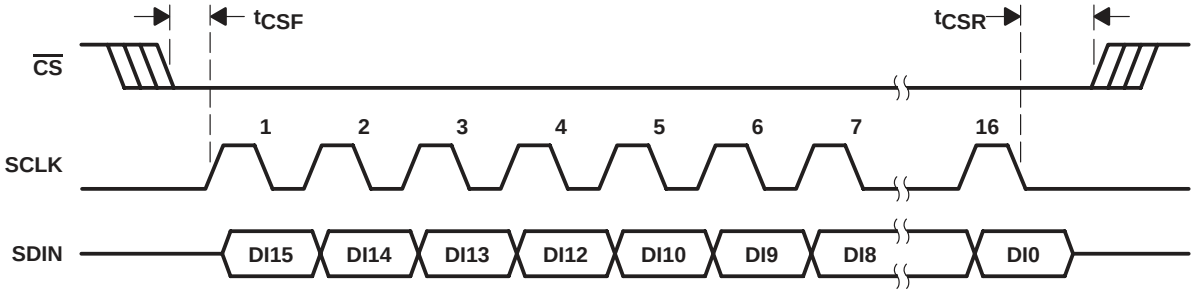
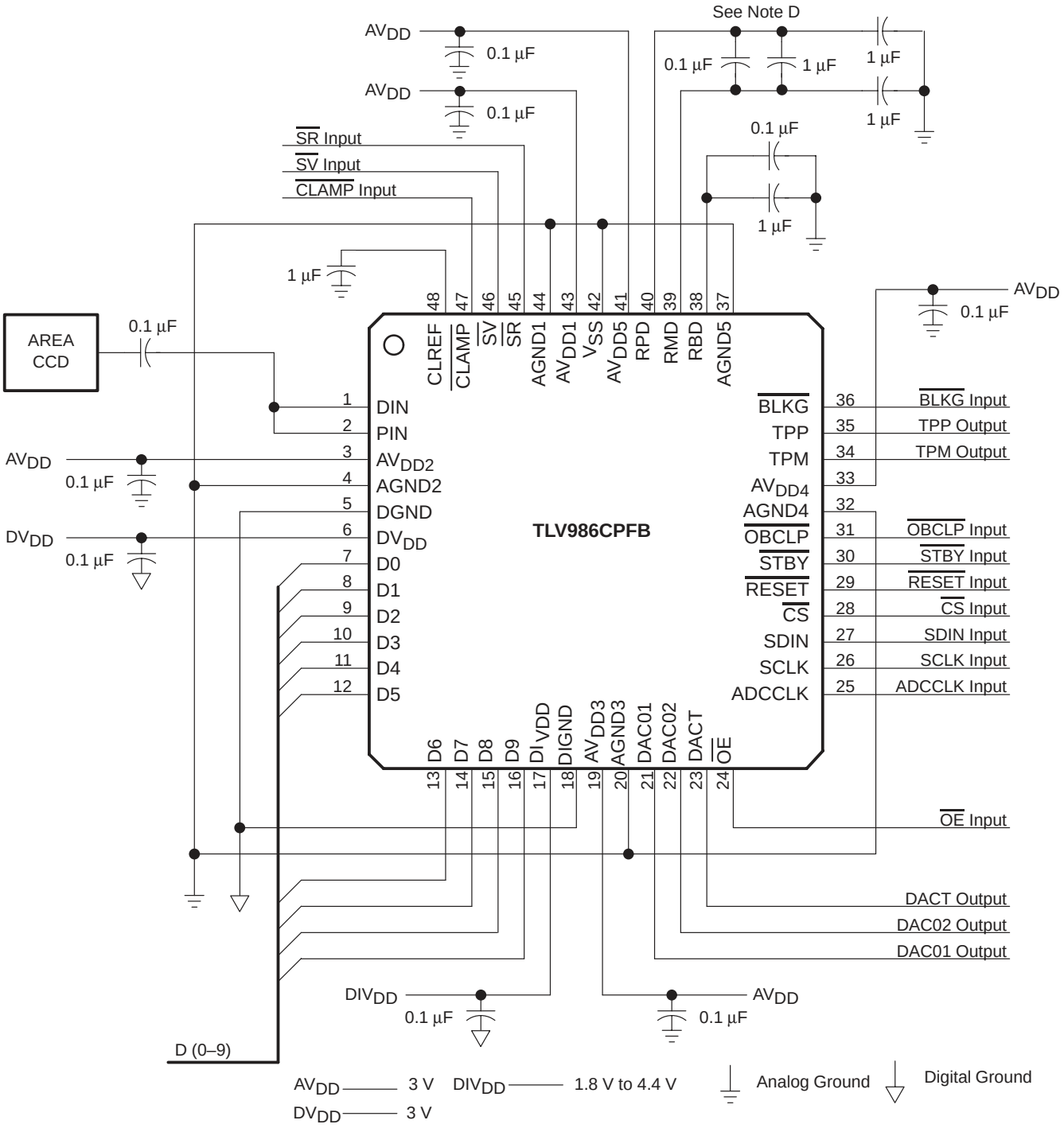


Figure 2. Serial Interface Timing Diagram

APPLICATION INFORMATION



NOTES: A. All analog outputs should be buffered if the load is resistive If the load is capacitive with more than 2 pF loading.
B. When using the TPP and TPM pins to test internal PGA, the AVDD supply voltage should be 3.3 V.
C. Clock signals on the TPP and TPM terminals are inverted.
D. Place these two capacitors as close to the device as possible.

Figure 3. Typical Application Connection

REGISTER DEFINITION

serial input data format

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
X	X	A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

A3	A2	A1	A0	
0	0	0	0	Control register
0	0	0	1	PGA gain register
0	0	1	0	User DAC1 register
0	0	1	1	User DAC2 register
0	1	0	0	Coarse offset DAC
0	1	0	1	Fine offset DAC
0	1	1	0	Digital Vb register (set reference code level at the ADc output during the optical black interval)
0	1	1	1	Optical black register (set the number of black pixels per line and number of the lines for digital averaging)
1	0	0	0	Test register

D9 – D0
10-bit data to be written into the selected register

control register format

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STBY	PDD1	PDD2	ACD	AFD	X	X	X	RTOB	RTSY

control register description

BIT	NAME	DESCRIPTION
D9	STBY	Device power down control: 1 = standby, 0 = active (default)
D8	PDD1	Power down the user DAC1: 1 = standby, 0 = active (default)
D7	PDD2	Power down the user DAC2: 1 = standby, 0 = active (default)
D6	ACD	Coarse offset DAC mode control: 0 = Auto calibration (default), 1 = Bypass auto calibration Note: When D6 is set to 0, D5 must also be set to 0 (automode). Otherwise, the automode will be disabled on both offset DACs.
D5	AFD	Fine offset DAC mode control: 0 = Auto calibration (default), 1 = Bypass auto calibration. Note: D5 can be set to 0 with or without the D6 being set to 0.
D4 – D2	X	Reserved
D1	RTOB	Write 1 to this bit will reset calculated black-level results in the digital averager.
D0	RTSY	#Write 1 to this bit will rewet entire system to the default settings.

PGA register format

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0

Default PGA gain = X000000000 or 0 dB

user DAC1 and DAC2 registers format

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
S	S	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0

Default user DAC register value = XX00000000

REGISTER DEFINITION

coarse offset DAC register format

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	SIGN	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0

coarse offset DAC register description

BIT	NAME	DESCRIPTION
D9	X	Reserved
D8	SIGN	Coarse DAC sign bit, 0 = + sign (default), 1 = – sign
D7–D0		Coarse DAC control data when the D6 in the control register is set at 1.

Default coarse DAC register value = X000000000

fine offset DAC register format

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	SIGN	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0

fine offset DAC register description

BIT	NAME	DESCRIPTION
D9	X	Reserved
D8	SIGN	Fine DAC sign bit, 0 = + sign (default), 1 = – sign
D7–D0		Fine DAC control data when the D5 in the control register is set at 1.

Default fine DAC register value = X000000000

digital Vb (optical black level) register format

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT9	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0

Default Vb register value = 40 hex

REGISTER DEFINITION

optical black calibration register format

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OMUX1	OMUX0	LN4	LN3	LN2	LN1	MP	PN2	PN1	PN0

optical black calibration register description

BIT	NAME	DESCRIPTION
D9, D8	OMUX1, OMUX0	These two bits multiplex digital output (data presented at D[9:0] pins): OMUX1 OMUX0 0 0 D[9:0] = ADC output (default) 0 1 D[9:0] = ADC output 1 0 D[9] = fine/coarse (1/0) auto–correction flag 1 1 D[9] = fine/coarse (1/0) auto–correction flag D[8] = fine DAC sign D[7:0] = fine DAC value
D7–D4	LN4–LN0	Number of black lines for moving average = 2^L. The L can be 0, 1, 2, 3, 4, 5, 6, 7, and 8. Or number of lines can be 1(default), 2, 4, 8, 16, 32, 64, 128, and 256. The maximum number of lines is 256 even if L>8.
D3	MP	When this bit is *1*, the number of black pixels to be averaged per line (2^N) is multiplied by 3. By setting the MP and PN2–PN0 bits together, the number of optical black pixels can be programmed to have the following numbers: 1, 2, 3 (1X3), 4, 6 (2×3), 8, 12 (4×3), 16, 24 (8×3), 32, 48 (16×3), 64, 96 (32×3), and 192 (64×3). Default: MP = 0, no multiplication.
D2–D0	PN2–PN0	Number of black pixels per line to average = 2^N The N can be 0, 1, 2, 3, 4, 5, and 6. Or number of pixels per line can be 1, 2, 4, 8 (default), 16, 32, and 64. The maximum number of pixels per line is 64 even if N>6.

Default optical black calibration register value = 0000000011

REGISTER DEFINITION

optical black calibration register format

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TB9	TB8	TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0

Default test register value = 0110000000

test register description

BIT	NAME	DESCRIPTION
D9–D6	TB9–TB6	These four bits are used to program the internal dc bias current. The bias current programming uses following equation: I_{bias} = 8 μA + (code) × 2 μA Hence, I_{bias} varies from 8 μA (code=0000) to 38 μA (code=1111), with a linear step of 2 μA. Recommend to set the code to 0101.
D5, D4	TB5, TB4	Test outputs (pin 34/35 – TPM/TPP) control: TB5 TB4 0 0 or 1 High impedance outputs at pin TPP and TPM. 1 0 Inverted internal CDS clock at pin TPP. Inverted internal PGA clock at pin TPM. 1 1 PGA noninverting output at pin TPP. PGA inverting output at pin TPM.
D3	TB3	1 – use external reference, power down internal reference 0 – use internal reference (default).
D2	TB2	Reserved
D1, D0	TB1, TB0	Test output (pin 23 – DACT) control for offset DACs: TB1 TB0 0 0 or 1 High impedance outputs at pin DACT (default = 00) 1 0 DACT = fine offset DAC output at pin DACT 1 1 DACT = coarse offset DAC output at pin DACT

PRINCIPLES OF OPERATION

CDS/PGA signal processor

The output from the CCD sensor is first fed to a correlated double sampler (CDS). The CCD signal is sampled and held during the reset reference interval and the video signal interval. By subtracting two resulting voltage levels, the CDS removes low frequency noise from the output of the CCD sensor and obtains the voltage difference between the CCD reference level and the video level of each pixel. Two sample/hold control pulses ($\overline{SR}$ and $\overline{SV}$) are required to perform the CDS function.

The CCD output is capacitively coupled to the TLV986. The ac coupling capacitor is clamped to establish proper dc bias during the dummy pixel interval by the $\overline{CLAMP}$ input. The bias at the input to the TLV986 is set to 1.2 V. Normally, the $\overline{CLAMP}$ is applied at sensor's line rate. Connect a capacitor with a value ten times larger than the input ac coupling capacitor between the CLREF terminal and the AGND.

When operating the TLV986 at its maximum speed, the CCD internal source resistance should be less than 50 Ω. Otherwise, the CCD output buffering is required.

The signal is sent to the PGA after the CDS function is complete. The PGA gain is adjustable from 0 to 36 dB by programming the internal gain register via the serial port. The PGA is digitally controlled with 9-bit resolution on a linear dB scale, resulting in a 0.09 dB gain step. The gain can be expressed by the following equation,

$$\text{Gain} = \text{PGA code} \times 0.09375 \text{ dB}$$

Where: PGA code has a range of 0 to 383

For example, If PGA code = 64, then the PGA Gain = 6 db (or gain of 2)

The TLV986 has direct access to the PGA outputs through the TPP terminal and the TPM terminal. See *Test Register Description* for details.

ADC

The ADC employs a pipelined architecture to achieve high throughput and low power consumption. Fully differential implementation and digital error correction ensure 10-bit resolution.

The latency of the ADC data output is 4.5 ADCCLK cycles as shown in Figure 1. Pulling $\overline{OE}$ (terminal 24) high puts the ADC output in high impedance.

user DACs

The TLV986 includes two user DACs that can be used for external analog settings. The output voltage of each DAC can be independently set and has a range of 0 V to the supply voltage with 8-bit resolution. When the user DACs are not in use in a camera system, they can be put in the standby mode by programming control bits in the control register.

PRINCIPLES OF OPERATION

internal timing

Operating the CDS requires signals $\overline{SR}$ and $\overline{SV}$ as previously explained. The user needs to synchronize the $\overline{SR}$ and $\overline{SV}$ clocks with the CCD signal waveform. The output of the ADC is read out to external circuitry by the ADCCLK signal that is also used internally to control both ADC and PGA operations. It is necessary that the positive half cycle of the ADCCLK signal always falls in between two adjacent $\overline{SV}$ pulses as shown in Figure 1. The user can then fine tune the ADCCLK timing in relation to the CDS timing to achieve optimal performance.

The TLV986 has direct access to the CDS and PGA internal clocks through the TPP and TPM terminal. The TPP and TPM assist the user in timing alignment. See *Test Register Description* for details.

The $\overline{CLAMP}$ signal activates the input clamping and the $\overline{OBCLP}$ signal activates auto optical black and offset correction.

input blanking function

During some period of operation, large input transients may occur at the TLV986's input, saturating the input circuits and causing long recovery time. To prevent the circuit saturation, the TLV986 includes an input blanking function that blocks the input signals by disabling the CDS operation whenever the BLKG input is pulled low.

3-wire serial interface

A simple 3-wire (SCLK, SDIN, and $\overline{CS}$) serial interface is provided to allow writing to the internal registers of the TLV986. The serial clock SCLK can be run at a maximum speed of 40 MHz. The serial data SDIN is 16 bits long. After two leading null bits, there are four address bits for which internal register is to be updated; the following ten bits are the data to be written to the register. To enable the serial port, the $\overline{CS}$ pin must be held low. The data transfer is initiated by the incoming SCLK after the $\overline{CS}$ falls.

device reset

When the reset (terminal 29) is pulled low, all internal registers are set to their default values. The device also resets itself when it is first powered on. In addition, the TLV986 has a software-reset function that resets the device when writing a control bit to the control register. See *Register Definition* section for the register default values.

device reset

When the reset (terminal 29) is pulled low, all internal registers are set to their default values. The device also resets itself when it is first powered on. In addition, the TLV986 has a software-reset function that resets the device when writing a control bit to the control register. See *Register Definition* section for the register default values.

power-down mode (standby)

The TLV986 has both hardware and software power–down modes. Pulling the $\overline{STBY}$ (terminal 30) low puts the device in the low-power standby mode. Total supply current drops to ~0.6 mA. Setting a power-down control bit in the control register can also activate the power-down mode. The user can still program all internal registers during the power-down mode.

PRINCIPLES OF OPERATION

voltage references

An internal precision voltage reference of 1.5 V nominal is provided. This reference voltage is used to generate the ADC Ref– voltage of 1 V and Ref+ of 2 V. It also sets the clamp voltage. All internally-generated voltages are fixed values and cannot be adjusted.

power supply

The TLV986 has several power supply pins. Each major internal analog block has a dedicated AV_{DD} supply terminal. All internal digital circuitry is powered by the DV_{DD}. Both AV_{DD} and DV_{DD} are 3 V nominal.

The DIV_{DD} and DIGND pins supply power to the output digital driver (D9–D0). The DIV_{DD} is independent of the DV_{DD} and can be operated from 1.8 V to 4.4 V. This allows the outputs to interface with digital ASICs requiring different supply voltages.

grounding and decoupling

General practices apply to the PCB design to limit high frequency transients and noise that are fed back into the supply and reference lines. This requires that the supply and reference terminals be sufficiently bypassed. In the case of power supply decoupling. A 0.1 μF ceramic chip capacitor are adequate to keep the impedance low over a wide frequency range. Recommended external decoupling for the three voltage reference terminals is shown in Figure 3. Since their effectiveness depends largely on the proximity to the individual supply terminal, all decoupling capacitors should be placed as close to the supply terminals as possible.

To reduce high-frequency and noise-coupling, it is highly recommended that digital and analog ground be shorted immediately outside the package. This can be accomplished by running a low impedance line between the DGND and AGND, under the package.

automatic optical black and offset correction

In the TLV986, the optical black and system channel offset corrections are performed by an auto digital feadback loop. Two DACs are used to compensate for both channel offset and the optical black offset. A coarse correction DAC (CDAC) is located before PGA gain stage and a fine correction DAC (FDAC) is located after the gain stage. The digital calibration system is capable of correcting the optical black and channel offset down to one ADC LSB accuracy.

The TLV986 automatically starts the auto-calibration whenever the $\overline{\text{OBCLP}}$ input is pulled low, the $\overline{\text{OBCLP}}$ pulse should be wide enough to cover one positive half cycle of the ADCCLK as shown in Figure 1.

For each line, the optical black pixels plus the channel offset are sampled and converted to digital data by the ADC. A digital circuit averages the data during the optical black pixels. The final averaged result is compared digitally with the desired output code stored in the Vb register (default is 40H), then control logic adjusts the FDAC to make the ADC output equal to the Vb. If the offset is out of the range of the FDAC (±255 ADC LSBs), the error is corrected by both CDAC and FDAC. The CDAC increments or decrements by one CDAC LSB depending on whether the offset is negative of positive, until the output is within the range of the FDAC. The remaining residue is corrected by the FDAC.

The relationship among the FDAC, CDAC, and ADC in terms of number of ADC LSBs is as follows,

1 FDAC LSB = 1 ADC LSB,

1 CDAC LSB = 0.5 x PGA linear gain × 1 ADC LSB.

For example, if PGA gain = 2 (6 dB), then, 1 CDAC LSB = 1 ADC LSBs.

PRINCIPLES OF OPERATION

automatic optical black and offset correction (continued)

After the auto-calibration is complete, the ADC's digital output during CCD signal interval can be expressed by the following equation,

ADC output [D9–D0] = CCD_input × PGA gain + Vb,

Where: Vb is the desired black level selected by user.

The total offset including optical black offset is calibrated to be equal to the Vb by adjusting the offset correction DACs during the auto-calibration.

The number of black pixels in each line and number of lines are programmable. The number of black pixels per line that can be averaged equals to 2^N, where N can be 0, 1, 2, 3, 4, 5, and 6. The number of lines equals to 2^L, where L can be 0, 1, 2, 3, 4, 5, 6, 7, and 8.

The auto-calibration feature can be bypassed if the user prefers to directly program the offset DAC registers. Switching the auto-calibration mode to the direct programming mode requires two register writes. First, the control bits for the offset DACs in the control register needs to be changed then desired offset value for the register is loaded to the offset DAC registers for proper error correction. If the total offset including optical black level is less than ±255 ADC LSBs, only the FDAC needs to be programmed. When switching from the direct programming mode to the auto-calibration mode, the previous DAC register values are used as starting offsets rather than default DAC register values.

A detailed block diagram for the internal automatic optical black and offset correction is shown in Figure 4. The timing diagram in Figure 5 illustrates the operation of the calibration system. In the example, the TLV986 is programmed to average four black pixels (N=2) per line for two lines (L=1).

PRINCIPLES OF OPERATION

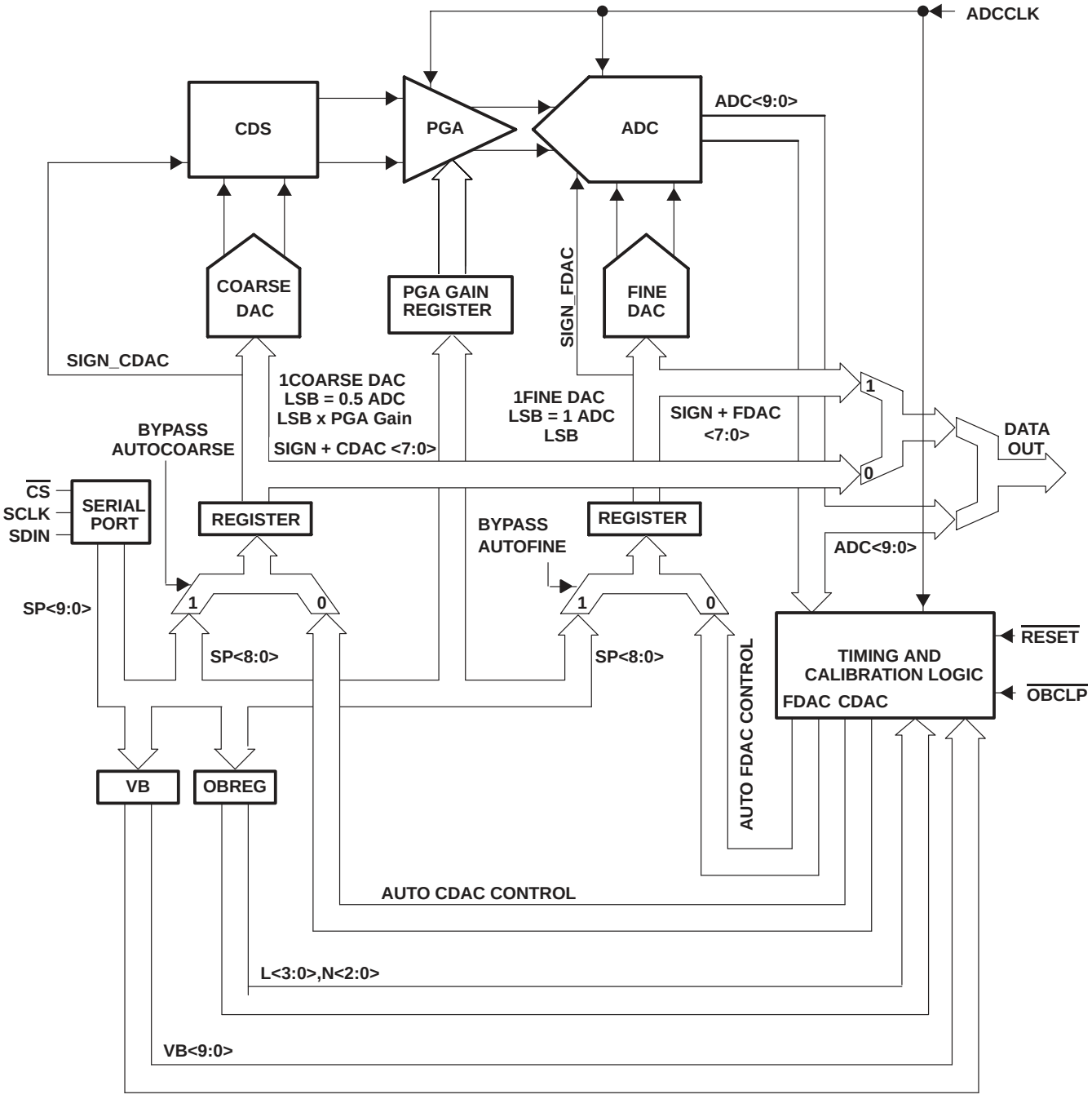
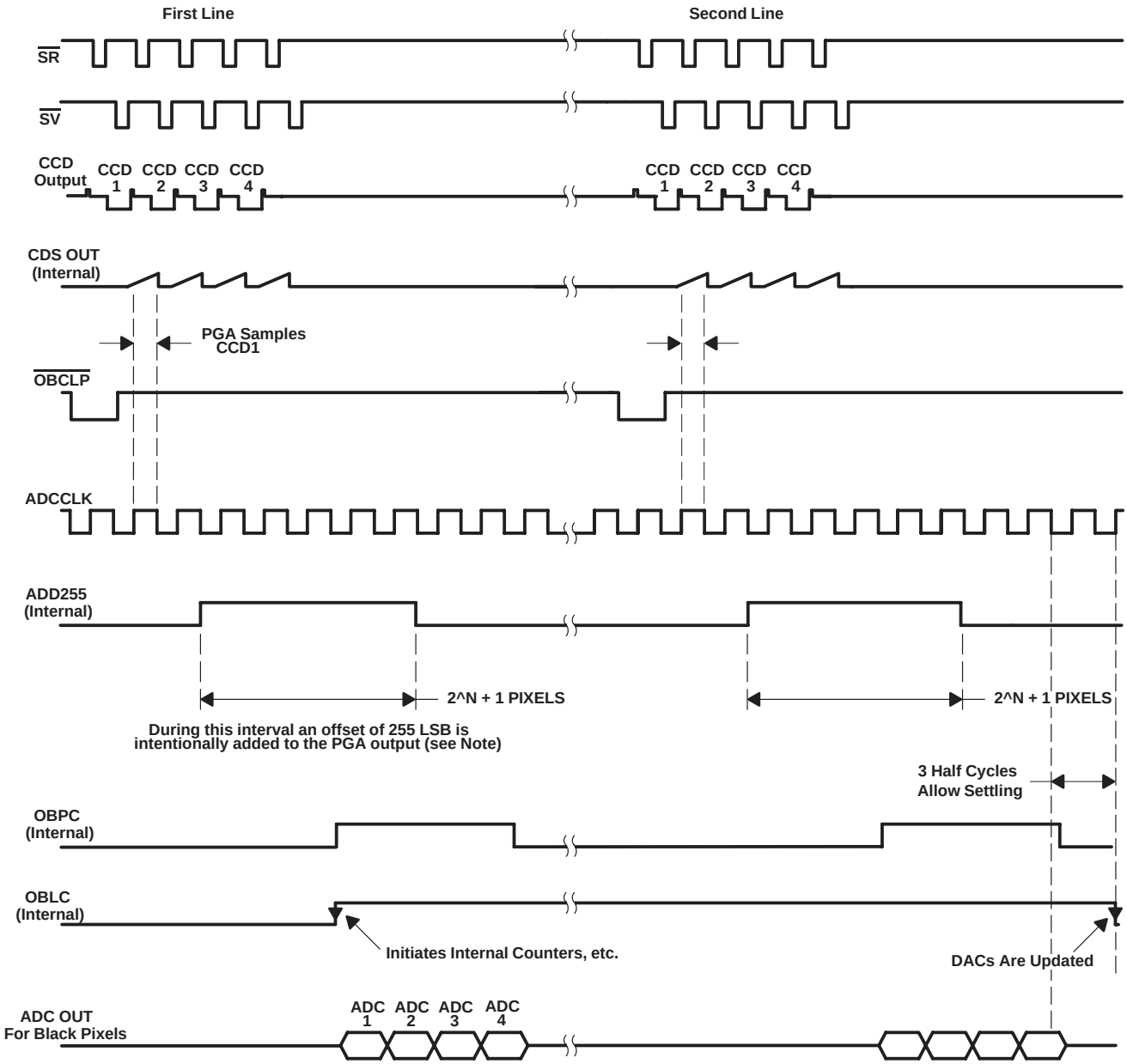


Figure 4. Optical Black and Offset Correct Block Diagram

PRINCIPLES OF OPERATION

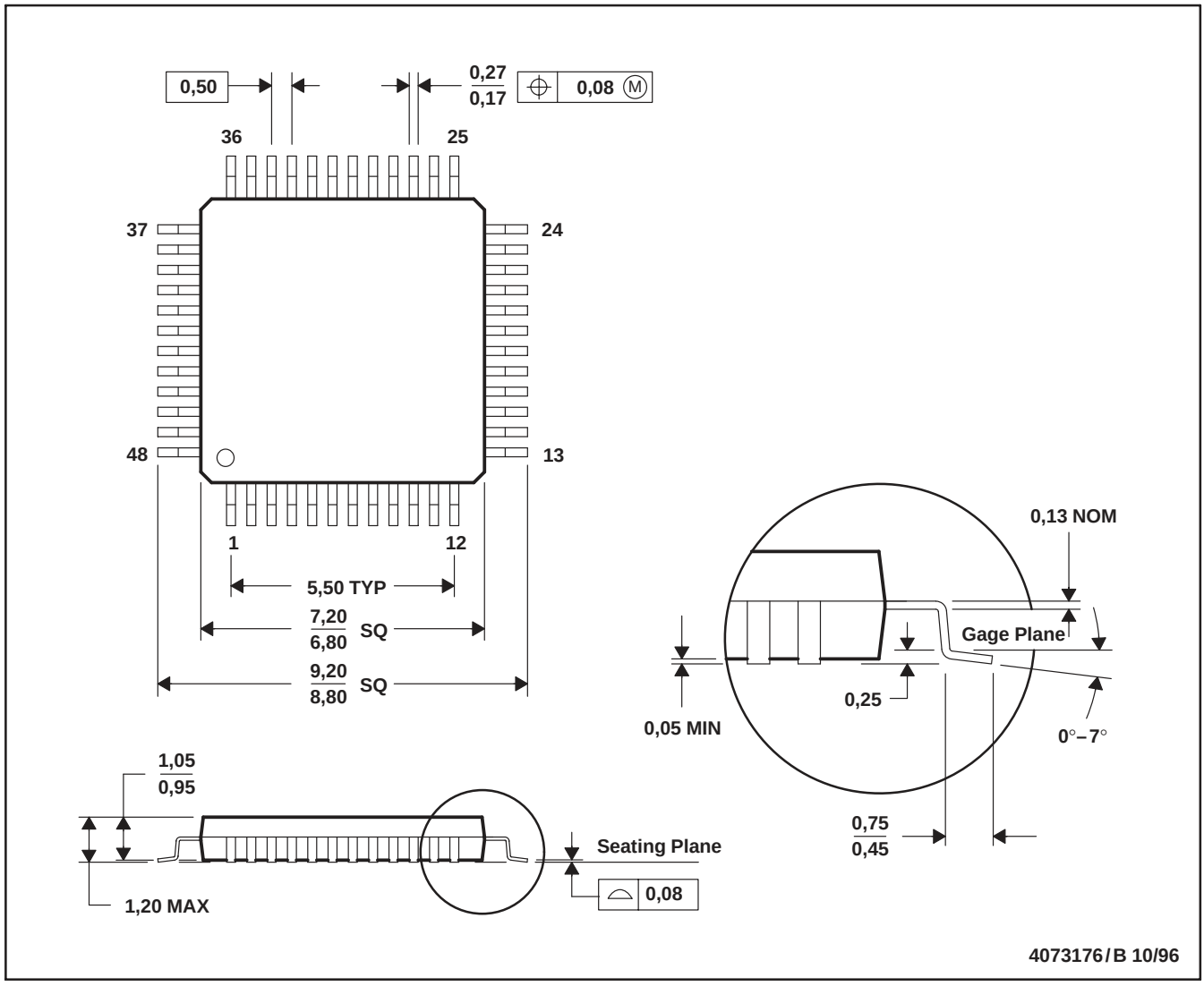


NOTE: To avoid the ADC being clipped on differential negative input signals, an internal offset that equals to 255 ADC LSBs is intentionally added to the PGA output signal. This offset is only added during optical black pixel interval with a total duration of 2^N + 3 pixels, where three additional pixels are necessary for accommodating internal latency adjustment.

Figure 5. Optical Black and Offset Correction Timing

MECHANICAL DATA

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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