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September 2016

FCPF150N65F

N-Channel SuperFET® II FRFET® MOSFET

650 V, 24 A, 150 mΩ

Features

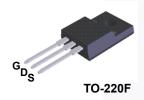
- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 133 m Ω
- Ultra Low Gate Charge (Typ. Q_q = 72 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 361 pF)
- · 100% Avalanche Tested
- · RoHS Compliant

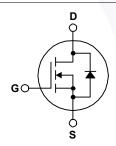
Applications

- Telecom/Server Power Supplies Solar Inverters
- · Computing Power Supplies
- · FPD TV Power/Lighting

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. SuperFET II FRFET® MOSFET combines a faster and more rugged intrinsic body diode performance with fast switching, aimed at achieving better reliability and efficiency especially in resonant switching applications. SuperFET II FRFET is very suitable for the switching power applications such as server/telecom power, Solar inverter, FPD TV power, computing power, lighting and industrial power applications.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FCPF150N65F	Unit
V _{DSS}	Drain to Source Voltage			650	V
V	Coto to Course Voltage	- DC		±20	V
V_{GSS}	Gate to Source Voltage	- AC	(f > 1 Hz)	±30	V
	Drain Current	- Continuous (T _C = 25°C)		24*	Α
ID	Drain Current	- Continuous (T _C = 100°C)		14.9*	A
I _{DM}	Drain Current	- Pulsed	(Note 1)	72*	Α
E _{AS}	Single Pulsed Avalanche Ene	ergy	(Note 2)	663	mJ
I _{AR}	Avalanche Current		(Note 1)	4.7	Α
E _{AR}	Repetitive Avalanche Energy (Note 1)		2.98	mJ	
dv/dt	MOSFET dv/dt			100	V/ns
uv/ut	Peak Diode Recovery dv/dt		(Note 3)	50	V/IIS
D	Bower Dissipation	(T _C = 25°C)		39	W
P _D Power Dissipation	- Derate Above 25°C		0.31	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range			-55 to +150	°C
TL	Maximum Lead Temperature	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			°C
Drain current lim	ited by maximum junction temperatu	re.	*		•

Thermal Characteristics

Symbol	Parameter	FCPF150N65F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. 62.5		- C/VV

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCPF150N65F	FCPF150N65F	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 25^{\circ}\text{C}$	650	-	-	V
	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 150^{\circ}\text{C}$	700	-	-	
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	-	0.72	-	V/°C
1	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	-	-	10	^
IDSS	Zero Gate voltage Drain Current	$V_{DS} = 520 \text{ V}, V_{GS} = 0 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	86	-	μΑ
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 2.4 \text{ mA}$	3	-	5	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}$	-	133	150	mΩ
9 _{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_{D} = 12 \text{ A}$	-	22	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 400 V V 0 V	-	2810	3737	pF
C _{oss}	Output Capacitance	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz		91	121	pF
C _{rss}	Reverse Transfer Capacitance			0.77	-	pF
C _{oss}	Output Capacitance	V _{DS} = 380 V, V _{GS} = 0 V, f = 1 MHz	-	54	-	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	-	361	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 380 V, I _D = 12 A,	-	72	94	nC
Q _{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	15	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	31	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	0.69	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time	V _{DD} = 380 V, I _D = 12 A,	-	28	66	ns
t _r	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, R_{q} = 4.7 \Omega$	-	15	40	ns
t _{d(off)}	Turn-Off Delay Time	Ŭ	-	73	156	ns
t _f	Turn-Off Fall Time	(Note 4)	-	6	22	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	24	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	72	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 12 A	-	-	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 12 A,	-	123	-	ns
Q _{rr}	Reverse Recovery Charge $dI_F/dt = 100 \text{ A/}\mu\text{s}$		-	597	-	nC

Notes:

- ${\it 1. Repetitive\ rating: pulse\ width\ limited\ by\ maximum\ junction\ temperature.}$
- 2. I_{AS} = 4.7 A, R_{G} = 25 Ω , Starting T_{J} = 25°C.
- 3. I $_{SD} \leq$ 12 A, di/dt \leq 200 A/µs, V $_{DD} \leq$ 380 V, Starting T $_{J}$ = 25°C.
- 4. Essentially independent of operating temperature.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

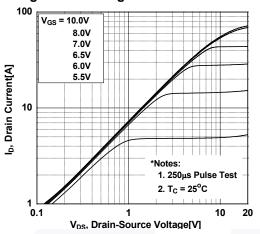


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

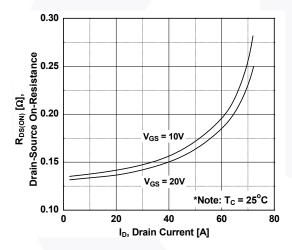


Figure 5. Capacitance Characteristics

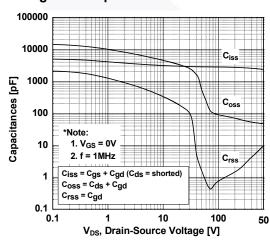


Figure 2. Transfer Characteristics

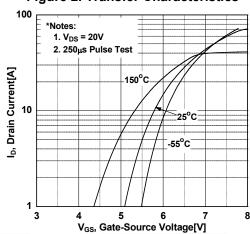


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

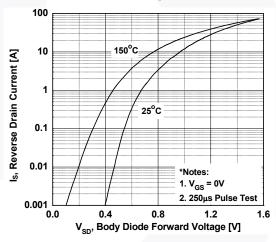
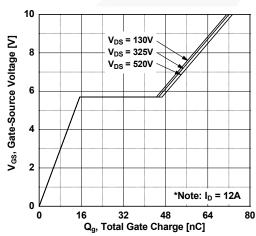


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

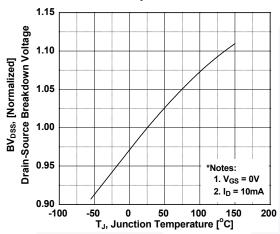


Figure 9. Maximum Safe Operating Area

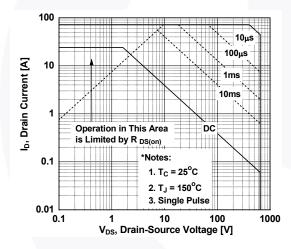


Figure 11. Eoss vs. Drain to Source Voltage

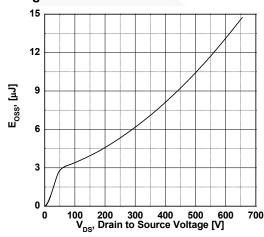


Figure 8. On-Resistance Variation vs. Temperature

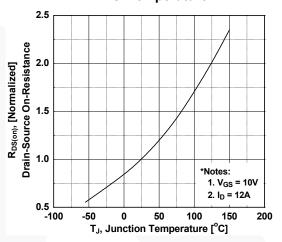
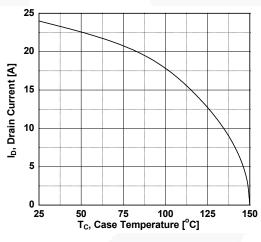
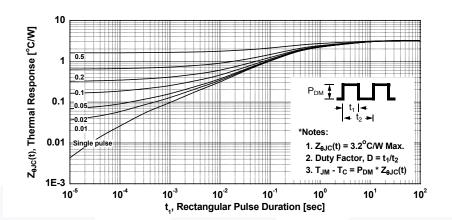


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



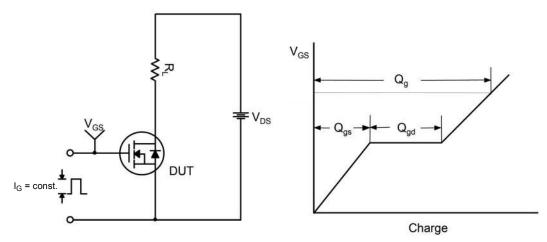


Figure 13. Gate Charge Test Circuit & Waveform

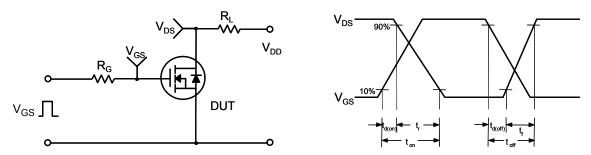


Figure 14. Resistive Switching Test Circuit & Waveforms

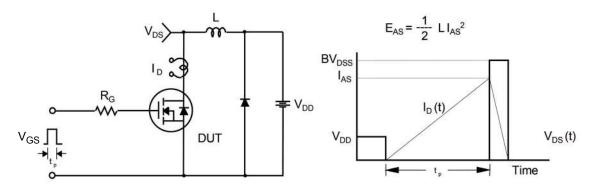
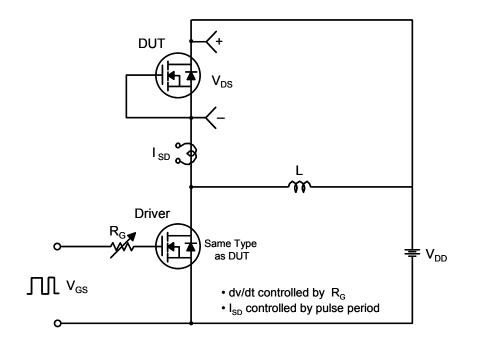


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms



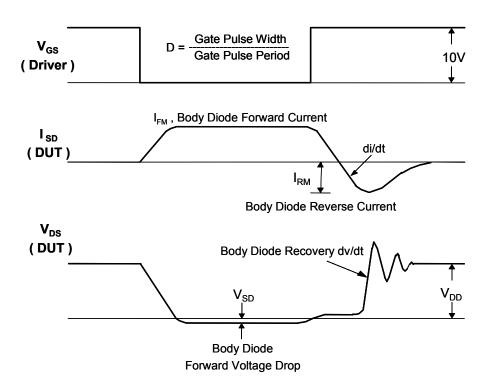
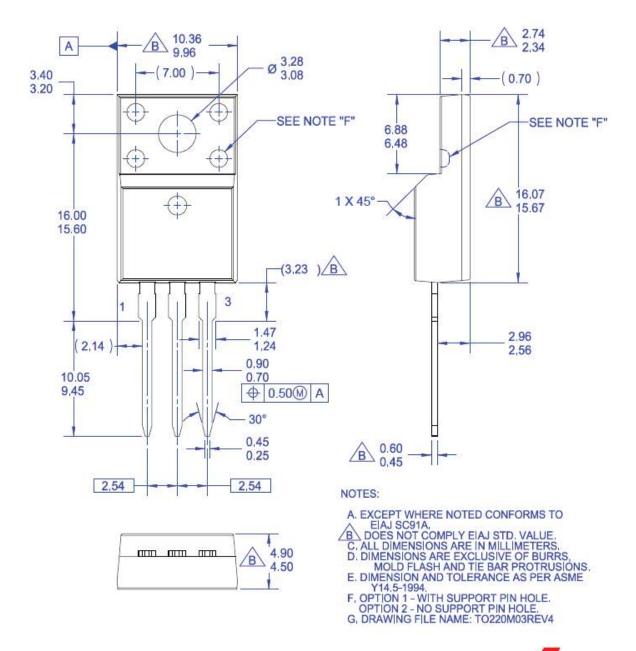


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions









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