3-Channel, Integrated Ultralow Power Solution with Dual Buck Regulators and Load Switch

Data Sheet

ADP5310

FEATURES

- Wide input voltage range: 2.7 V to 15.0 V
- 700 nA quiescent current when EN1 = SYNC/MODE = low
- ±1.5% output accuracy over full temperature range in PWM mode
- 600 kHz (or 1.2 MHz) switching frequency with optional synchronization input from 400 kHz to 1.4 MHz
- Channel 1: 800 mA buck regulator
  - Automatic PSM/PWM or forced PWM mode via factory fuse
  - 100% duty cycle operation mode
  - Adjustable/fixed output options via factory fuse
  - Power-good flag
- Channel 2: ultralow power buck regulator
  - Selectable hysteresis or PWM operation mode
  - Output current up to 50 mA in hysteresis mode, 300 mA in PWM mode with 100% duty cycle operation mode
  - Low noise at 0.8 V reference in PWM mode
  - Adjustable/fixed output voltage options via factory fuse
- Channel 3: high-side load switch
  - Low $R_{DS(ON)}$ of 494 mΩ at V_{OUT3} = 2.5 V
- Quick output discharge (QOD) option
- UVLO, OCP, and TSD protection
- 16-lead TSSOP_EP package
- −40°C to +125°C operational junction temperature

APPLICATIONS

- Energy (gas and water) metering
- Portable and battery-powered equipment
- Medical applications
- Keep-alive power supplies

TYPICAL APPLICATION CIRCUIT

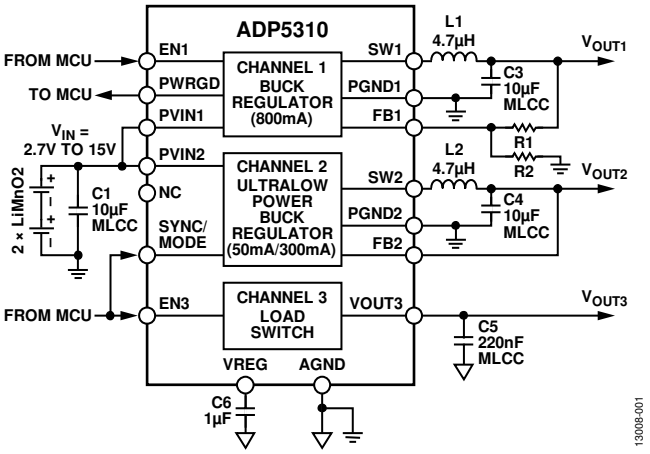

Figure 1.

GENERAL DESCRIPTION

The ADP5310 combines dual buck regulators and one load switch in a 16-lead TSSOP_EP package that meets demanding performance and board space requirements. The device enables direct connection to a wide input voltage range of 2.7 V to 15.0 V, allowing the use of multiple alkaline/NiMH or lithium cells and other power sources.

The buck regulator in Channel 1 uses a current mode, constant frequency pulse-width modulation (PWM) control scheme for excellent stability and transient performance, which provides up to 800 mA of output current. The automatic PWM/pulse skipping mode (PSM) control scheme achieves excellent efficiency in light output current. A power-good signal indicates that the output of Channel 1 is within 92% of its nominal value.

An ultralow power buck regulator is integrated in Channel 2 with the SYNC/MODE pin to control its operation mode. When SYNC/MODE is set to low, the buck regulator operates in hysteresis mode, which draws only 700 nA of quiescent current to regulate the output under zero load and provides up to 50 mA of output current. Hysteresis mode helps achieve excellent efficiency at less than 1 mW and can work as a keep-alive power supply in a battery-powered system. When the SYNC/MODE pin is set to high, the buck regulator switches to a traditional constant frequency PWM control scheme to provide low output ripple for noise sensitive applications, and the buck regulator provides up to 300 mA of output current in PWM mode.

Channel 3 integrates a high-side load switch that operates from 1.65 V to 5.5 V with its input connected to the output of Channel 2. The load switch provides power domain isolation and extends battery operation time.

Other key safety features of the ADP5310 include overcurrent protection (OCP), thermal shutdown (TSD), and input undervoltage lockout (UVLO). The ADP5310 is rated for the −40°C to +125°C junction temperature range.

Rev. A Document Feedback

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REVISION HISTORY

11/2016—Rev. 0 to Rev. A

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4/2015—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAM

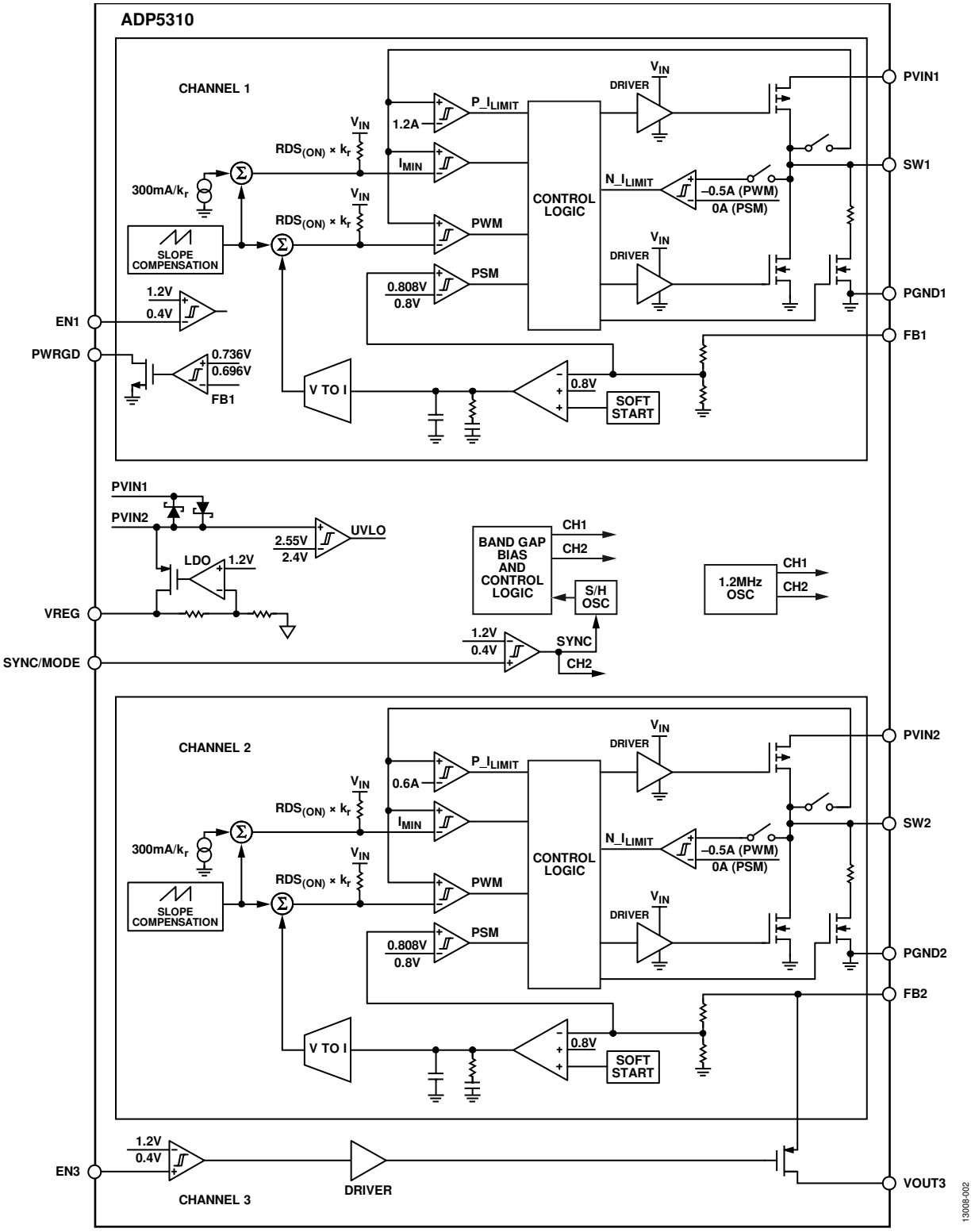

Figure 2.

SPECIFICATIONS

V_{IN} = 6 V, V_{REG} = 3.9 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SUPPLY VOLTAGE RANGE	V_{IN}	2.7		15.0	V	PVIN1 and PVIN2 pins
QUIESCENT CURRENT						PVIN1 and PVIN2 pins
Operating Quiescent Current						
Standby Operation	I_{Q1}		700	1850	nA	−40°C ≤ T_J ≤ +85°C, EN1 = SYNC/MODE = low
			700	3800	nA	−40°C ≤ T_J ≤ +125°C, EN1 = SYNC/MODE = low
PWM Operation	I_{Q3}		1.4	1.65	mA	EN1 = SYNC/MODE = high
UNDERVOLTAGE LOCKOUT	UVLO					PVIN2 pin
UVLO Threshold						
Rising	V_{UVLO_RISING}		2.55	2.75	V	
Falling	$V_{UVLO\_FALLING}$	2.15	2.40		V	
Hysteresis	V_{HYS}		150		mV	
OSCILLATOR CIRCUIT						For Channel 1 and Channel 2, PWM mode
Switching Frequency	f_{SW}	1050	1200	1350	kHz	
		525	600	675	kHz	
Feedback (FB) Threshold of Frequency Fold	V_{OSC_FOLD}		0.3		V	
SYNCHRONIZATION THRESHOLD						
SYNC Clock Range	$SYNC_{CLOCK}$	400		800	kHz	f_{SW} = 600 kHz
	$SYNC_{CLOCK}$	800		1400	kHz	f_{SW} = 1.2 MHz
SYNC High Level Threshold	$SYNC_{HIGH}$	1.2			V	
SYNC Low Level Threshold	$SYNC_{LOW}$			0.4	V	
SYNC Pulse On Time Range	$SYNC_{ON}$	80		$1/f_{SW}$ − 150	ns	
EN1 and EN3						
Input High Level Threshold	V_{IH}	1.2			V	
Input Low Level Threshold	V_{IL}			0.4	V	
Input Leakage Current	$I_{LEAKAGE}$			300	nA	
INTERNAL POWER GOOD						
Internal Power-Good Threshold	$V_{PWRGD(RISE)}$	88	92	96	%	
Internal Power-Good Hysteresis	$V_{PWRGD(HYS)}$		5		%	
Internal Power-Good Rising Delay	t_{PWRGD_RISE}		16		Clock cycles	
Internal Power-Good Falling Delay	t_{PWRGD_FALL}		1		µs	
Leakage Current for PWRGD Pin	$I_{PWRGD\_LEAKAGE}$		10	40	nA	
Output Low Voltage for PWRGD Pin	V_{PWRGD_LOW}		50	100	mV	I_{PWRGD} = 100 µA
INTERNAL REGULATOR						
VREG Output Voltage	V_{REG}	3.6	3.9	4.2	V	
THERMAL SHUTDOWN						
Threshold	T_{SHDN}		135		°C	
Hysteresis	T_{HYS}		15		°C	

BUCK REGULATORS AND LOAD SWITCH SPECIFICATIONS

V_{IN} = 6 V, V_{REG} = 3.9 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 1 SYNC BUCK REGULATOR						
Supply Voltage Range	V_{IN1}	2.7		15.0	V	PVIN1 pin
Rating Output Current	I_{OUT}		800		mA	
FB1 Pin in PWM Mode						
Fixed Output Options	V_{OUT1_FIX}	1.2		5.0	V	Factory trim, 3 bits (adjustable, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 2.85 V, 3.3 V, 5.0 V)
Fixed Output Accuracy	V_{FB1_FIX}	−1.5		+1.5	%	
Adjustable Output Voltage Range	V_{OUT1_ADJ}	0.8		PVIN1	V	Adjustable voltage option
Adjustable Feedback Voltage	V_{FB1}		0.800		V	Adjustable voltage option
Adjustable Feedback Voltage Accuracy	V_{FB1_ADJ}	−0.55		+0.55	%	T_J = 25°C
		−1.2		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
FB1 Pin in PSM Mode						
Threshold Accuracy from Active Mode to Skip Mode	V_{FB1_PSM}	−1.5		+1.5	%	
Hysteresis of Threshold Accuracy from Active Mode to Skip Mode	$V_{FB1\_PSM(PSM)}$		1		%	
Feedback Bias Current	I_{FB1}			0.1	µA	Adjustable voltage option
SW1 Pin						
High-Side Power FET On Resistance	$R_{DS(ON)1H}$		472	690	mΩ	Pin to pin measurement
Low-Side Power FET On Resistance	$R_{DS(ON)1L}$		438	725	mΩ	Pin to pin measurement
Current-Limit Threshold	$I_{TH(ILIM1)}$	1000	1260	1450	mA	
Minimum On Time	t_{MIN_ON1}		38	70	ns	
Soft Start Time	t_{SS1}		350		µs	Factory trim, 1 bit (350 µs, 2800 µs)
C_{OUT} Discharge Switch On Resistance	R_{DIS1}		287		Ω	
CHANNEL 2 SYNC BUCK REGULATOR						
Supply Voltage Range	V_{IN2}	2.7		15.0	V	PVIN2 pin
Rating Output Current						
Hysteresis Mode	I_{OUT_HYS}		50		mA	
PWM Mode	I_{OUT_PWM}		300		mA	
Mode Transition						
Transition Delay from Hysteresis Mode to PWM Mode	$T_{HYS\_TO\_PWM}$		8		Clock cycles	SYNC/MODE goes logic high from logic low
FB2 Pin in PWM Mode						
Fixed Output Options	V_{OUT2_FIX}	1.2		5.0	V	Factory trim, 8 bits (adjustable, 1.2 V to 3.6 V in 50 mV steps, and 3.6 V to 5.0 V in 100 mV steps)
Fixed Output Accuracy	V_{FB2_FIX}	−1.5		+1.5	%	
Adjustable Output Voltage Range	V_{OUT2_ADJ}	0.8		PVIN2	V	Adjustable voltage option (note that Channel 3 has no use in this setting)
Adjustable Feedback Voltage	V_{FB2}		0.800		V	Adjustable voltage option

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Adjustable Feedback Voltage Accuracy	V_{FB2_ADJ}	−0.55		+0.55	%	T_J = 25°C
		−1.2		+1.0	%	0°C ≤ T_J ≤ 85°C
		−1.5		+1.5	%	−40°C ≤ T_J ≤ +125°C
Feedback Bias Current	I_{FB2_ADJ}		15	200	nA	Adjustable voltage option
Feedback Resistor to GND	I_{FB2_FIX}		57		MΩ	Fixed voltage option
FB2 Pin in Hysteresis Mode						
Threshold Accuracy from Active Mode to Standby Mode	V_{FB2_HYS}	−1.5		+1.5	%	
Hysteresis of Threshold Accuracy from Active Mode to Standby Mode	$V_{FB2\_HYS(HYS)}$		1		%	
SW2 Pin						
High-Side Power FET On Resistance	$R_{DS(ON)2H}$		868	1250	mΩ	Pin to pin measurement
Low-Side Power FET On Resistance	$R_{DS(ON)2L}$		893	1360	mΩ	Pin to pin measurement
Current-Limit Threshold in PWM Mode	$I_{TH(ILIM2)}$	450	600	730	mA	SYNC/MODE = high
Peak Inductor Current in Hysteresis Mode	I_{L2}		300		mA	SYNC/MODE = low
Minimum On Time	t_{MIN_ON2}		36	70	ns	
Soft Start Time	t_{SS2}		350		µs	Factory trim, 1 bit (350 µs, 2800 µs)
C_{OUT} Discharge Switch On Resistance	R_{DIS2}		282		Ω	
CHANNEL 3 LOAD SWTICH						
Supply Voltage Range	V_{IN3}	1.65		5.5	V	FB2 pin
FB2 to VOUT3 On Resistance	$R_{DS(ON)3}$		382	550	mΩ	V_{OUT3} = 5.0 V, I_{LOAD3} = 50 mA
			430	615	mΩ	V_{OUT3} = 3.3 V, I_{LOAD3} = 50 mA
			494	700	mΩ	V_{OUT3} = 2.5 V, I_{LOAD3} = 50 mA
VOUT3 TIME						
Turn On Rise Time	t_{RISE3}		12	16	µs	V_{OUT3} = 2.5 V, C_{LOAD3} = 1 µF, factory trim, 2 bits (3 µs, 12 µs, 48 µs, 192 µs)
C_{OUT} Discharge Switch On Resistance	R_{DIS3}		286		Ω	

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
PVIN1, PVIN2 to PGNDx	−0.3 V to +17 V
SW1, SW2 to PGNDx	−0.3 V to PVIN + 0.3 V
VREG to PGNDx	−0.3 V to +6 V
EN1, EN3, SYNC/MODE, PWRGD to AGND	−0.3 V to +17 V
FB1, FB2 to AGND	−0.3 V to +6 V
VOUT3 to PGNDx	−0.3 V to +6 V
PGND1, PGND2 to AGND	−0.3 V to +0.3 V
Storage Temperate Range	−65°C to +150°C
Operational Junction Temperature Range	−40°C to +125°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead TSSOP_EP	39.14	2.59	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

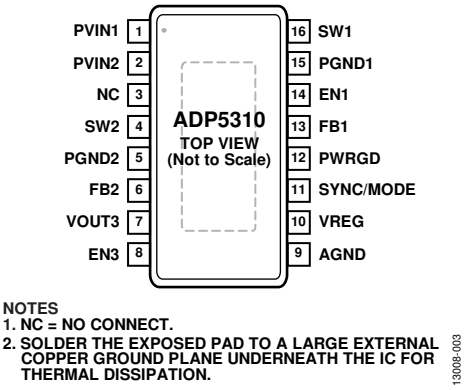

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PVIN1	Power Input of Channel 1. This pin must be connected to PVIN2.
2	PVIN2	Power Input of Channel 2 and Internal Linear Regulator.
3	NC	No Connect. This pin is not internally connected. Leave this pin floating.
4	SW2	Switching Node Output of Channel 2.
5	PGND2	Power Ground of Channel 2.
6	FB2	Feedback Sensing Input of Channel 2.
7	VOUT3	Power Output of Channel 3.
8	EN3	Enable Input of Channel 3.
9	AGND	Analog Ground.
10	VREG	Output of the Internal Linear Regulator. Connect a 1.0 µF ceramic capacitor between this pin and ground.
11	SYNC/MODE	Synchronization Input Pin (SYNC). To synchronize the switching frequency of the device to an external clock, connect this pin to an external clock with a frequency from 400 kHz to 1.4 MHz. PWM or Hysteresis Mode Selection Pin of Channel 2 (MODE). When this pin is logic high, the regulator operates in PWM mode. When this pin is logic low, the regulator operates in hysteresis mode.
12	PWRGD	Power-Good Signal Output. This open-drain output is the power-good signal of Channel 1.
13	FB1	Feedback Sensing Input of Channel 1.
14	EN1	Enable Input of Channel 1.
15	PGND1	Power Ground of Channel 1.
16	SW1	Switching Node Output of Channel 1.
	EPAD	Exposed Pad. Solder the exposed pad to a large external copper ground plane underneath the IC for thermal dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 6 V, V_{OUT1} = 4 V, V_{OUT2} = 3 V, L1 = 4.7 µH, L2 = 6.8 µH, C_{IN} = C_{OUT} = 10 µF, f_{SW} = 1.2 MHz, T_A = 25°C, unless otherwise noted.

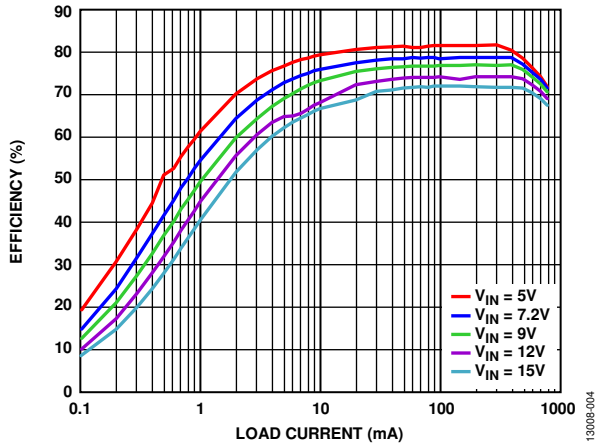

Figure 4. Channel 1 Auto PSM/PWM Efficiency vs. Load Current, V_{OUT1} = 1.2 V

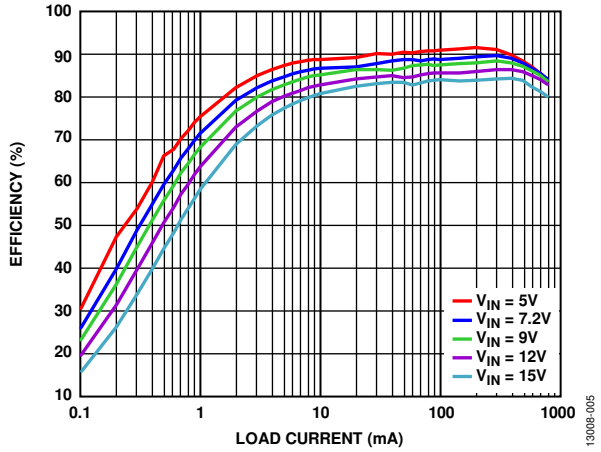

Figure 5. Channel 1 Auto PSM/PWM Efficiency vs. Load Current, V_{OUT1} = 2.5 V

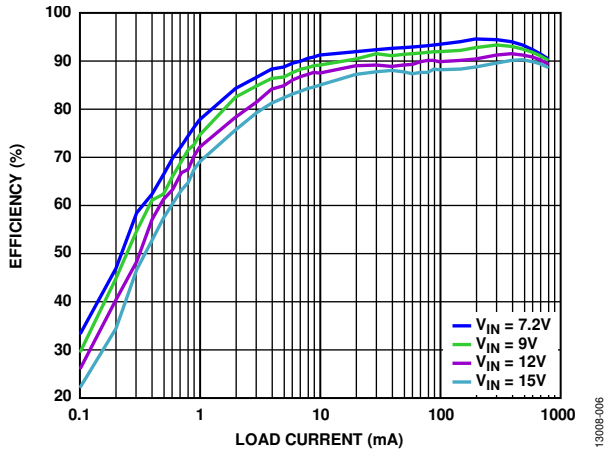

Figure 6. Channel 1 Auto PSM/PWM Efficiency vs. Load Current, V_{OUT1} = 5 V

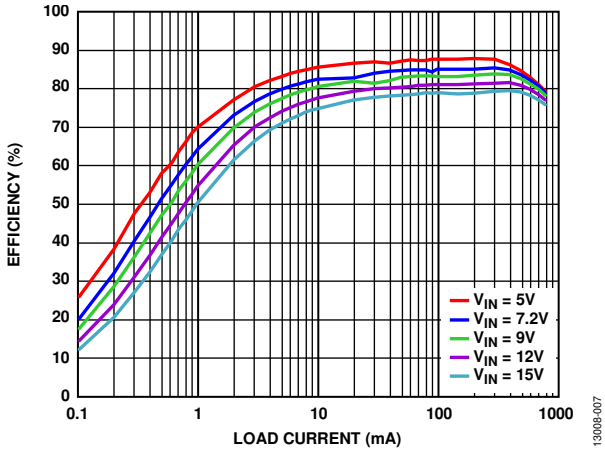

Figure 7. Channel 1 Auto PSM/PWM Efficiency vs. Load Current, V_{OUT1} = 1.8 V

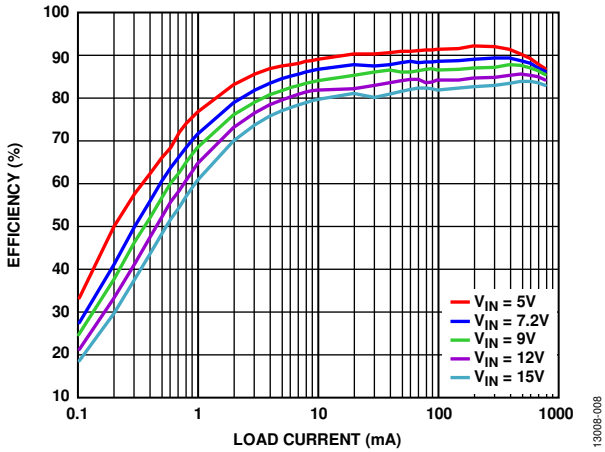

Figure 8. Channel 1 Auto PSM/PWM Efficiency vs. Load Current, V_{OUT1} = 3.3 V

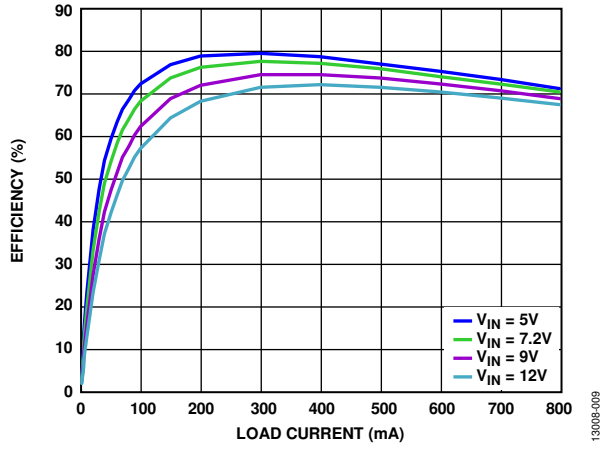

Figure 9. Channel 1 PWM Efficiency vs. Load Current, V_{OUT1} = 1.2 V

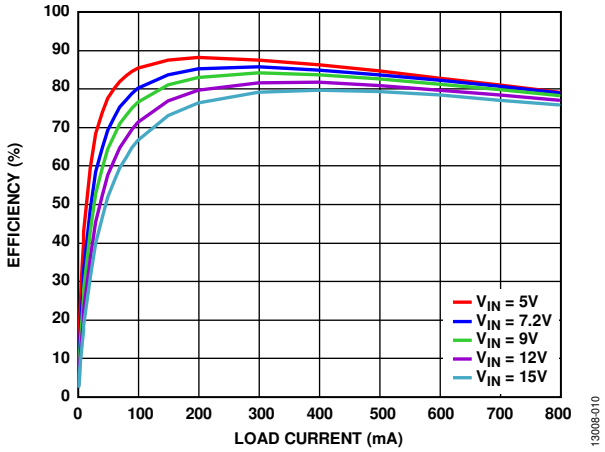

Figure 10. Channel 1 PWM Efficiency vs. Load Current, V_{OUT1} = 1.8 V

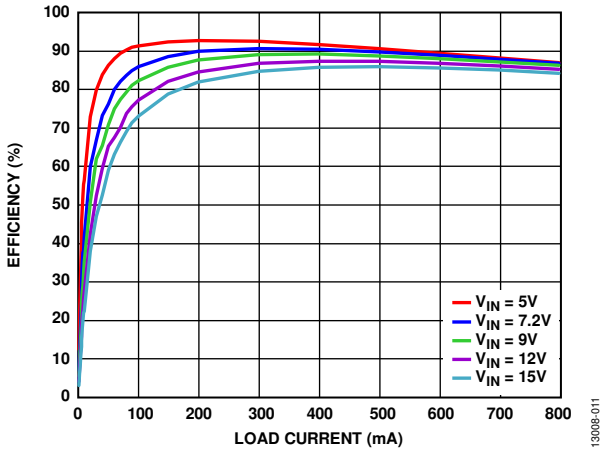

Figure 11. Channel 1 PWM Efficiency vs. Load Current, V_{OUT1} = 3.3 V

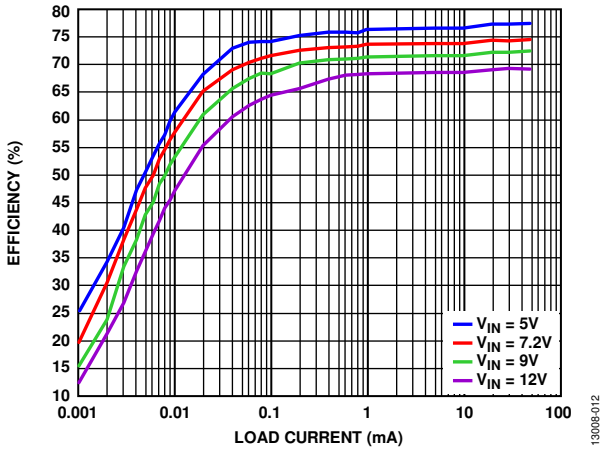

Figure 12. Channel 2 Hysteresis Efficiency vs. Load Current, V_{OUT2} = 1.2 V

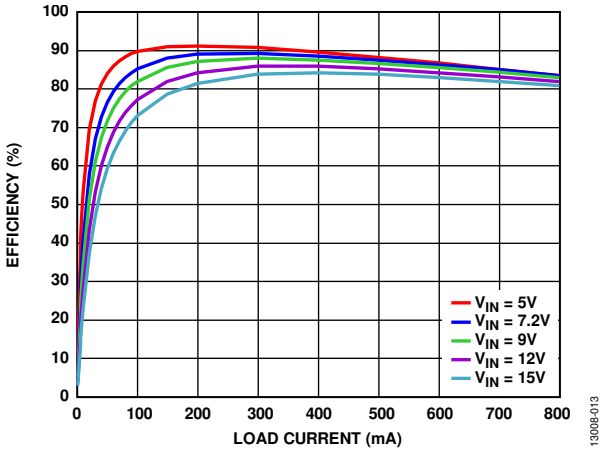

Figure 13. Channel 1 PWM Efficiency vs. Load Current, V_{OUT1} = 2.5 V

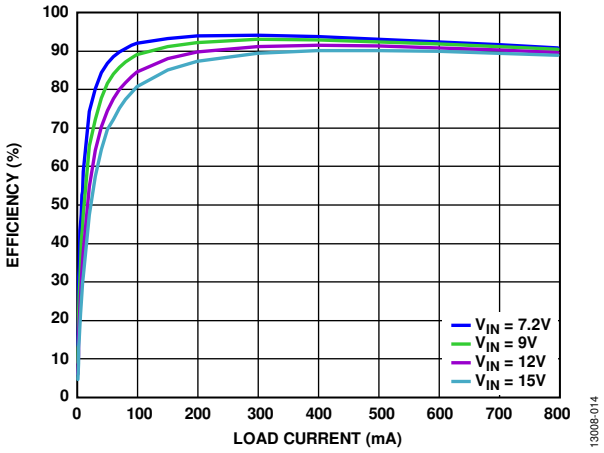

Figure 14. Channel 1 PWM Efficiency vs. Load Current, V_{OUT1} = 5 V

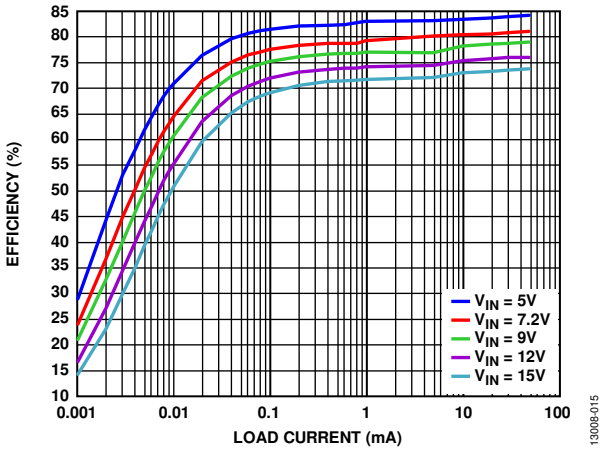

Figure 15. Channel 2 Hysteresis Efficiency vs. Load Current, V_{OUT2} = 1.8 V

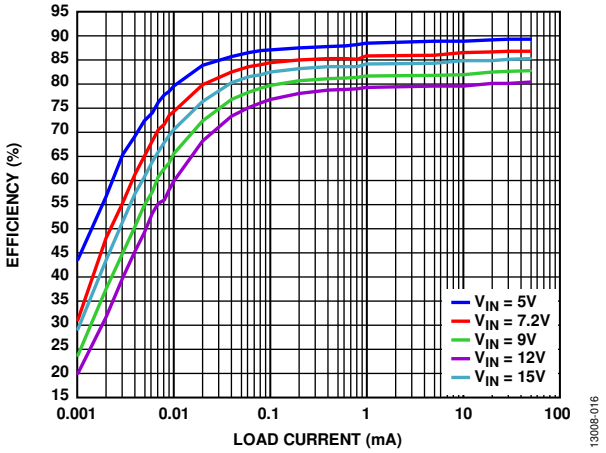

Figure 16. Channel 2 Hysteresis Efficiency vs. Load Current, V_{OUT2} = 2.5 V

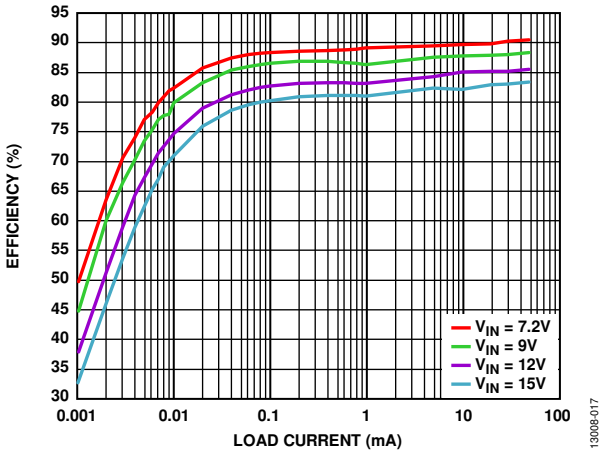

Figure 17. Channel 2 Hysteresis Efficiency vs. Load Current, V_{OUT2} = 5 V

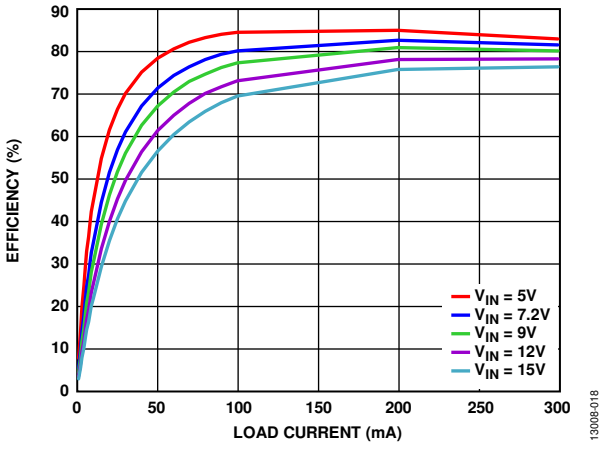

Figure 18. Channel 2 PWM Efficiency vs. Load Current, V_{OUT2} = 1.8 V

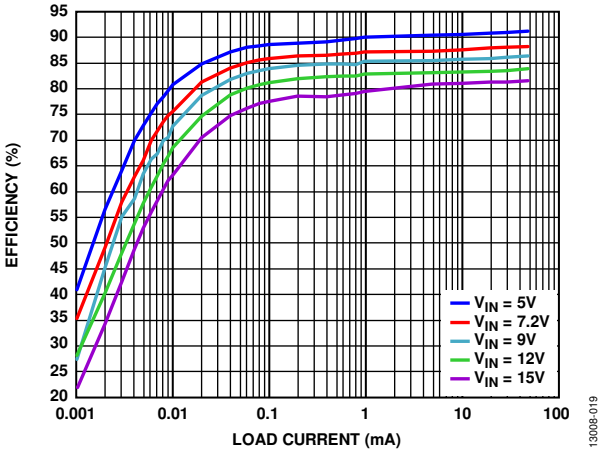

Figure 19. Channel 2 Hysteresis Efficiency vs. Load Current, V_{OUT2} = 3.3 V

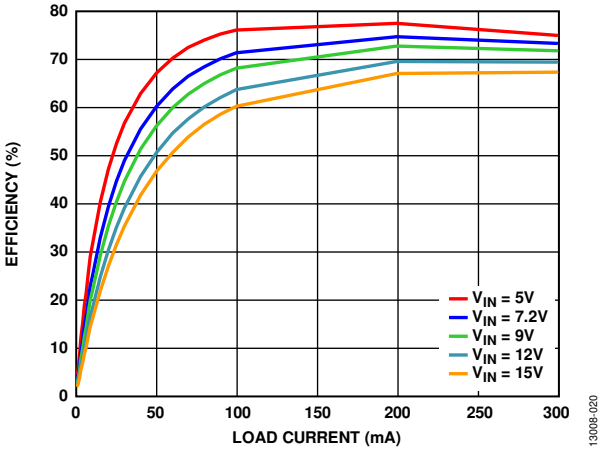

Figure 20. Channel 2 PWM Efficiency vs. Load Current, V_{OUT2} = 1.2 V

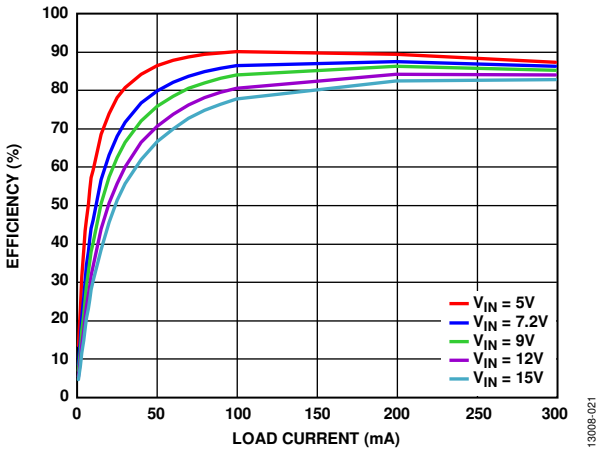

Figure 21. Channel 2 PWM Efficiency vs. Load Current, V_{OUT2} = 2.5 V

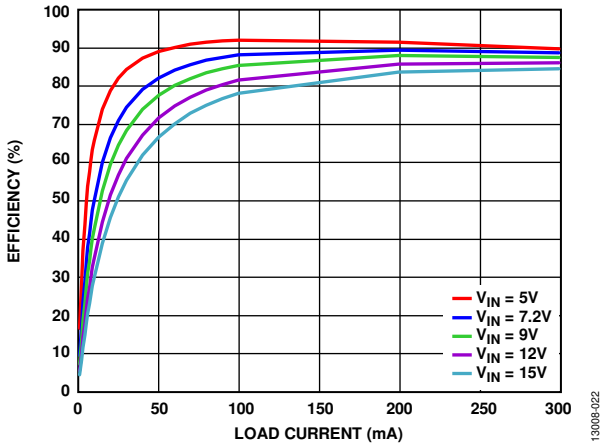

Figure 22. Channel 2 PWM Efficiency vs. Load Current, V_{OUT2} = 3.3 V

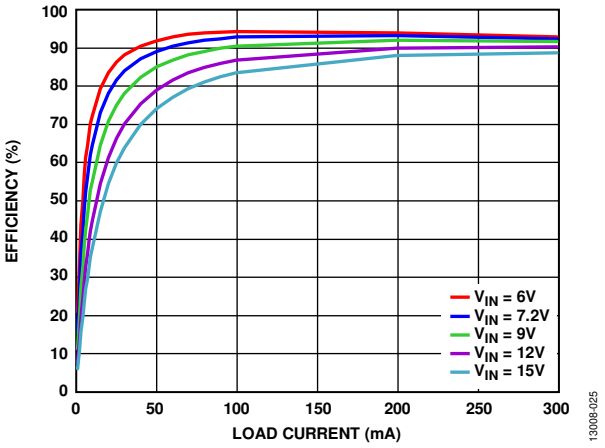

Figure 25. Channel 2 PWM Efficiency vs. Load Current, V_{OUT2} = 5 V

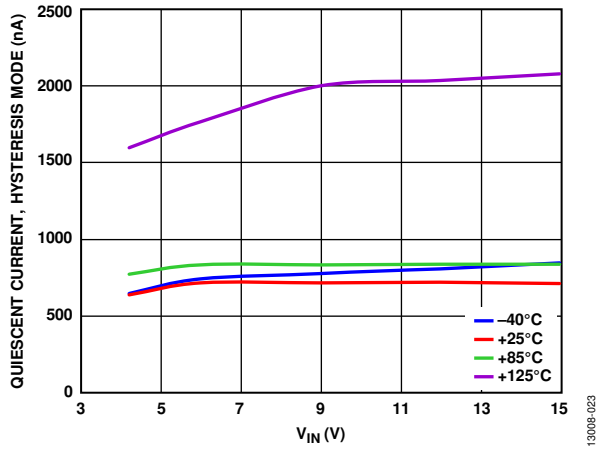

Figure 23. Quiescent Current, Hysteresis Mode vs. V_{IN}, EN1 = SYNC/MODE = Low

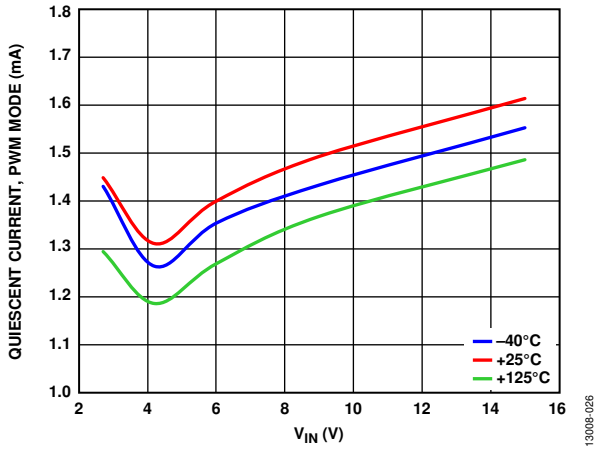

Figure 26. Quiescent Current, PWM Mode, EN1 = SYNC/MODE = High

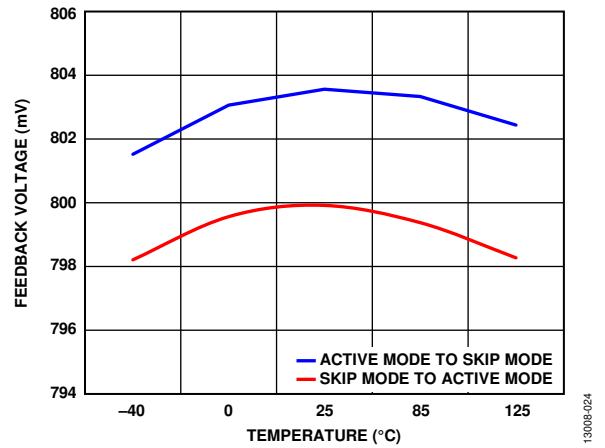

Figure 24. Channel 1 Feedback Voltage of PSM Mode vs. Temperature

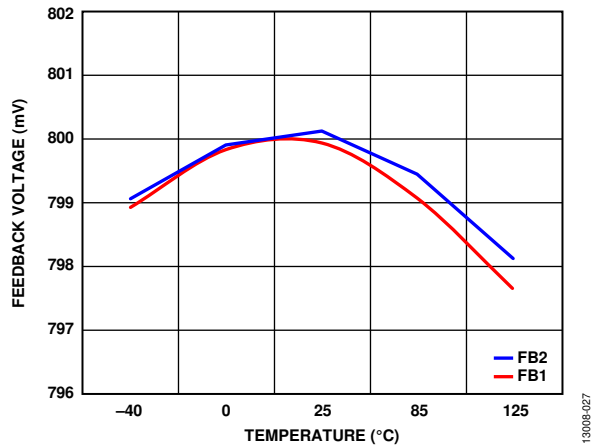

Figure 27. Channel 2 Feedback Voltage of PWM Mode vs. Temperature

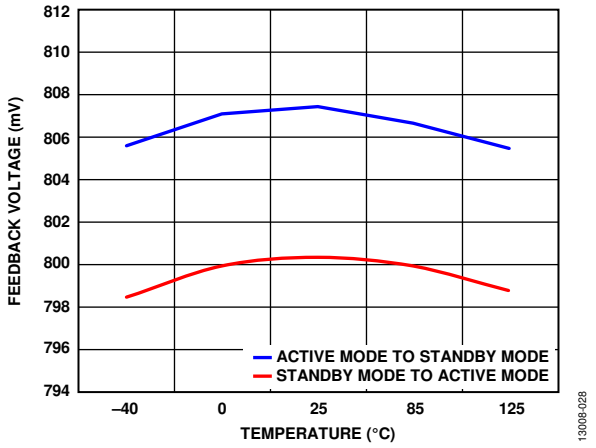

Figure 28. Channel 2 Feedback Voltage of Hysteresis Mode vs. Temperature

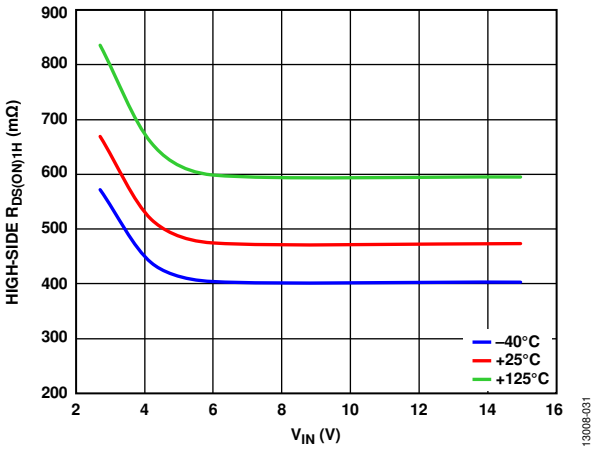

Figure 31. Channel 1 High-Side $R_{DS(ON)1H}$ vs. V_{IN}

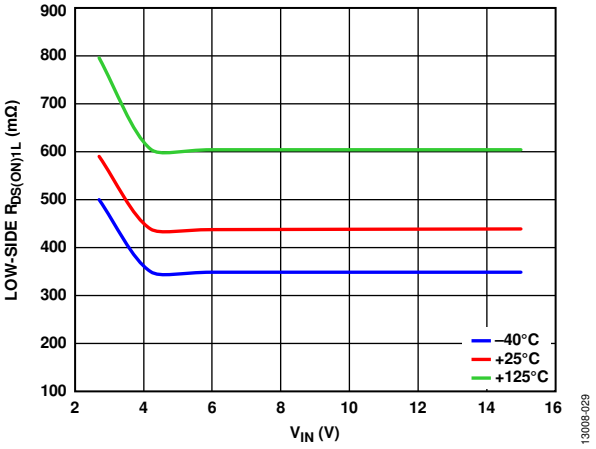

Figure 29. Channel 1 Low-Side $R_{DS(ON)1L}$ vs. V_{IN}

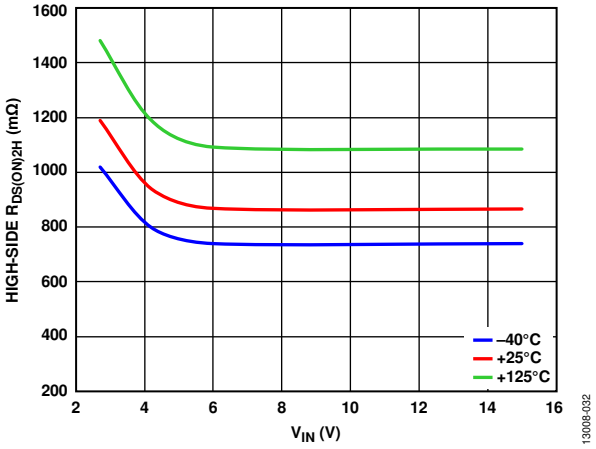

Figure 32. Channel 2 High-Side $R_{DS(ON)2H}$ vs. V_{IN}

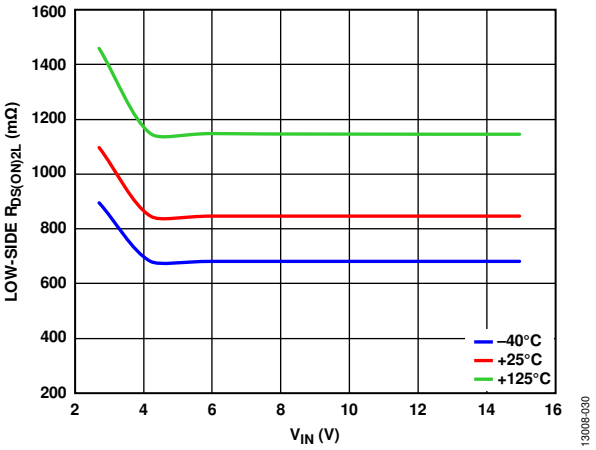

Figure 30. Channel 2 Low-Side $R_{DS(ON)2L}$ vs. V_{IN}

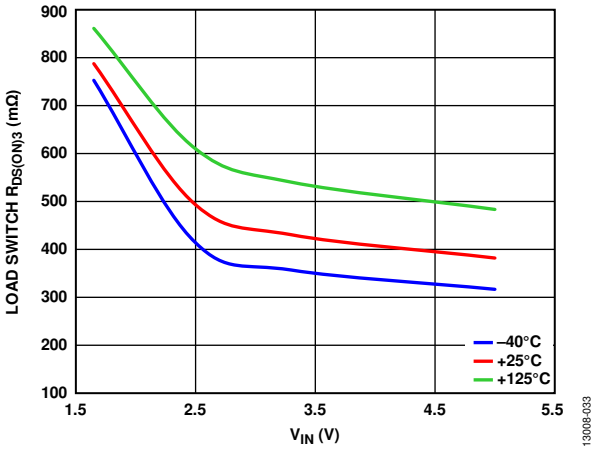

Figure 33. Channel 3 Load Switch $R_{DS(ON)3}$ vs. V_{IN}

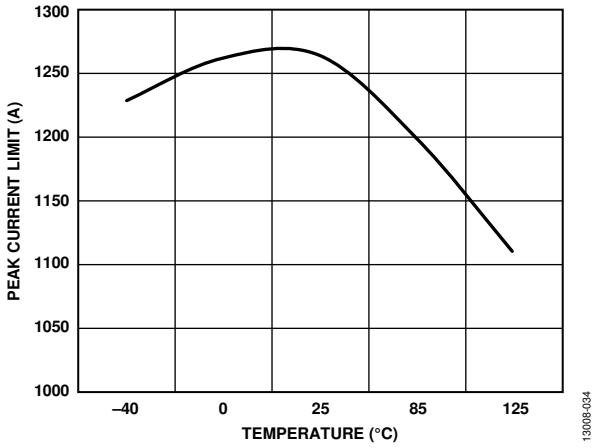

Figure 34. Channel 1 Peak Current Limit vs. Temperature

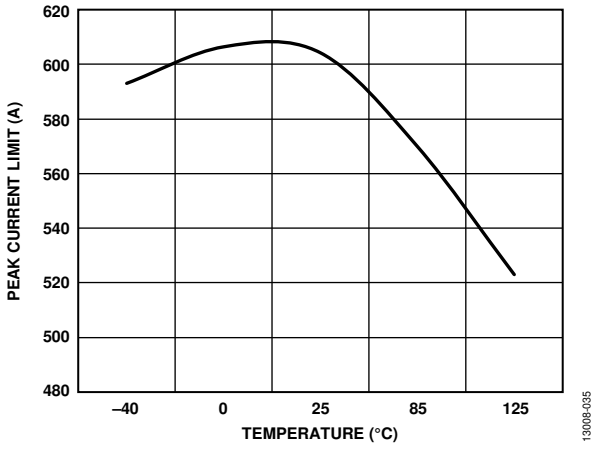

Figure 35. Channel 2 Peak Current Limit vs. Temperature

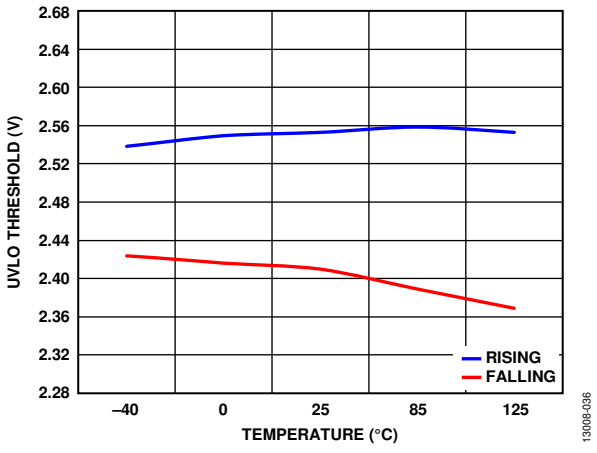

Figure 36. UVLO Threshold, Rising and Falling, vs. Temperature

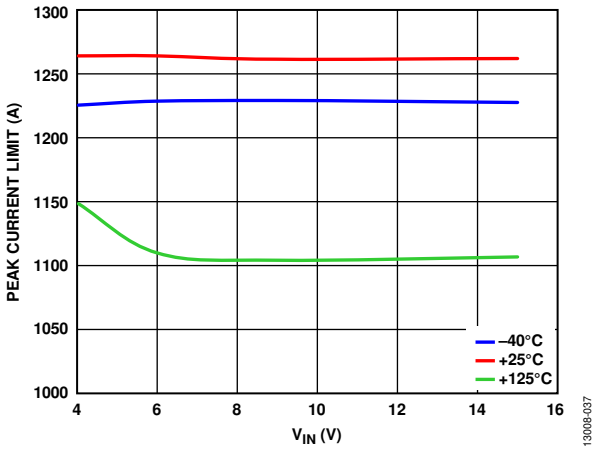

Figure 37. Channel 1 Peak Current Limit vs. V_{IN}

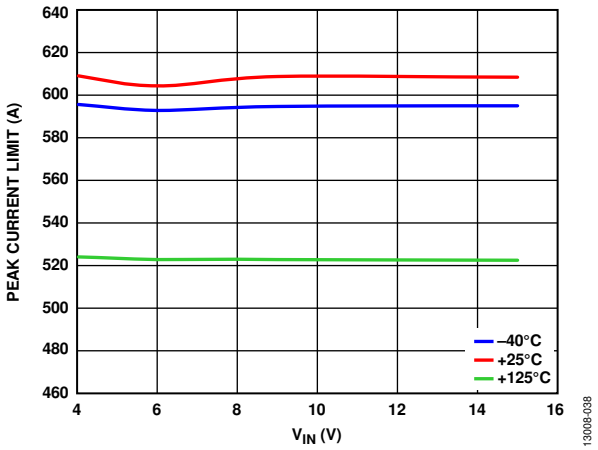

Figure 38. Channel 2 Peak Current Limit vs. V_{IN}

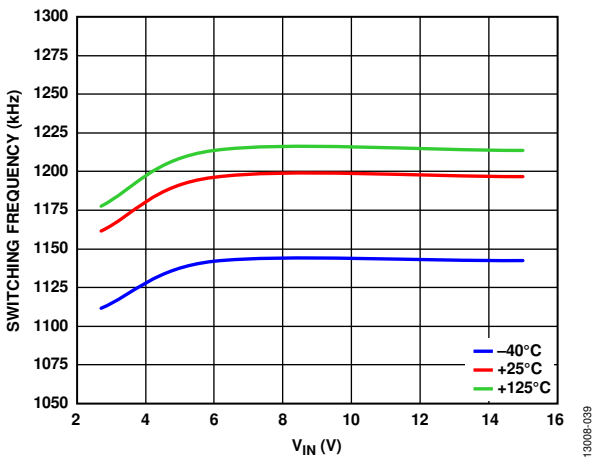

Figure 39. Switching Frequency vs. V_{IN}

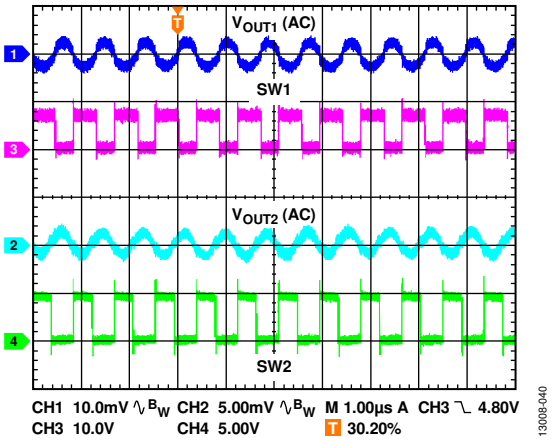

Figure 40. Steady Waveform of PWM Mode

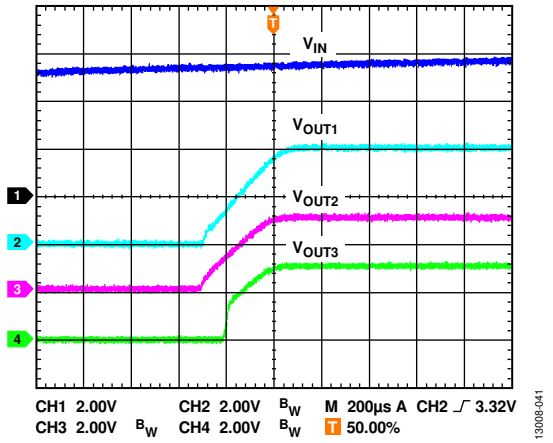

Figure 41. Soft Start Waveform

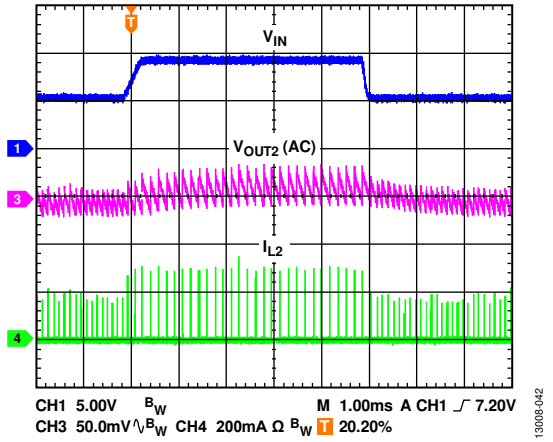

Figure 42. Channel 2 Line Transient in Hysteresis Mode

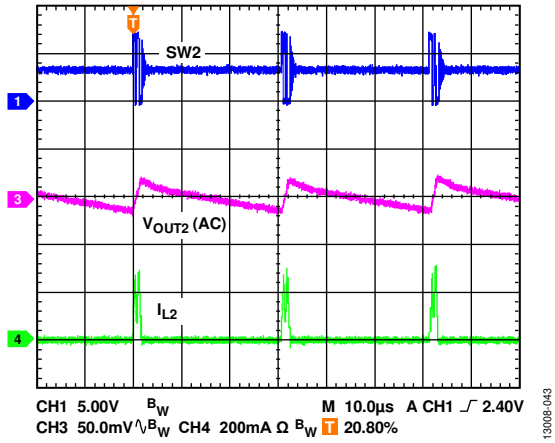

Figure 43. Channel 2 Output Ripple of Hysteresis Mode

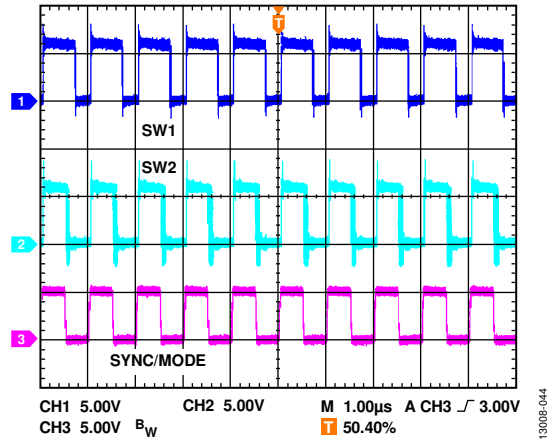

Figure 44. Synchronization to 1 MHz

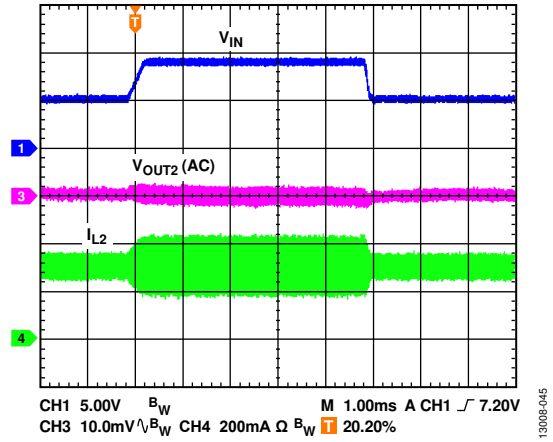

Figure 45. Channel 2 Line Transient in PWM Mode

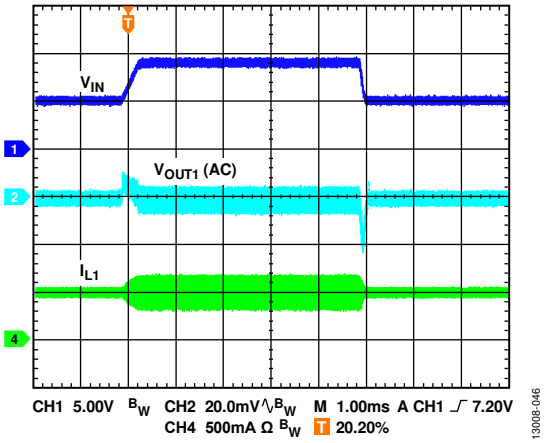

Figure 46. Channel 1 Line Transient in PWM Mode

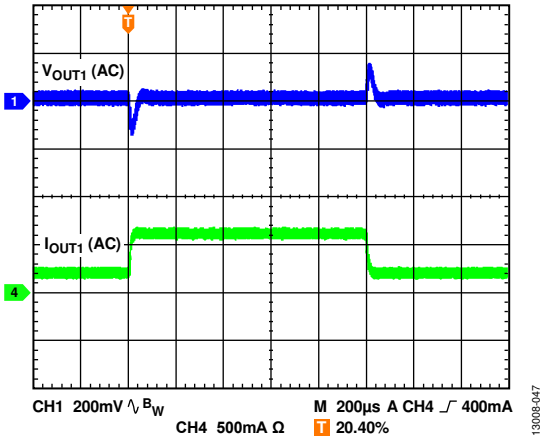

Figure 47. Channel 1 Load Transient (0.2 A to 0.6 A Load Step)

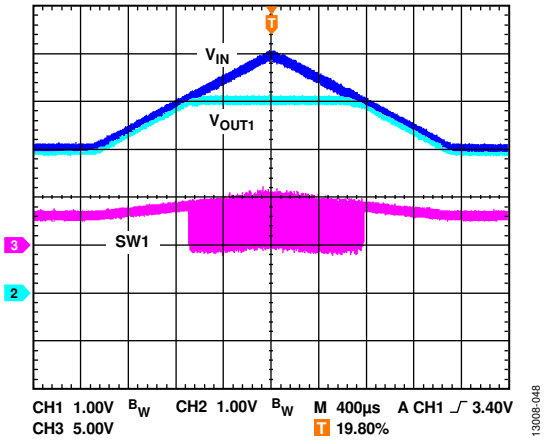

Figure 48. Channel 1 100% Duty Operation in PWM Mode

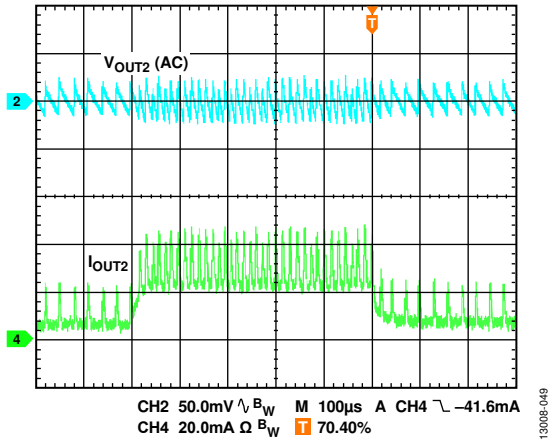

Figure 49. Channel 2 Hysteresis Mode Load Transient (10 mA to 30 mA Load Step)

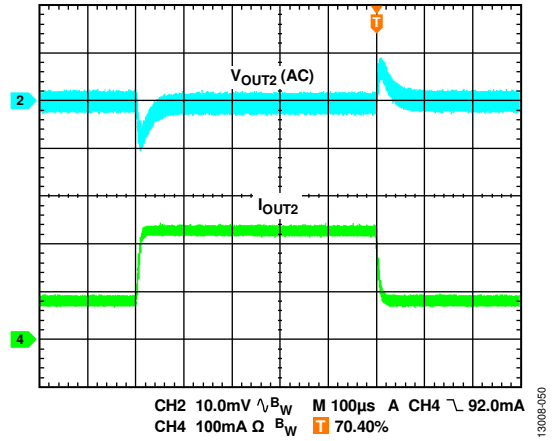

Figure 50. Channel 2 PWM Mode Load Transient (75 mA to 225 mA Load Step)

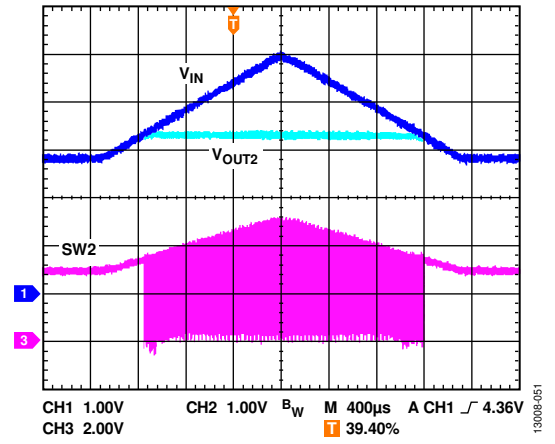

Figure 51. Channel 2 100% Duty Operation in PWM Mode

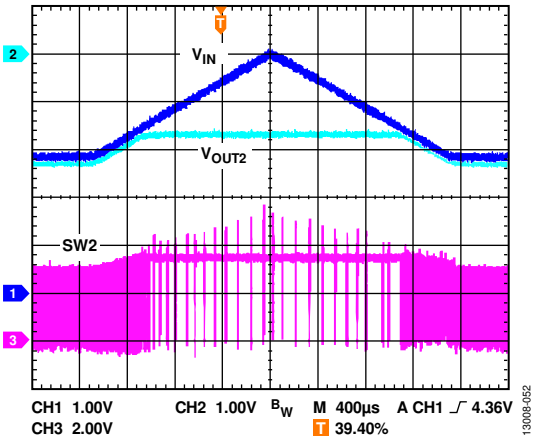

Figure 52. Channel 2 100% Duty Operation in Hysteresis Mode

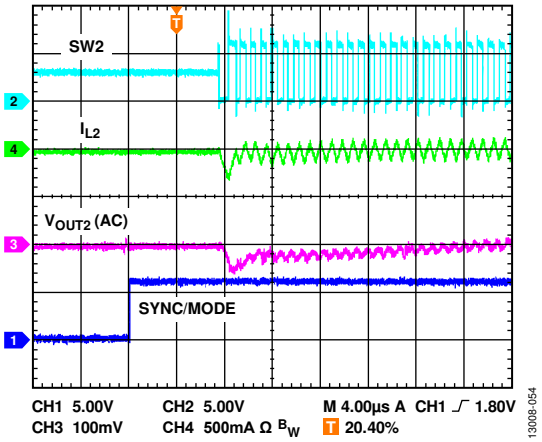

Figure 54. Mode Transition from Hysteresis Mode to PWM Mode

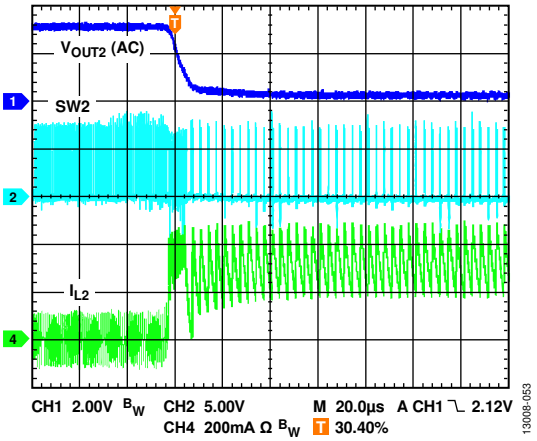

Figure 53. Output Short

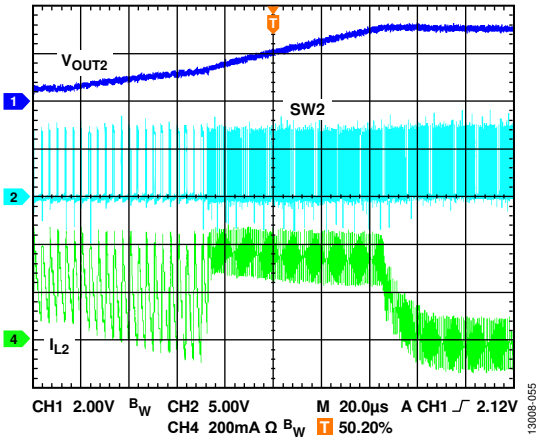

Figure 55. Output Short Recovery

THEORY OF OPERATION

The ADP5310 is an ultralow power management unit that combines dual buck regulators and one load switch in a 16-lead TSSOP_EP package to meet demanding performance and board space requirements. The device enables direct connection to the wide input voltage range of 2.7 V to 15 V, allowing the use of multiple alkaline/NiMH or lithium cells and other power sources.

BUCK REGULATOR OPERATION MODES

PWM Mode

In PWM mode, the buck regulators in the ADP5310 operate at a fixed frequency that is set by an internal oscillator. At the start of each oscillator cycle, the high-side MOSFET switch turns on and sends a positive voltage across the inductor. The inductor current increases until the current sense signal exceeds the peak current threshold of the inductor that turns off the high-side MOSFET switch and turns on the low-side MOSFET. This places a negative voltage across the inductor, causing the inductor current to reduce. The low-side MOSFET stays on for the remainder of the cycle.

PSM Mode

The ADP5310 smoothly transitions to the variable frequency PSM mode of operation when the load current decreases below the pulse skipping threshold current, I_{MIN}. For the peak current of the inductor based on the input and output voltages, the design of the I_{MIN} value is based on the recommended inductor values. Deviating from the recommended inductor value for a particular output voltage results in shifting the PSM to PWM threshold and may result in the device entering discontinuous mode (DCM).

As long as the required peak inductor current is above I_{MIN}, the regulator remains in PWM mode. As the load decreases, the PSM circuitry prevents the peak inductor current from dropping below the PSM peak current value. This circuitry causes the regulator to supply more current to the output than the load requires, resulting in the output voltage increasing and the output of the internal compensation node of the error amplifier, V_{COMP}, decreasing.

When the FB1 pin voltage rises above 1% of the nominal output voltage and the V_{COMP} node voltage is below a predetermined PSM threshold voltage level, the regulator enters skip mode. While in skip mode, the high-side and low-side switches and a majority of the circuitry are disabled to allow a low skip mode quiescent current as well as high efficiency performance.

During skip mode, the output voltage decreases as the output capacitor discharges into the load. Fixed frequency operation starts when the FB1 voltage reaches the nominal output voltage. When the load requirement increases past the I_{MIN} peak current level, the V_{COMP} node rises and the PWM control loop sets the duty cycle. While the device is entering and exiting skip mode, the PSM voltage ripple is larger than 1% because of the delay in the comparators.

Hysteresis Mode

In hysteresis mode, the buck regulator in the ADP5310 charges the output voltage slightly higher than its nominal output voltage with PWM pulses by regulating the constant peak inductor current. When the output voltage increases until the output sense signal exceeds the hysteresis upper threshold, the regulator enters standby mode. In standby mode, the high-side and low-side MOSFET and a majority of the circuitry are disabled to allow a low quiescent current as well as high efficiency performance.

During standby mode, the output capacitor supplies the energy into the load and the output voltage decreases until it falls below the hysteresis comparator lower threshold. The buck regulator wakes up and generates the PWM pulses to charge the output again.

Because the output voltage occasionally enters standby mode and then recovers, the output voltage ripple in hysteresis mode is larger than the ripple in PWM mode.

Mode Selection

The buck regulator in Channel 1 uses the default automatic PSM/PWM mode for excellent light load efficiency. Current mode, constant frequency PWM mode can be programmed by the factory fuse for excellent stability and transient performance.

The buck regulator in Channel 2 includes the SYNC/MODE pin, allowing configuration in hysteresis mode or PWM mode.

When a logic high level is applied to the SYNC/MODE pin, the buck regulator in Channel 2 is forced to operate in PWM mode. In PWM mode, the regulator can supply up to 300 mA of output current. The regulator can provide lower output ripple and lower 1/f output noise in PWM mode, which benefits noise sensitive applications.

When a logic low level is applied to the SYNC/MODE pin, the buck regulator in Channel 2 is forced to operate in hysteresis mode. In hysteresis mode, the regulator draws only 700 nA of quiescent current to regulate the output under zero load, which allows Channel 2 to act as a keep-alive power supply in a battery-powered system. In hysteresis mode, the regulator supplies up to 50 mA of output current with a relatively large output ripple compared to PWM mode.

The user can alternate between hysteresis mode and PWM mode during operation. The flexible configuration capability during operation of the device enables efficient power management to meet high efficiency and low output ripple requirements when the system switches between active mode and standby mode.

ADJUSTABLE AND FIXED OUTPUT VOLTAGES

The buck regulator in Channel 1 provides adjustable and fixed output voltage settings via the factory fuse. For the adjustable output settings, use an external resistor divider to set the desired output voltage via the feedback reference voltage (0.8 V for Channel 1).

The buck regulator in Channel 2 provides adjustable and fixed output voltage settings via the factory fuse as well. Because the input source of the load switch in Channel 3 shares the FB2 pin, the load switch in Channel 3 is unusable when Channel 2 is configured in adjustable output mode via the factory fuse.

UNDERVOLTAGE LOCKOUT (UVLO)

The UVLO circuitry monitors the input voltage level of the ADP5310 in the PVIN2 pin. When the input voltage falls below 2.40 V (typical), all channels turn off. After the input voltage rises above 2.55 V (typical), the soft start period is initiated, and the corresponding channel is enabled when the ENx pin is high.

ENABLE AND SHUTDOWN FEATURES

The ADP5310 uses the enable pins (EN1 and EN3) at logic levels to enable and disable Channel 1 and Channel 3. The associated channel begins operation with soft start when the enable pin is toggled from logic low to logic high. Pulling an enable pin low forces the associated channel into a shutdown condition.

The buck regulator in Channel 2 is always alive as long as the PVIN2 voltage is above the UVLO threshold.

INTERNAL LINEAR REGULATOR (VREG)

The internal linear VREG regulator in the ADP5310 provides a stable 3.9 V power supply for the bias voltage of the MOSFET drivers and internal control circuits. Connect a 1.0 µF ceramic capacitor between VREG and ground.

OSCILLATOR AND SYNCHRONIZATION

The ADP5310 ensures that both buck regulators operate at the same switching frequency when both buck regulators are in PWM mode.

The ADP5310 offers 600 kHz or 1.2 MHz switching frequency options in PWM operation mode via the factory fuse. The default switching frequency is 1.2 MHz.

The switching frequency of the ADP5310 can be synchronized to an external clock with a frequency range from 400 kHz to 1.4 MHz. The ADP5310 automatically detects the presence of an external clock applied to the SYNC/MODE pin, and the switching frequency transitions to the frequency of the external clock. When the external clock signal stops, the device automatically switches back to the internal clock and continues to operate.

CURRENT LIMIT

The buck regulators in the ADP5310 have protection circuitry that limit the direction and the amount of current to a certain level that flows through the high-side MOSFET and the low-side MOSFET in cycle-by-cycle mode. The positive current limit on the high-side MOSFET limits the amount of current that can flow from the input to the output. The negative current limit on the low-side MOSFET prevents the inductor current from reversing direction and flowing out of the load.

SHORT-CIRCUIT PROTECTION

The buck regulators in the ADP5310 include frequency foldback to prevent current runaway on a hard short. When the output voltage at the feedback pin falls below 0.3 V, indicating the possibility of a hard short at the output, the switching frequency (in PWM mode) is reduced to ¼ of the internal oscillator frequency. The reduction in the switching frequency allows more time for the inductor to discharge, preventing a runaway of output current.

SOFT START

The ADP5310 has an internal soft start function that ramps up the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the device. The default soft start time is 350 µs for the regulators in Channel 1 and Channel 2.

Different soft start times can be programmed for each channel by the factory fuse.

STARTUP WITH PRECHARGED OUTPUT

The buck regulators in the ADP5310 include a precharged start-up feature to protect the low-side FETs from damage during startup. If the output voltage is precharged before the regulator is turned on, the regulator prevents reverse inductor current, which discharges the output capacitor until the internal soft start reference voltage exceeds the precharged voltage on the feedback pin.

100% DUTY OPERATION

With a drop in input voltage or with an increase in load current, the buck regulator in the ADP5310 may reach a limit where, even with the high-side MOSFET on 100% of the time, the ADP5310 works in 100% duty operation and the output is lower than the preset value. At this limit, the buck regulator transitions to a mode where the high-side MOSFET switch stays on 100% of the time. When the input conditions charge again and the required duty cycle falls, the buck immediately restarts PWM regulation without allowing overshoot on the output voltage.

ACTIVE DISCHARGE

All channels in the ADP5310 integrate an optional, factory programmable, discharge switch from the switching node (or from the VOUT3 pin in the load switch) to ground. This switch turns on when its associated regulator is disabled, which helps discharge the output capacitor quickly. The typical value of the discharge switch is 282 Ω to 287 Ω for each channel.

By default, the discharge function is not enabled. The option to enable this active discharge function can be programmed for each channel by the factory fuse.

POWER-GOOD FUNCTION

The ADP5310 includes an open-drain, power-good output (PWRGD pin) that becomes active high when the buck regulator in Channel 1 is operating normally.

A logic high on the PWRGD pin indicates that the regulated output voltage of the buck regulator in Channel 1 is above 92% (typical) of its nominal output for a delay time greater than approximately 16 switching cycles (typical). When the regulated output voltage of the buck regulator in Channel 1 falls below 87% (typical) of its nominal output, the PWRGD pin goes low.

LOAD SWITCH

The ADP5310 integrates a high-side load switch that operates from 1.65 V to 5.5 V. The supply of the load switch is connected to the FB2 pin of Channel 2 internally, which provides the power domain isolation for the output of Channel 2 and helps extend battery operation time. The Channel 3 load switch has a low on resistance of 494 mΩ (typical) at V_{OUT3} = 2.5 V.

The inrush control circuitry (soft start) is included in the load switch as well. The default soft start time is 12 µs. Different soft start times can be programmed by the factory fuse.

Note that the load switch in Channel 3 is not usable when Channel 2 is configured as the adjustable output mode via the factory fuse.

THERMAL SHUTDOWN

If the ADP5310 junction temperature exceeds 135°C, the thermal shutdown circuit turns off the IC except for the internal linear regulator. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 15°C hysteresis is included so that the ADP5310 does not return to operation after thermal shutdown, until the on-chip temperature falls below 120°C. When the device exits thermal shutdown, a soft start is initiated for each enabled channel.

APPLICATIONS INFORMATION

This section describes the external components selection for the ADP5310. The typical application circuit is shown in Figure 56.

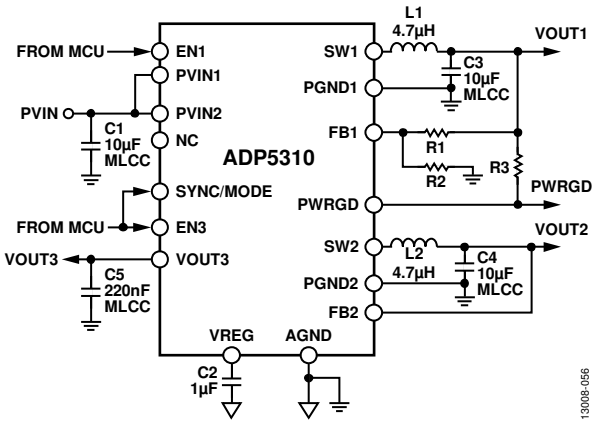

Figure 56. Typical Application Circuit

EXTERNAL COMPONENT SELECTION

Table 6, Table 7, and Table 8 list external component selections for the ADP5310 application circuit. The selection of components is dependent on the input voltage, output voltage, and load current requirements. Additionally, trade-offs among performance parameters, such as efficiency and transient response, are made by varying the choice of external components.

SELECTING THE INDUCTOR

The high frequency switching of the ADP5310 allows the use of small surface-mount power inductors. The inductor value affects the transition from PWM to PSM, efficiency, output ripple, and current limit values. Use the following equation to calculate the ideal inductance, which is derived from the inductor current slope compensation, for a given output voltage and switching frequency:

$$L = \frac{1.2 \times V_{OUT}}{k \times f_{SW}}$$

where:

L is the inductor value in µH.

V_{OUT} is the output voltage for Channel 1 and Channel 2 of the buck regulator.

k is 1.06 (Channel 1) or 0.478 (Channel 2).

f_{SW} is the switching frequency in MHz (1.2 MHz typical).

The ripple current is calculated as follows:

$$\Delta I_L = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The dc resistance (DCR) value of the selected inductor affects efficiency. A minimum requirement of the dc current rating of the inductor is for it to be equal to the maximum load current plus half of the inductor current ripple, as shown in the following equation:

$$I_{PK} = I_{LOAD(MAX)} + \left(\frac{\Delta I_L}{2}\right)$$

OUTPUT CAPACITOR

Output capacitance is required to minimize the voltage overshoot, voltage undershoot, and the ripple voltage present on the output. Capacitors with low equivalent series resistance (ESR) values produce the lowest output ripple; Furthermore, use capacitors such as the X5R and X7R dielectric. Do not use Y5V and Z5U capacitors. Y5V and Z5U capacitors are unsuitable choices because of their large capacitance variation over temperature and their dc bias voltage changes. Because ESR is important, select the capacitor using the following equation:

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{\Delta I_L}$$

where:

ESR_{COUT} is the ESR of the chosen capacitor.

V_{RIPPLE} is the peak-to-peak output voltage ripple.

Use the following equation to determine the output capacitance:

$$C_{OUT} \geq \frac{\Delta I_L}{8 \times f_{SW} \times V_{RIPPLE}}$$

Increasing the output capacitor value has no effect on stability and may reduce output ripple and enhance load transient response. When choosing the output capacitor value, it is important to account for the loss of capacitance due to output voltage dc bias.

INPUT CAPACITOR

An input capacitor is required to reduce input voltage ripple and source impedance. Place the input capacitor as close as possible to the PVINx pin. A low ESR X7R or X5R type capacitor is highly recommended to minimize the input voltage ripple. Use the following equation to determine the rms input current:

$$I_{RMS} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

ADJUSTABLE OUTPUT VOLTAGE PROGRAMMING

The ADP5310 features an adjustable output voltage range from 0.8 V to 5.0 V. The output voltage is set by the ratio of two external resistors. The device servos the output to maintain the voltage at the FBx pin at 0.8 V, referenced to ground; the current in R1 is then equal to 0.8 V/R2 plus the FB pin bias current. The bias current of the FBx pin, 15 nA at 25°C, flows through R2 into the FBx pin.

The output voltage is calculated using the equation

$$V_{OUT} = 0.8\ V(1 + R1/R2) + (I_{FB\_ADJ})(R1)$$

To minimize errors in the output voltage caused by the bias current of the FBx pin, maintain a value of R2 that is less than 200 kΩ. For example, when R1 and R2 each equal 200 kΩ, the output voltage is 1.6 V. The output voltage error introduced by the FBx pin bias current is 3 mV, or 0.187%, assuming a typical FBx pin bias current of 15 nA at 25°C.

Note that in shutdown mode, the output is turned off and the divider current is zero.

EFFICIENCY

Efficiency is the ratio of output power to input power. The high efficiency of the ADP5310 has two distinct advantages. First, only a small amount of power is lost in the dc-to-dc converter package, which in turn, reduces thermal constraints. Second, the high efficiency delivers the maximum output power for the given input power, thereby extending battery life in portable applications.

Power Switch Conduction Losses

Power switch dc conduction losses are caused by the flow of output current through the P-channel power switch and the N-channel synchronous rectifier, which have internal resistances ($R_{DS(ON)}$) associated with them. The amount of power loss is approximated by

$$P_{SW\_COND} = (R_{DS(ON)\_P} \times D + R_{DS(ON)\_N} \times (1 - D)) \times I_{OUT}^2$$

where:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The internal resistance of the power switches increases with temperature and increases when the input voltage is less than 5.5 V.

Inductor Losses

Inductor conduction losses are caused by the flow of current through the inductor, which has an internal DCR associated with it. Larger size inductors have smaller DCR, which can decrease inductor conduction losses. Inductor core losses relate to the magnetic permeability of the core material. Because the ADP5310 has high switching frequency dc-to-dc regulators, shielded ferrite core material is recommended because of its low EMI.

To estimate the total amount of power lost in the inductor (P_L), use the following equation:

$$P_L = DCR \times I_{OUT}^2 + Core\ Losses$$

Driver Losses

Driver losses are associated with the current drawn by the driver to turn on and turn off the power devices at the switching frequency. Each time a power device gate is turned on and turned off, the driver transfers a charge from the input supply to the gate, and then from the gate to ground.

Estimate driver losses using the following equation:

$$P_{DRIVER} = (C_{GATE\_P} + C_{GATE\_N}) \times V_{IN}^2 \times f_{SW}$$

where:
C_{GATE_P} is the gate capacitance of the internal high-side switch.
C_{GATE_N} is the gate capacitance of the internal low-side switch.
f_{SW} is the switching frequency.

The typical value for both gate capacitances, C_{GATE_P} and C_{GATE_N}, is 150 pF.

Transition Losses

Transition losses occur because the P-channel switch cannot turn on or turn off instantaneously. In the middle of an SWx node transition, the power switch provides all of the inductor current. The source-to-drain voltage of the power switch is half of the input voltage, resulting in power loss. Transition losses increase with both load current and input voltage and occur twice for each switching cycle.

Use the following equation to estimate transition losses:

$$P_{TRAN} = V_{IN}/2 \times I_{OUT} \times (t_R + t_F) \times f_{SW}$$

where:
t_R is the rise time of the SWx node.
t_F is the fall time of the SWx node.

The typical value for the rise and fall times, t_R and t_F, is 2 ns.

RECOMMENDED BUCK EXTERNAL COMPONENTS

The recommended external components for use with the ADP5310 are listed in Table 6, Table 7, and Table 8.

Table 6. Channel 1 Inductors

Vendor	Model	Frequency	Output Voltage (V)	Ideal Value (µH)	Standard Value (µH)	Dimensions (mm)	I_{SAT}[1] (A)	DCR (mΩ)
Coilcraft	XFL4020-102ME	1.2 MHz	1.2	1.1	1	4 × 4 × 2	4.5	12
Coilcraft	XFL4020-152ME	1.2 MHz	1.8	1.7	1.5	4 × 4 × 2	4.1	16
Coilcraft	XFL4020-222ME	1.2 MHz	2.5	2.4	2.2	4 × 4 × 2	3.1	24
Coilcraft	XFL4020-332ME	1.2 MHz	3.3	3.1	3.3	4 × 4 × 2	2.7	38
Coilcraft	XFL4020-472ME	1.2 MHz	5	4.7	4.7	4 × 4 × 2	2.0	57
Coilcraft	XFL4020-222ME	600 kHz	1.2	2.3	2.2	4 × 4 × 2	3.1	24
Coilcraft	XFL4020-332ME	600 kHz	1.8	3.4	3.3	4 × 4 × 2	2.7	38
Coilcraft	XFL4020-472ME	600 kHz	2.5	4.7	4.7	4 × 4 × 2	2.0	57
Coilcraft	XAL4030-682ME	600 kHz	3.3	6.2	6.8	4 × 4 × 3	1.9	74
Coilcraft	XAL4040-103ME	600 kHz	5	9.4	10	4 × 4 × 4	1.5	92

[1] I_{SAT} is the dc current at which the inductance drops 30% (typical) from its value without current.

Table 7. Channel 2 Inductors

Vendor	Model	Frequency	Output Voltage (V)	Ideal Value (µH)	Standard Value (µH)	Dimensions (mm)	I_{SAT}[1] (A)	DCR (mΩ)
Coilcraft	XFL4020-222ME	1.2 MHz	1.2	2.5	2.2	4 × 4 × 2	4.1	24
Coilcraft	XFL4020-332ME	1.2 MHz	1.8	3.8	3.3	4 × 4 × 2	3.1	38
Coilcraft	XFL4020-472ME	1.2 MHz	2.5	5.2	4.7	4 × 4 × 2	2.0	57
Coilcraft	XAL4030-682ME	1.2 MHz	3.0	6.3	6.8	4 × 4 × 3	1.9	74
Coilcraft	XAL4030-682ME	1.2 MHz	3.3	6.9	6.8	4 × 4 × 3	1.9	74
Coilcraft	XAL4040-103ME	1.2 MHz	5	10.5	10	4 × 4 × 4	1.5	92
Coilcraft	XFL4020-472ME	600 kHz	1.2	5.0	4.7	4 × 4 × 2	2.0	57
Coilcraft	XAL4030-682ME	600 kHz	1.8	7.5	6.8	4 × 4 × 3	1.9	74
Coilcraft	XAL4040-103ME	600 kHz	2.5	10.5	10	4 × 4 × 4	1.5	92
Coilcraft	XAL4040-103ME	600 kHz	3.0	12.6	10	4 × 4 × 4	1.5	92
Coilcraft	XAL4040-153ME	600 kHz	3.3	13.8	15	4 × 4 × 4	1.3	120
Coilcraft	LPS6235-223ML	600 kHz	5	20.9	22	6 × 6 × 3.5	1.6	145

[1] I_{SAT} is the dc current at which the inductance drops 30% (typical) from its value without current.

Table 8. 10 µF Capacitors

Vendor	Model	Case Size	Voltage Rating (V)	Location	Input Voltage (V)	Output Voltage (V)
Murata	GRM32ER7YA106KA12	1210	35	Input	$12 < V_{IN} < 15$	Not applicable
Murata	GRM32DR61E106KA12	1210	25	Input	$8 < V_{IN} < 12$	Not applicable
Murata	GRM31CR61C106KA88	1206	16	Input	$V_{IN} < 8$	Not applicable
Murata	GRM32ER7YA106KA12	1210	35	Output	Not applicable	$9 < V_{OUT} < V_{IN}$
Murata	GRM32DR61E106KA12	1210	25	Output	Not applicable	$7 < V_{OUT} < 9$
Murata	GRM31CR61C106KA88	1206	16	Output	Not applicable	$2.5 < V_{OUT} < 7$
Murata	GRM21BR61C106KE15	0805	16	Output	Not applicable	$V_{OUT} < 2.5$

CAPACITOR SELECTION

Output Capacitor

The ADP5310 is designed for operation with small, space-saving ceramic capacitors, but functions with most common capacitors provided that the ESR value is carefully considered. The ESR of the output capacitor affects the stability of the control loop. A minimum output capacitance of 6.2 µF with an ESR of 10 mΩ or less is recommended to ensure the stability of the ADP5310.

Input Bypass Capacitor

Connect a 10 µF capacitor from PVINx to PGND to reduce the circuit sensitivity to the printed circuit board (PCB) layout, especially when long input traces or high source impedance are encountered. If greater than 10 µF of output capacitance is required, increase the input capacitor to match the output capacitance to improve the transient response.

Input and Output Capacitor Properties

Use any good quality ceramic capacitors with the ADP5310; however they must meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectric capacitors with a voltage rating of 6.3 V to 25 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended because of their poor temperature and dc bias characteristics.

Use the following equation to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage:

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient (TC).
TOL is the worst-case component tolerance.

In this example, the worst-case TC over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 8.53 µF at 12 V for the 10 µF, 35 V capacitor in a 1210 package.

Substituting these values in Equation 1 yields

$$C_{EFF} = 8.53\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 6.53\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the ADP5310 over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP5310, it is imperative that the effects of dc bias, temperature, and tolerances of the capacitors are evaluated for each application.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

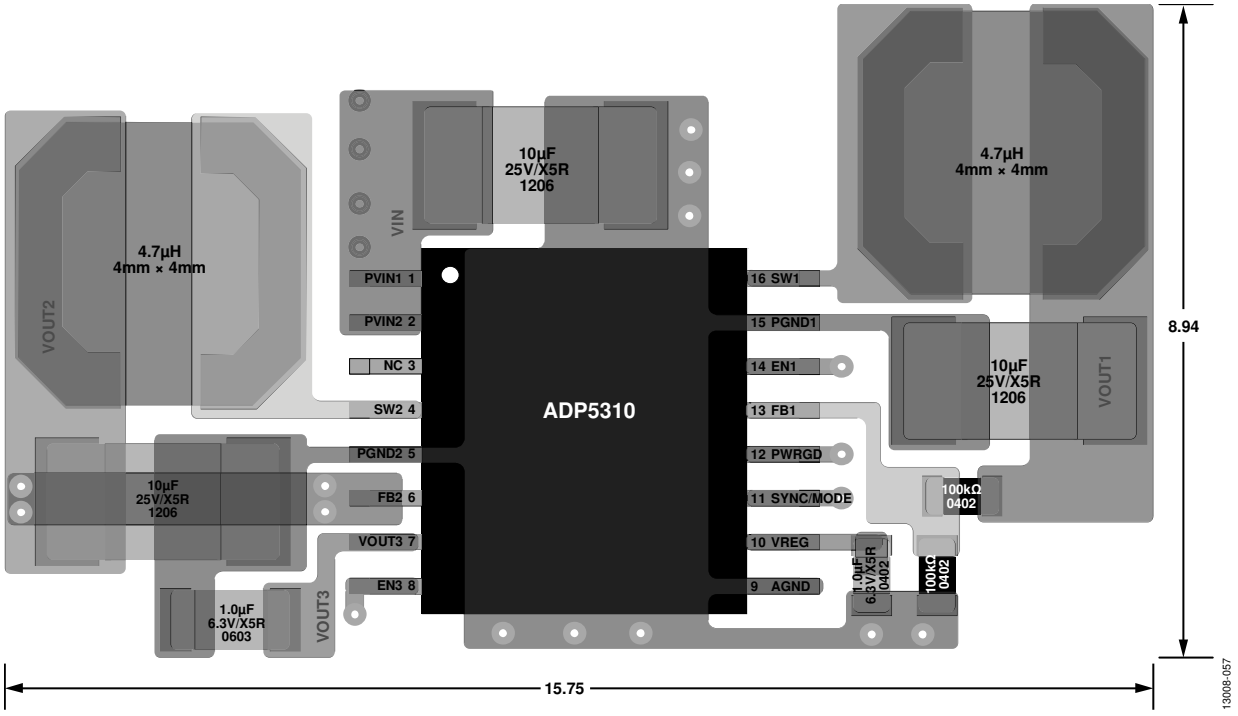

Figure 57. Typical PCB Layout for the ADP5310

TYPICAL APPLICATION CIRCUITS

Figure 58 and Figure 59 show how the ADP5310 can be applied in energy metering and medical applications controlled by a microcontroller or a processor.

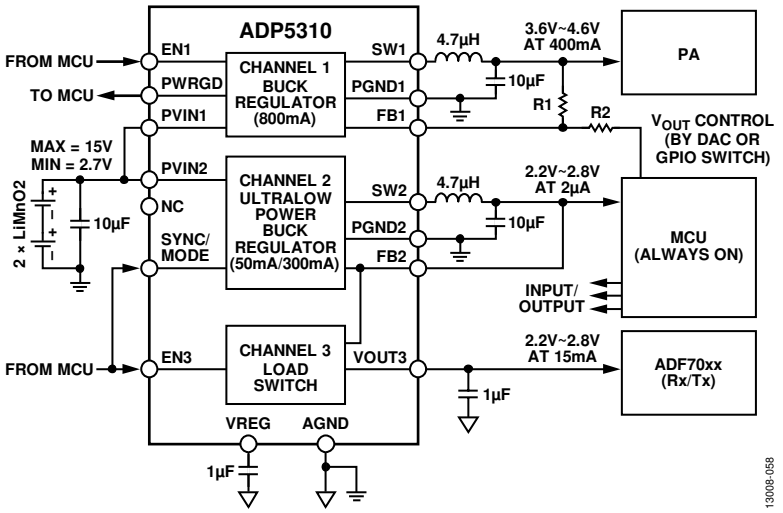

Figure 58. Typical Application of a Smart Meter

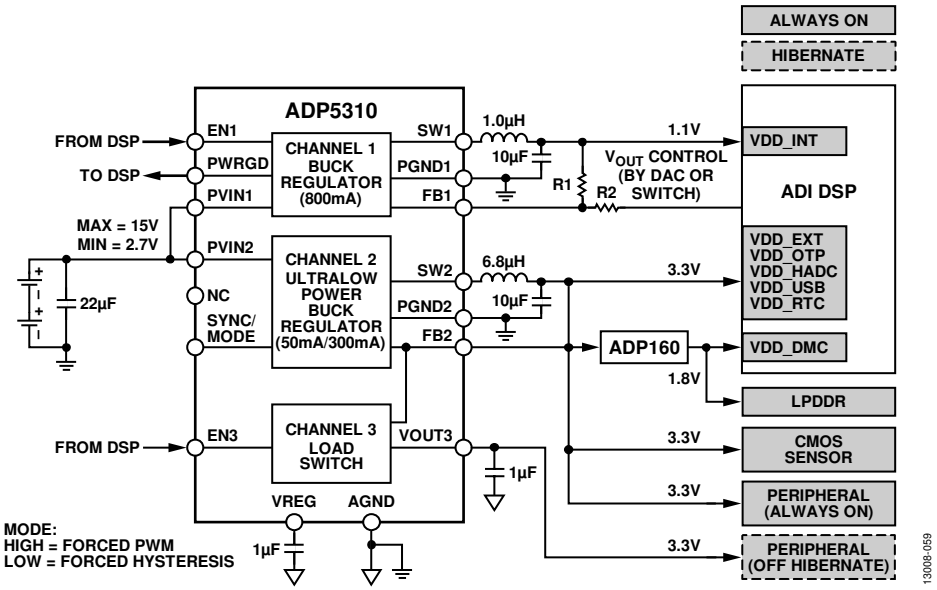

Figure 59. Battery Powered Typical Application with a DSP from Analog Devices, Inc.

FACTORY PROGRAMMABLE OPTIONS

To order a device with options other than the default options, contact your local Analog Devices sales or distribution representative.

Table 9. Output Voltage Options for Channel 1 (Fixed Output Options: 1.2 V to 5.0 V)

Option	Description
Option 0	0.8 V adjustable output (default)
Option 1	1.2 V fixed output
Option 2	1.5 V fixed output
Option 3	1.8 V fixed output
Option 4	2.5 V fixed output
Option 5	2.85 V fixed output
Option 6	3.3 V fixed output
Option 7	5.0 V fixed output

Table 10. Output Voltage Options for Channel 2 (Fixed Output Options: 1.20 V to 3.60 V in 50 mV Increments, and 3.60 V to 5.00 V in 100 mV Increments)

Option	Description
Option 0	0.8 V adjustable output (note that the Channel 3 load switch is not usable in this configuration)
Option 1	1.20 V fixed output
Option 2	1.25 V fixed output
…	…
Option 35	2.90 V fixed output
Option 36	2.95 V fixed output
Option 37	3.00 V fixed output (default)
Option 38	3.05 V fixed output
…	…
Option 48	3.55 V fixed output
Option 49	3.60 V fixed output
Option 50	3.70 V fixed output
Option 51	3.80 V fixed output
…	…
Option 62	4.90 V fixed output
Option 63	5.00 V fixed output

Table 11. Switching Frequency

Option	Description
Option 0	1.2 MHz (default)
Option 1	600 kHz

Table 12. Operation Mode for Channel 1

Option	Description
Option 0	Forced PWM mode
Option 1	Automatic PWM/PSM mode (default)

Table 13. Output Discharge Functionality Options for Channel 1

Option	Description
Option 0	Output discharge function disabled for the buck regulator in Channel 1 (default)
Option 1	Output discharge function enabled for the buck regulator in Channel 1

Table 14. Output Discharge Functionality Options for Channel 2

Option	Description
Option 0	Output discharge function disabled for the buck regulator in Channel 2 (default)
Option 1	Output discharge function enabled for the buck regulator in Channel 2

Table 15. Output Discharge Functionality Options for Channel 3

Option	Description
Option 0	Output discharge function disabled for the load switch in Channel 3 (default)
Option 1	Output discharge function enabled for the load switch in Channel 3

Table 16. Soft Start Time for Channel 1

Option	Description
Option 0	350 µs (default)
Option 1	2800 µs

Table 17. Soft Start Time for Channel 2

Option	Description
Option 0	350 µs (default)
Option 1	2800 µs

Table 18. Turn-On Rise (Soft Start) Time for Channel 3

Option	Description
Option 0	3 µs
Option 1	12 µs (default)
Option 2	48 µs
Option 3	192 µs

OUTLINE DIMENSIONS

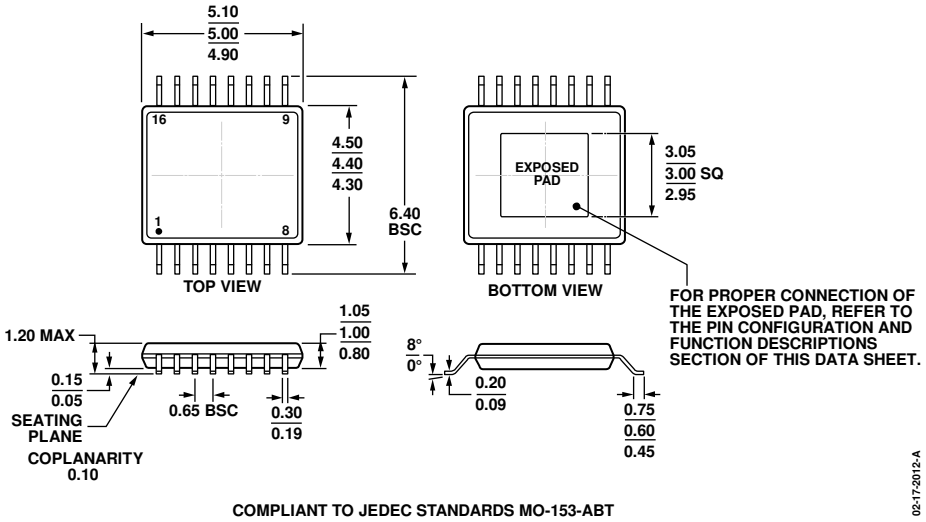

Figure 60. 16-Lead Thin Shrink Small Outline With Exposed Pad [TSSOP_EP]
(RE-16-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage	Package Description	Package Option
ADP5310AREZN-255R7	−40°C to +125°C	Channel 1 = adjustable, Channel 2 = 2.55 V	16-Lead TSSOP_EP	RE-16-2
ADP5310AREZN-2.8R7	−40°C to +125°C	Channel 1 = adjustable, Channel 2 = 2.8 V	16-Lead TSSOP_EP	RE-16-2
ADP5310AREZN-3.3R7	−40°C to +125°C	Channel 1 = adjustable, Channel 2 = 3.3 V	16-Lead TSSOP_EP	RE-16-2
ADP5310AREZN-R7	−40°C to +125°C	Channel 1 = adjustable with automatic PWM/PSM mode, Channel 2 = adjustable	16-Lead TSSOP_EP	RE-16-2
ADP5310READJ-EVALZ			Evaluation Board	

[1] Z = RoHS Compliant Part.

D13008-0-11/16(A)