Zero Drift, High Voltage, Low Power, Programmable Gain Instrumentation Amplifier

Data Sheet

ADA4254

FEATURES

- Optimized for ADC synchronization
- Low power: 22 mW (±12 V supplies)
- 12 binary gain steps from 1/16 V/V to 128 V/V
- 3 scaling gains: 1 V/V, 1.25 V/V, and 1.375 V/V
- ±60 V protected input multiplexer
- Excellent dc precision
  - Low input offset voltage: ±14 µV maximum
  - Low input offset voltage drift: ±0.08 µV/°C maximum
  - Gain calibration via ROM
  - Low gain drift: ±1 ppm/°C maximum
  - High CMRR: 116 dB minimum, G = 1 V/V
- Low input bias current: ±1.5 nA maximum
- High input impedance
- Integrated input EMI filtering
- Wide input supply range: ±5 V to ±28 V
- Dedicated output amplifier supplies
- 7 GPIO ports with special functions
- Sequential chip select mode
- External multiplexer control
- Excitation current sources
- SPI port with checksum (CRC) support
- Internal fault detection
- Wire break test currents
- On-chip test multiplexer
- 28-lead, 5 mm × 5 mm LFCSP, 24-lead TSSOP
- Specified temperature range: −40°C to +105°C

APPLICATIONS

- Universal process control front ends
- Data acquisition systems
- Test and measurement systems

GENERAL DESCRIPTION

The ADA4254 is a zero drift, high voltage, low power programmable gain instrumentation amplifier (PGIA) designed for process control and industrial applications. The ADA4254 features 12 binary weighted gains ranging from 1/16 V/V to 128 V/V and three scaling gain options of 1 V/V, 1.25 V/V, and 1.375 V/V, resulting in 36 possible gain settings. The power consumption of the ADA4254 is a mere 22 mW, making the device an excellent choice for industrial systems that demand precision, robustness, and low power.

The zero drift amplifier topology of the ADA4254 self calibrates dc errors and low frequency 1/f noise, achieving excellent dc precision over the entire specified temperature range. This high level of precision maximizes dynamic range and greatly reduces calibration requirements in many applications.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

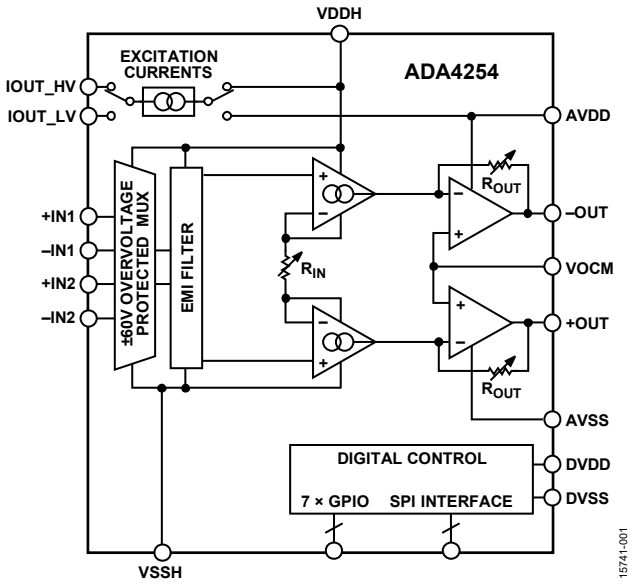

Figure 1.

The input multiplexer provides ±60 V protection to the high impedance inputs of the amplifier, while providing the capability to switch between two input sources. In addition, integrated electromagnetic interference (EMI) filters block harsh RF noise from the sensitive inputs of the amplifier.

Various safety features on the ADA4254 detect both internal and external faults. The serial port interface (SPI) supports cyclical redundancy check (CRC) error detection to ensure robust communication. These safety features ease system safety integrity level (SIL) certification.

Seven general-purpose input/output (GPIO) pins, which can be configured to provide various special functions, are included in the ADA4254. An excitation current source output is available to bias sensors such as resistance temperature detectors (RTDs).

The ADA4254 is specified over the −40°C to +105°C temperature range and is offered in a compact 5 mm × 5 mm, 28-lead LFCSP and a 24-lead TSSOP.

COMPANION PRODUCTS

ADCs: AD4007, AD7768, AD7175-2
ADC Drivers: ADA4945-1, LTC6363
Voltage References: ADR4550, ADR3450, LT6656

Rev. B
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

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11/2019—Rev. 0 to Rev. A

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11/2019—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, VDDH = 28 V, VSSH = −28 V, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, DVSS = 0 V, VOCM = AVDD/2, and no load, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OFFSET VOLTAGE	Total offset, referred to input (RTI) = $V_{OSI} + \frac{V_{OSO}}{Gain}$				
Differential Offset Voltage					
Input Offset Voltage (V_{OSI})			±3	±14	µV
Output Offset Voltage (V_{OSO})			±40	±125	µV
Differential Offset Voltage Drift	T_A = −40°C to +105°C[1], total offset drift, RTI = $V_{OSI}/T + \frac{V_{OSO}/T}{Gain}$				
V_{OSI}/T			±0.03	±0.08	µV/°C
V_{OSO}/T			±0.98	±2.5	µV/°C
Differential Offset Voltage vs. VDDH and VSSH (Power Supply Rejection Ratio (PSRR)), RTI	VDDH − VSSH = 10 V to 56 V				
Gain (G) = 1/16 V/V		80	90		dB
G = 1 V/V		110	120		dB
G = 128 V/V		140	154		dB
Differential Offset Voltage vs. AVDD (PSRR), RTI	AVDD − AVSS = 2.7 V to 5.5 V				
G = 1/16 V/V		66	76		dB
G = 1 V/V		90	100		dB
G = 128 V/V		118	136		dB
Differential Offset vs. External Clock Frequency, RTI	Clock frequency = 0.8 MHz to 1.2 MHz				
G = 1/16 V/V			±0.2		µV/kHz
G = 1 V/V			±0.1		µV/kHz
G = 128 V/V			±0.002		µV/kHz
COMMON–MODE REJECTION RATIO (CMRR), RTI	+IN = –IN = –25 V to +25 V, scaling gain = 1 V/V				
CMRR to 60 Hz					
G = 1/16 V/V		92	102		dB
G = 1 V/V		116	126		dB
G = 128 V/V		140	150		dB
G = 1/16	T_A = −40°C to +105°C[1]	88			dB
G = 1	T_A = −40°C to +105°C[1]	112			dB
G = 128	T_A = −40°C to +105°C[1]	136			dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GAIN	Output voltage (V_{OUT}) = 8.5 V p-p[2]				
Input Gain Range			1/16 to 128		V/V
Output Gain Range			1, 1.25, 1.375		V/V
Gain Error					
Before Calibration	All Gains		<±0.06	±0.12	%
Using Calibration Coefficient	All Gains		<±0.01	±0.025	%
All Gain Values Except as Follows:	T_A = −40°C to +105°C[1]		<±0.3	±1	ppm/°C
G = 1/16 V/V, All Scaling Gains	T_A = −40°C to +105°C[1]		±0.8	±1.5	ppm/°C
G = 32 V/V, 64 V/V, All Scaling Gains	T_A = −40°C to +105°C[1]		±0.4	±1.5	ppm/°C
G = 128 V/V, Scaling Gains 1 V/V, 1.25 V/V	T_A = −40°C to +105°C[1]		±0.6	±2	ppm/°C
G = 128 V/V, Scaling Gain 1.375 V/V	T_A = −40°C to +105°C[1]		±0.7	±2.5	ppm/°C
Nonlinearity	All gains except 32 V/V, 64 V/V and 128 V/V[2, 3]		5	15	ppm
	G = 32 V/V		7.5		ppm
	G = 64 V/V		12		ppm
	G = 128 V/V		15		ppm
NOISE	Total noise, RTI = $\sqrt{e_{ni}^2 + \left(\frac{e_{no}}{Gain}\right)^2}$				
Voltage Noise, 1 kHz, RTI					
Input Noise (e_{ni})			17		nV/√Hz
Output Noise (e_{no})			253		nV/√Hz
0.1 Hz to 10 Hz, RTI					
G = 1/16 V/V			95		µV p-p
G = 1 V/V			5.75		µV p-p
G = 128 V/V			330		nV p-p
0.01 Hz to 10 Hz, RTI					
G = 1/16 V/V			100		µV p-p
G = 1 V/V			6.8		µV p-p
G = 128 V/V			395		nV p-p
Current Noise					
10 Hz			100		fA/√Hz
0.1 Hz to 10 Hz			3.1		pA p-p
0.01 Hz to 10 Hz			4		pA p-p
INPUT CHARACTERISTICS					
Input Bias Current			±0.45	±1.5	nA
	T_A = −40°C to +85°C[1]			±4	nA
	T_A = −40°C to +105°C[1]			±14	nA
Input Offset Current			±0.2	±1.3	nA
	T_A = −40°C to +85°C[1]			±2.5	nA
	T_A = −40°C to +105°C[1]			±3.5	nA
Input Impedance	Common mode		>1‖11		GΩ‖pF
	Differential		>1‖4.7		GΩ‖pF
Input Operating Voltage Range	Guaranteed by CMRR	VSSH + 3		VDDH − 3	V
MUX_OVER_VOLT_ERR					
Positive Threshold			VDDH − 0.9		V
Negative Threshold			VSSH + 0.9		V
INPUT_ERR/GAIN_RST					
Positive Threshold			VDDH − 1.5		V
Negative Threshold			VSSH + 1.5		V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG OUTPUTS					
Output Voltage Swing from Each Rail	AVDD = 5 V, load resistor (R_L) = 2.49 kΩ to 2.5 V	AVSS + 0.06		AVDD − 0.08	V
	AVDD = 2.7 V, R_L = 1.8 kΩ to 1.35 V	AVSS + 0.05		AVDD − 0.06	V
Capacitive Load Drive			500		pF
Short-Circuit Current	To 2.5 V, G = 1.375, AVDD = 2.7 V to 5 V	3.5	11	25	mA
OUTPUT_ERR					
Positive Threshold			AVDD − 0.03		V
Negative Threshold			AVSS + 0.03		V
VOCM DYNAMIC PERFORMANCE					
−3 dB Bandwidth			2.3		MHz
Slew Rate			1.9		V/µs
Voltage Noise	Frequency = 1 kHz		160		nV/√Hz
Gain			1		V/V
VOCM INPUT CHARACTERISTICS					
Input Voltage Range		AVSS		AVDD − 1	V
Input Resistance			10		GΩ
Common Mode Offset Voltage			20		µV
Common Mode Offset Voltage Drift			2.5		µV/°C
Input Bias Current			500		pA
DYNAMIC RESPONSE					
Small Signal ±3 dB Bandwidth					
G = 1/16 V/V			15		kHz
G = 1/8 V/V			28		kHz
G = 1/4 V/V			67		kHz
G = 1/2 V/V			138		kHz
G = 1 V/V			1800		kHz
G = 2 V/V			513		kHz
G = 4 V/V			341		kHz
G = 8 V/V			319		kHz
G = 16 V/V			297		kHz
G = 32 V/V			275		kHz
G = 64 V/V			257		kHz
G = 128 V/V			209		kHz
Settling Time 0.01%	V_{OUT} = 8 V p-p				
G = 1 V/V			10		µs
G = 8 V/V			8		µs
G = 128 V/V			5		µs
Settling Time 0.0015% (16-Bit)	V_{OUT} = 8 V p-p				
G = 1 V/V			18		µs
G = 8 V/V			15		µs
G = 128 V/V			15		µs
Slew Rate	V_{OUT} = 8 V p-p[2]				
G = 1/16 V/V			0.06		V/µs
G = 1 V/V			0.8		V/µs
G = 128 V/V			3.1		V/µs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
THD	V_{OUT} = 8 V p-p at frequency = 1 kHz				
G = 1 V/V			−104		dB
G = 8 V/V			−96		dB
G = 128 V/V			−80		dB
Input Overload Recovery Time	Input voltage (V_{IN}) = 56 V p-p		40		µs
Output Overload Recovery Time	G = 1 V/V, V_{IN} = 10 V p-p		6		µs
EXCITATION CURRENT SOURCES (IOUT_LV/IOUT_HV)					
Output Current Range		100		1500	µA
Initial Tolerance			±3	±10	%
Drift	T_A = −40°C to +105°C		±200		ppm/°C
Current Matching			±3	±8	%
Drift Matching	T_A = −40°C to +105°C		±50		ppm/°C
WIRE BREAK CURRENTS					
Output Current Range		0.25		16	µA
Impedance Threshold			(VDDH − 4)/I_{WB}[4]		Ω
Initial Tolerance			±12		%
Drift	T_A = −40°C to +105°C		±250		ppm/°C
DIGITAL INPUTS					
Low (V_{INL})		0		0.8	V
High (V_{INH})		0.6 × DVDD		DVDD	V
Digital Input Pin Capacitance			5		pF
DIGITAL OUTPUT					
Low (V_{OL})	Sinking 4 mA			0.7	V
High (V_{OH})	Sourcing 2 mA	DVDD − 0.8			V
INTERNAL/EXTERNAL CLOCK					
Internal Clock Frequency		0.8	1	1.2	MHz
Duty Cycle			50		%
Internal Clock Divider Range		1		32	MHz/MHz
POWER SUPPLY					
VDDH − VSSH		10		56	V
AVDD − AVSS		2.7		5	V
DVDD − DVSS		2.7		5	V
IVDDH			600	765	µA
IVSSH			780	985	µA
IDVDD	DVDD = 3 V		150	205	µA
IAVDD			980	1305	µA
Static Power Dissipation	DVDD = 3 V, VSSH = −28 V, VDHH = 28 V		44	56	mW
	DVDD = 3 V, VSSH = −15 V, VDDH = 15 V		26	34	mW
	DVDD = 3 V, VSSH = −12 V, VDDH = 12 V		22	28	mW

[1] Guaranteed by design. These specifications are not production tested but are supported by characterization data at the initial product release.
[2] For gains less than 1/2, a smaller output swing is used.
[3] Only G = 1 V/V is production tested.
[4] I_{WB} means wire break current.

TIMING SPECIFICATIONS

VDDH = 28 V, VSSH = −28 V, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, DVSS = 0 V, VOCM = AVDD/2 V.

Table 2. Digital Values and SPI Timing Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Maximum Clock Rate (SCLK)				5	MHz
Minimum Pulse Width (SCLK)					
High	t_{PWH}	75			ns
Low	t_{PWL}	75			ns
SDI/SDO to SCLK Setup Time	t_{DS}	10			ns
SDI/SDO to SCLK Hold Time	t_{DH}	10			ns
Data Valid, SDO to SCLK	t_{DV}	50			ns
Setup Time, $\overline{CS}$ to SCLK	$t_{D\overline{CS}}$	30			ns

Timing Diagrams

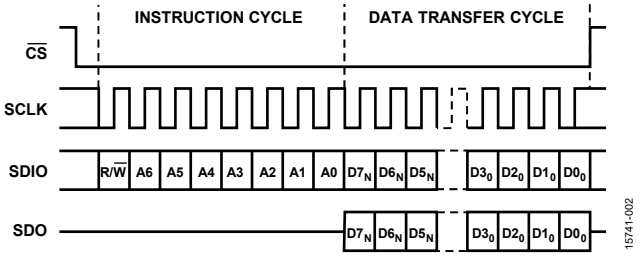


Figure 2. SPI Timing Diagram, MSB First

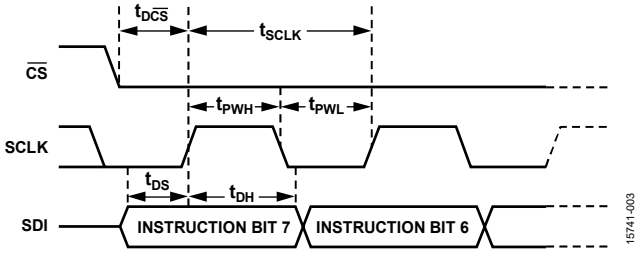


Figure 3. SPI Register Write Timing Diagram

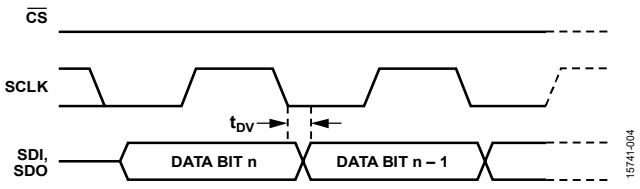


Figure 4. SPI Register Read Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VDDH	VSSH – 0.3 V to VSSH + 60 V
AVDD	AVSS – 0.3 V to AVSS + 5.5 V
DVDD	DVSS – 0.3 V to DVSS + 5.5 V
AVSS or DVSS	VSSH – 0.3 V to VSSH + 30 V
Voltage	VDDH – 30 V to VDDH + 0.3 V
Current	±10 mA
Input Voltage (+IN1, –IN1, +IN2, or –IN2)	VSSH – 60 V to VSSH + 60 V
Differential Input Voltage Between Any Two Amplifier Inputs (+IN1, –IN1, +IN2, or –IN2)	60 V
–OUT, +OUT Short-Circuit Current	Indefinite
VOCM	
Voltage	AVSS – 0.3 V to AVDD + 0.3 V
Current	±10 mA
Digital Inputs/Outputs (SPI and GPIO), Voltage	DVSS – 0.3 V to DVDD + 0.3 V
Digital Inputs (SPI and GPIO), Current	±10 mA
IOUT_LV	
Voltage	AVSS – 0.3 V to AVDD + 0.3 V
Current	±10 mA
IOUT_HV	
Voltage	VSSH – 0.3 V to VDDH + 0.3 V
Current	±10 mA
Operating Temperature Range	–40°C to +125°C
Specified Temperature Range	–40°C to +105°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	–65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient, thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
CP-28-10	36.9	1.9	°C/W
RU-24	64.8	14.11	°C/W

[1] The thermal resistance values specified in Table 4 are simulated based on JEDEC specifications (unless specified otherwise) and must be used in compliance with JESD51-12.

Refer to the ESD Map section for a schematic of ESD diodes and paths.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

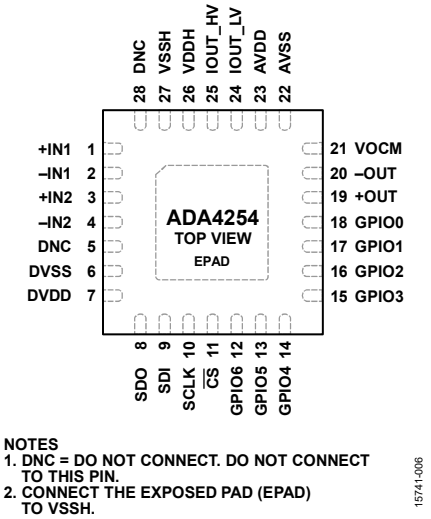


Figure 5. 28-Lead LFCSP Pin Configuration

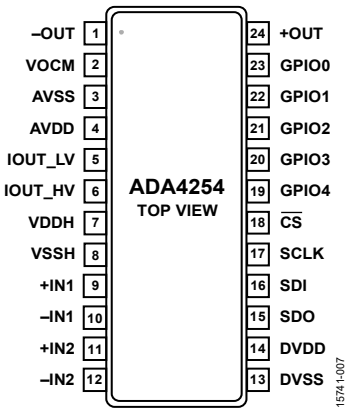


Figure 6. 24-Lead TSSOP Pin Configuration

Table 5. Pin Function Descriptions

Mnemonic	LFCSP Pin No.	TSSOP Pin No.	Description
+IN1	1	9	Channel 1 Positive Input.
–IN1	2	10	Channel 1 Negative Input.
+IN2	3	11	Channel 2 Positive Input.
–IN2	4	12	Channel 2 Negative Input.
DNC	5, 28	Not applicable	Do Not Connect. Do not connect to this pin.
DVSS	6	13	Negative Digital Supply Voltage.
DVDD	7	14	Positive Digital Supply Voltage.
SDO	8	15	SPI Serial Data Output.
SDI	9	16	SPI Serial Data Input.
SCLK	10	17	SPI Serial Clock Input.
$\overline{CS}$	11	18	SPI Chip Select Input.
GPIO6	12	Not applicable	GPIO6/SCS6.
GPIO5	13	Not applicable	GPIO5/SCS5.
GPIO4	14	19	GPIO4/SCS4/Clock Input or Output.
GPIO3	15	20	GPIO3/SCS3/Fault Interrupt Output.
GPIO2	16	21	GPIO2/SCS2/Calibration Busy Out.
GPIO1	17	22	GPIO1/SCS1/External Multiplexer Control 1.
GPIO0	18	23	GPIO0/SCS0/External Multiplexer Control 0.
+OUT	19	24	Positive Output.
–OUT	20	1	Negative Output.
VOCM	21	2	Output Amplifier Common-Mode Voltage Input. This pin is high impedance and is not internally biased.
AVSS	22	3	Output Amplifier Negative Supply Voltage.
AVDD	23	4	Output Amplifier Positive Supply Voltage.
IOUT_LV	24	5	Low Voltage Excitation Current Source Output.
IOUT_HV	25	6	High Voltage Excitation Current Source Output.
VDDH	26	7	Positive High Voltage Supply.
VSSH	27	8	Negative High Voltage Supply.
EPAD		Not applicable	Exposed Pad. Connect the exposed pad (EPAD) to VSSH.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, VDDH = 28 V, VSSH = −28 V, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, DVSS = 0 V, VOCM = AVDD/2, and no load, unless otherwise noted.

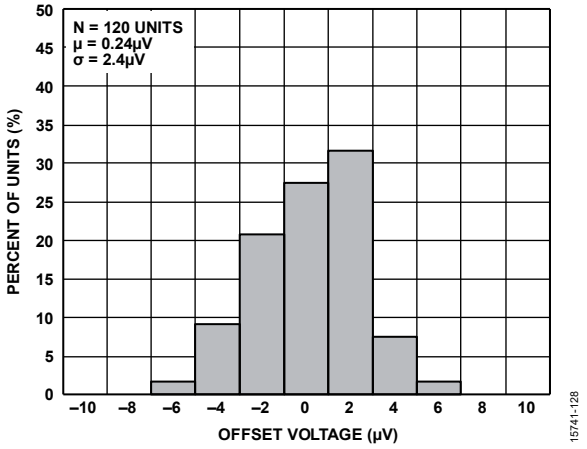


Figure 7. Offset Voltage Distribution, RTI (Gain = 128 V/V)

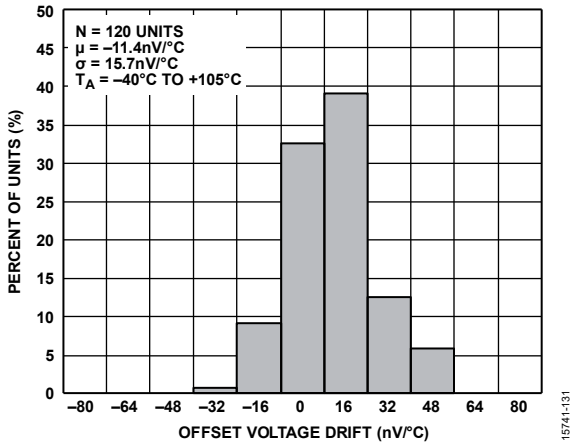


Figure 10. Offset Voltage Drift Distribution, RTI (Gain = 128 V/V)

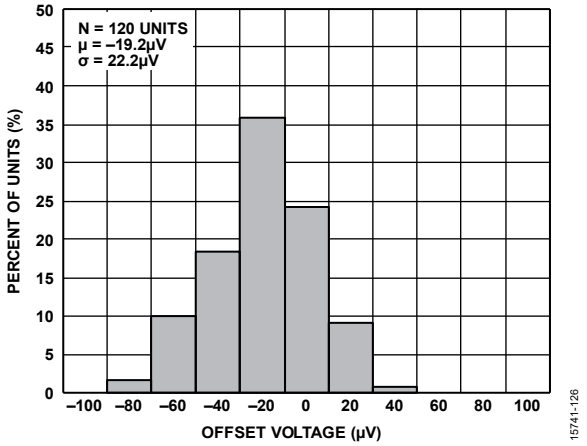


Figure 8. Offset Voltage Distribution, RTI (Gain = 1 V/V)

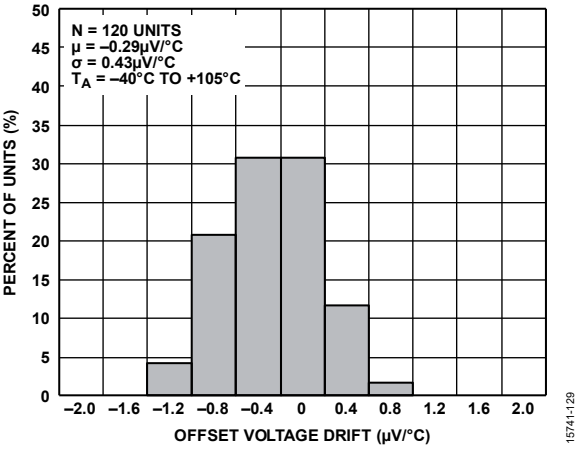


Figure 11. Offset Voltage Drift Distribution, RTI (Gain = 1 V/V)

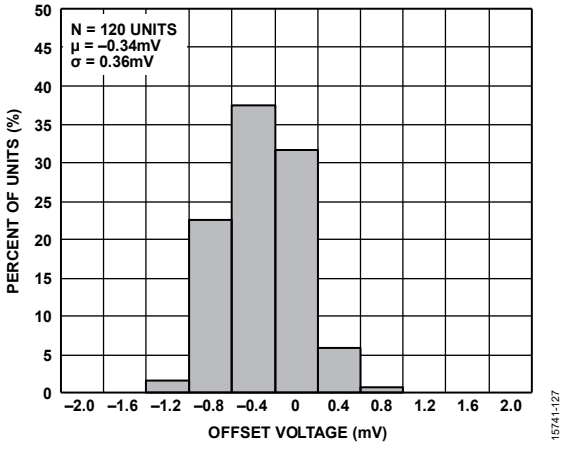


Figure 9. Offset Voltage Distribution, RTI (Gain = 1/16 V/V)

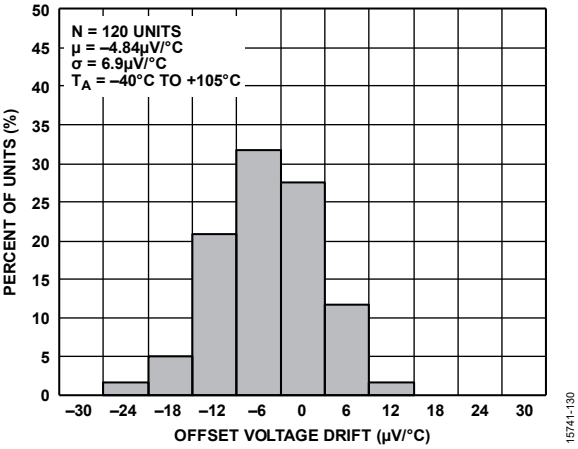


Figure 12. Offset Voltage Drift Distribution, RTI (Gain = 1/16 V/V)

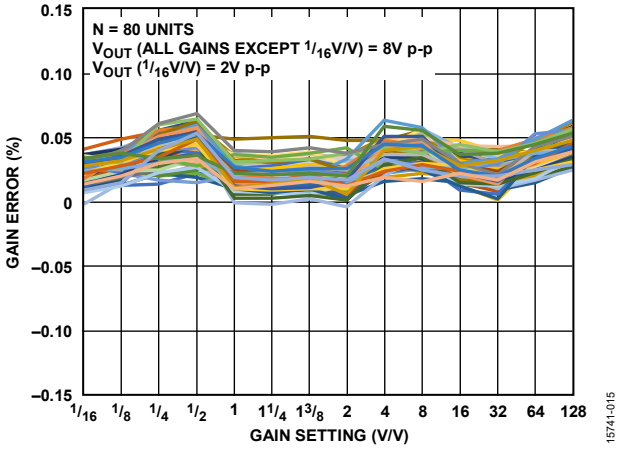


Figure 13. Gain Error vs. Gain Setting

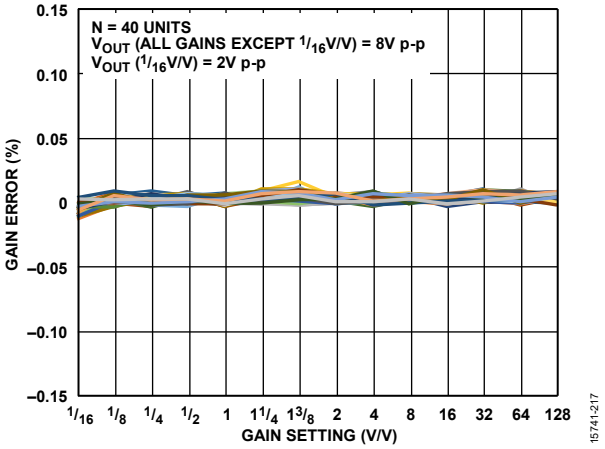


Figure 16. Gain Error vs. Gain Setting Using Calibration Coefficients

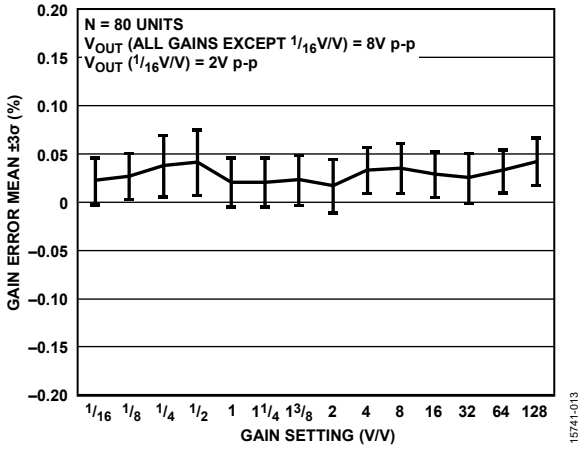


Figure 14. Gain Error Distribution vs. Gain Setting

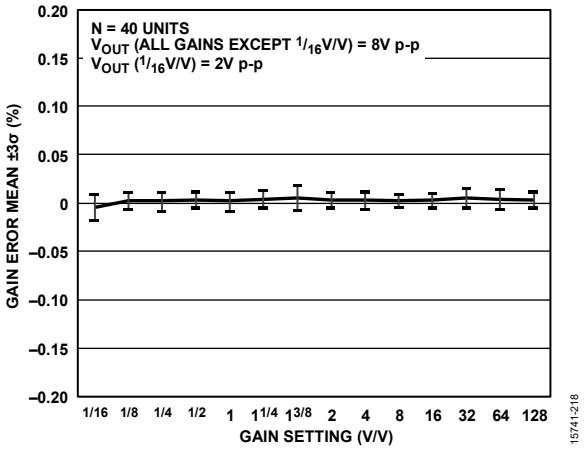


Figure 17. Gain Error Distribution vs. Gain Setting Using Calibration Coefficients

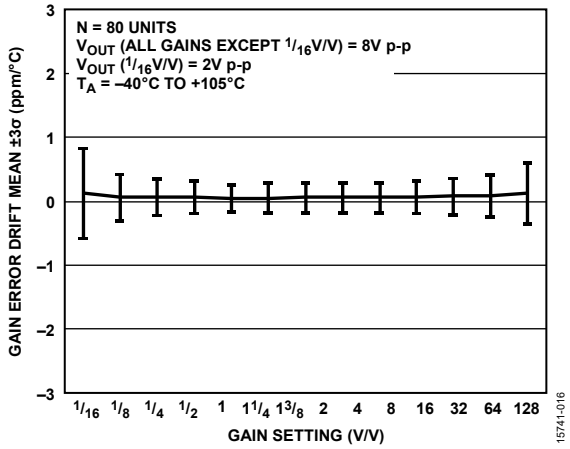


Figure 15. Gain Error Drift vs. Gain Setting

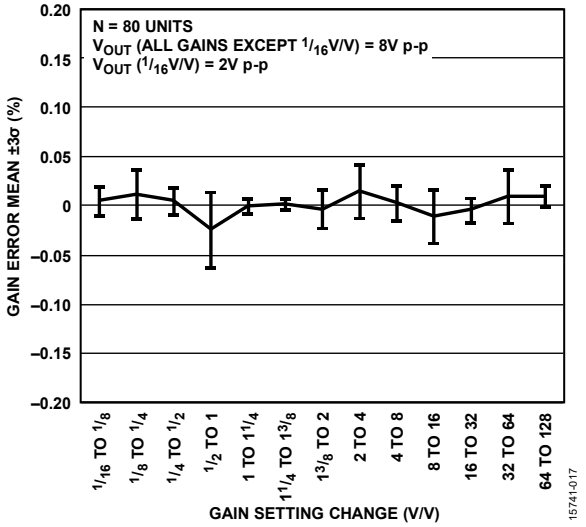


Figure 18. Gain Error Deviation Between Sequential Gain Settings

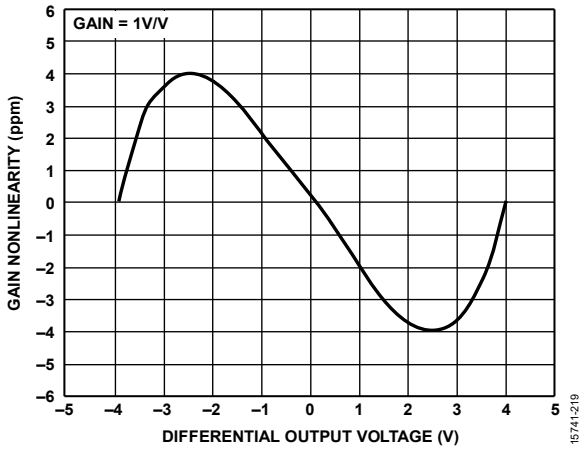


Figure 19. Gain Nonlinearity

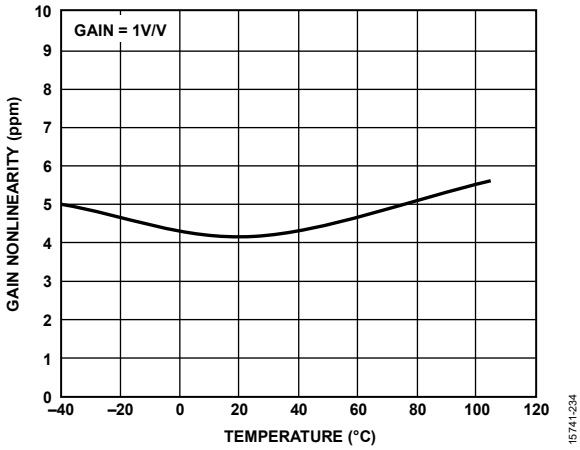


Figure 22. Gain Nonlinearity vs. Temperature

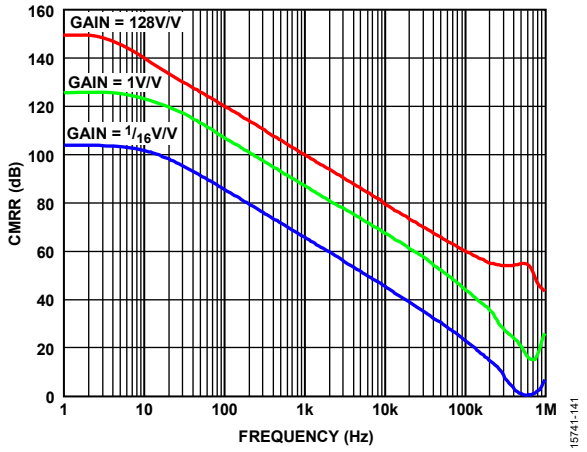


Figure 20. CMRR vs. Frequency

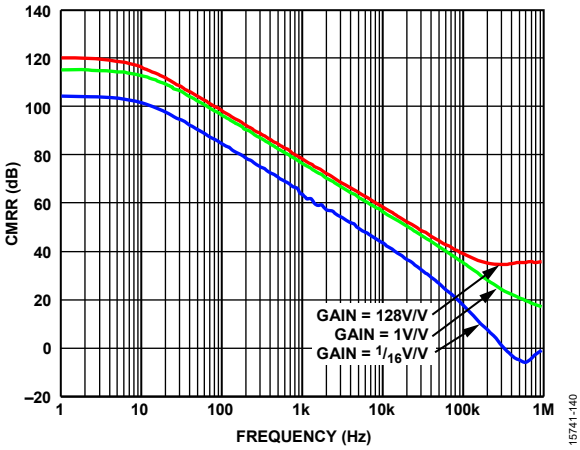


Figure 23. CMRR vs. Frequency with 1 kΩ Imbalance

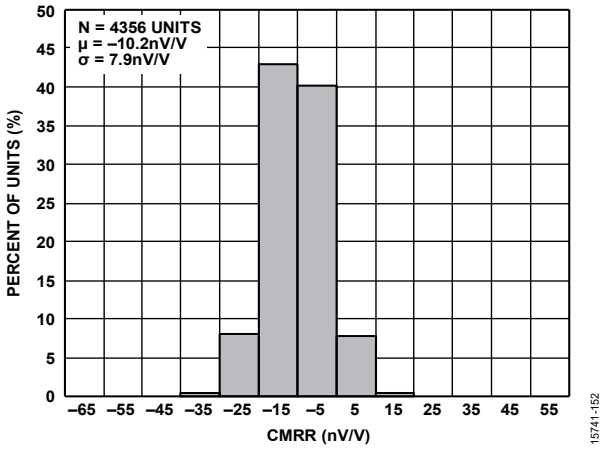


Figure 21. CMRR Distribution (Gain = 128 V/V)

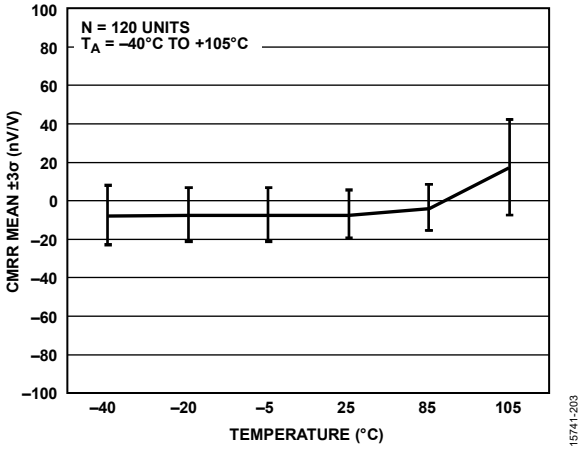


Figure 24. CMRR Mean vs. Temperature (Gain = 128 V/V)

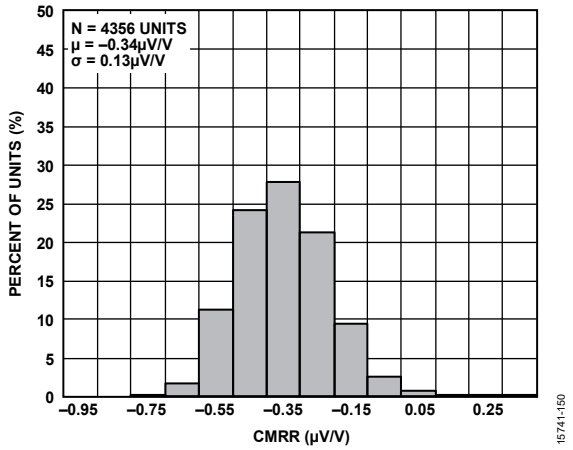


Figure 25. CMRR Distribution (Gain = 1 V/V)

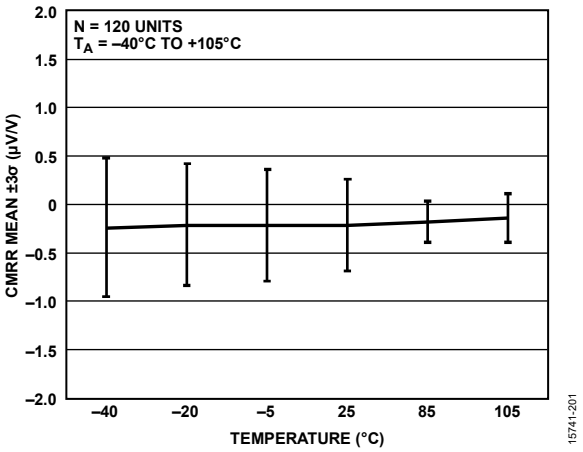


Figure 28. CMRR Mean vs. Temperature (Gain = 1 V/V)

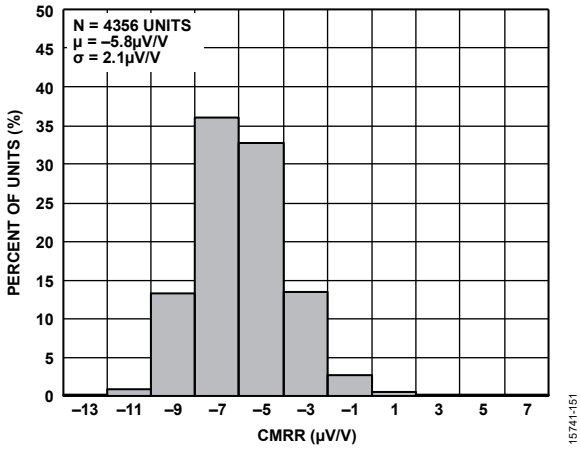


Figure 26. CMRR Distribution (Gain = 1/16 V/V)

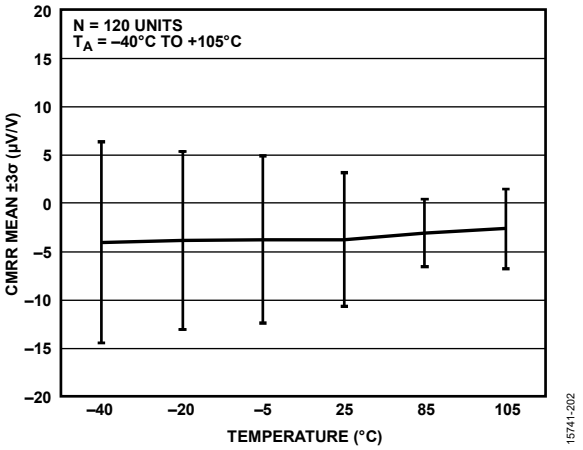


Figure 29. CMRR Mean vs. Temperature (Gain = 1/16 V/V)

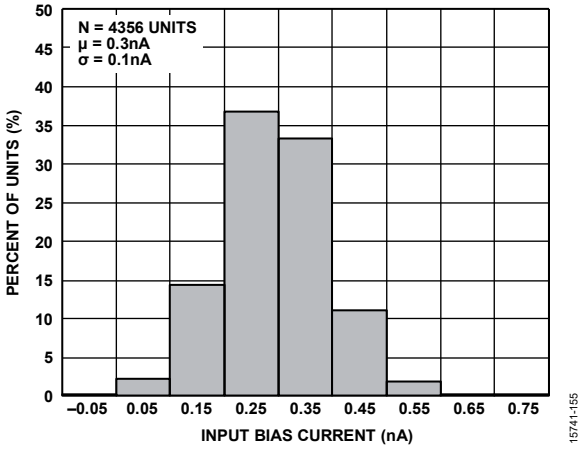


Figure 27. Input Bias Current Distribution

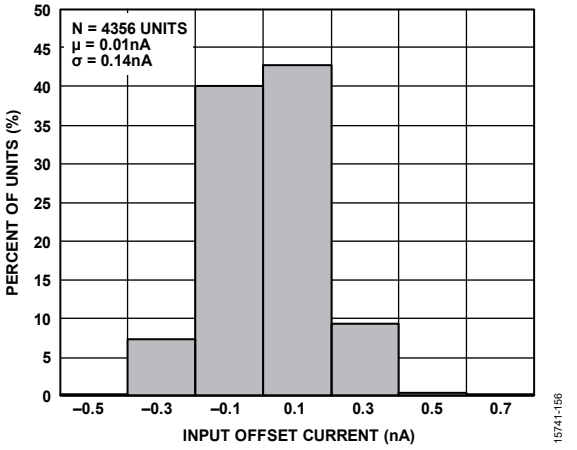


Figure 30. Input Offset Current Distribution

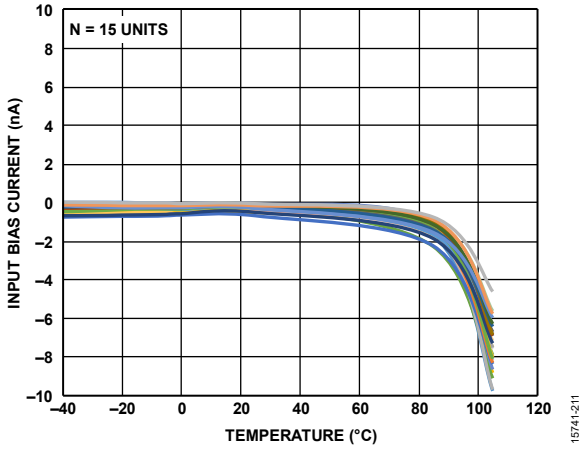


Figure 31. Input Bias Current vs. Temperature

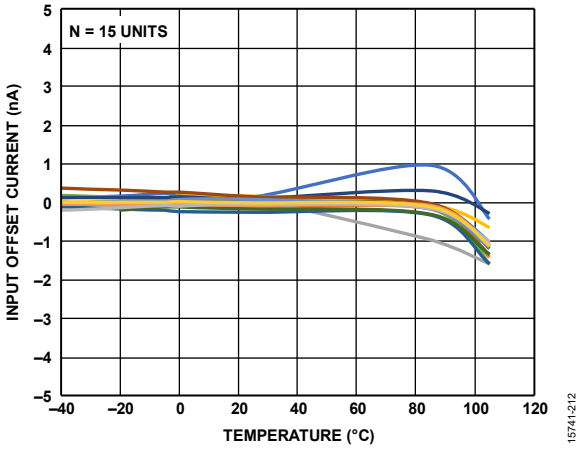


Figure 34. Input Offset Current vs. Temperature

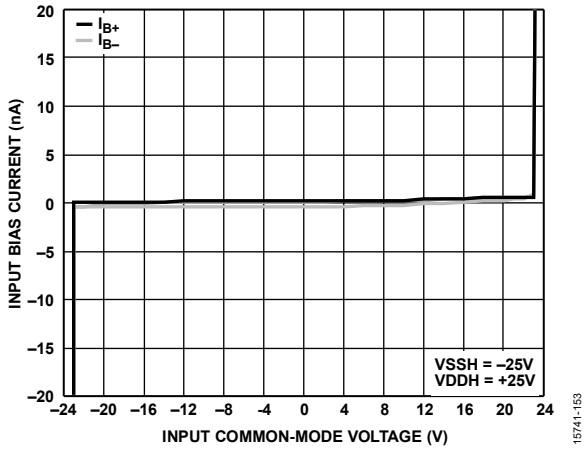


Figure 32. Input Bias Current vs. Input Common-Mode Voltage

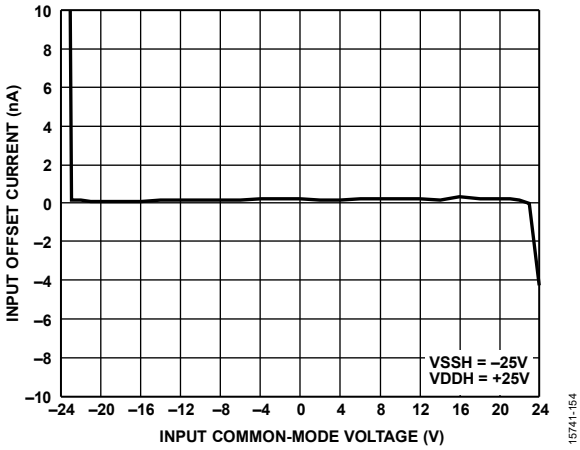


Figure 35. Input Offset Current vs. Input Common-Mode Voltage

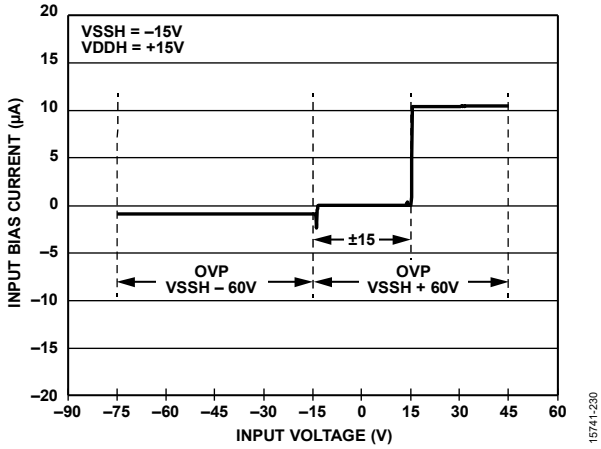


Figure 33. Input Overvoltage Performance, VDDH/VSSH = ±15 V

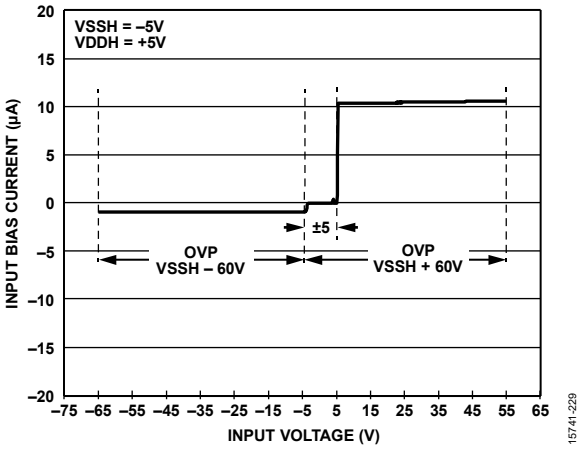


Figure 36. Input Overvoltage Performance, VDDH/VSSH = ±5 V

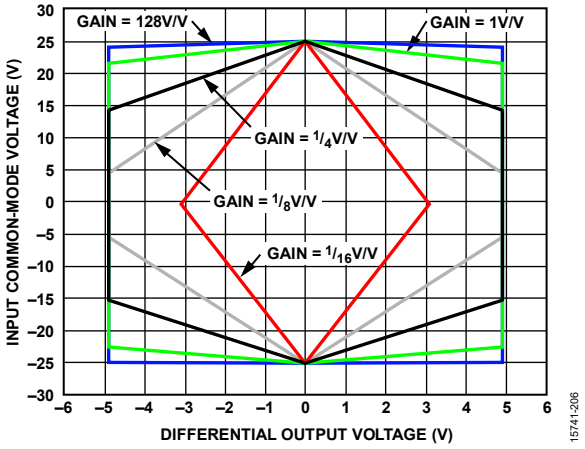


Figure 37. Diamond Plot

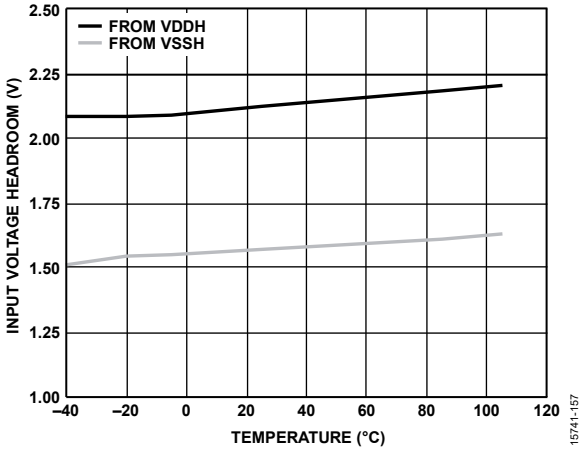


Figure 40. Input Voltage Headroom vs. Temperature

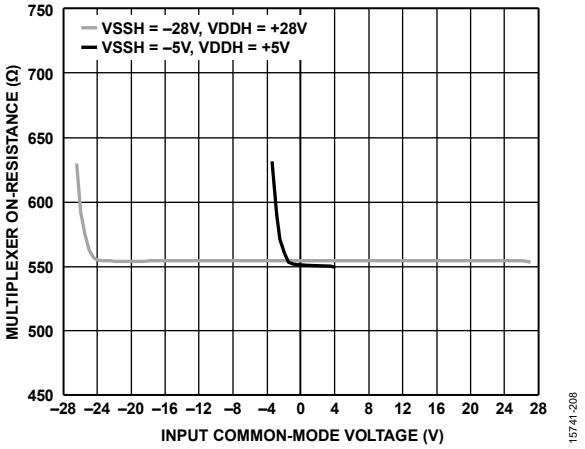


Figure 38. Multiplexer On-Resistance vs. Input Common-Mode Voltage

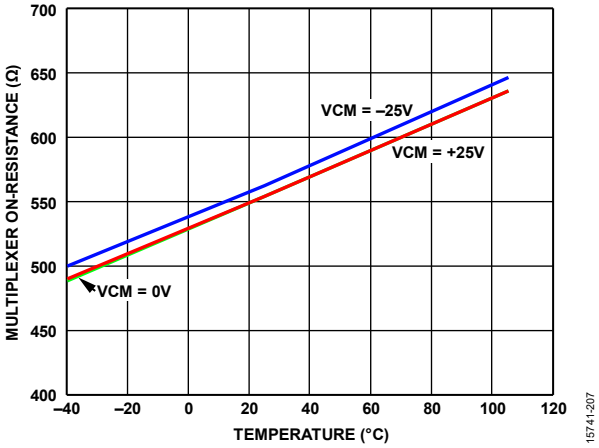


Figure 41. Multiplexer On-Resistance vs. Temperature

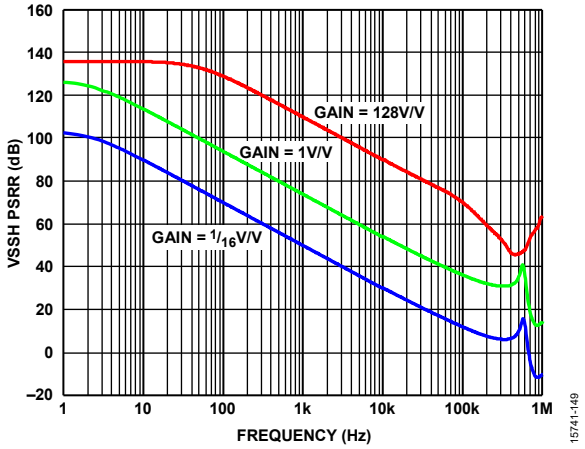


Figure 39. VSSH PSRR vs. Frequency

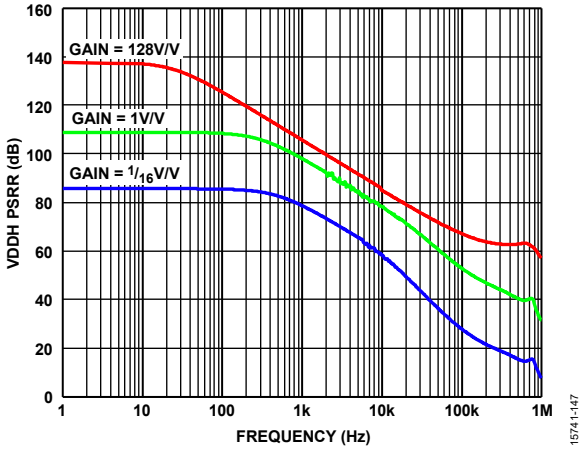


Figure 42. VDDH PSRR vs. Frequency

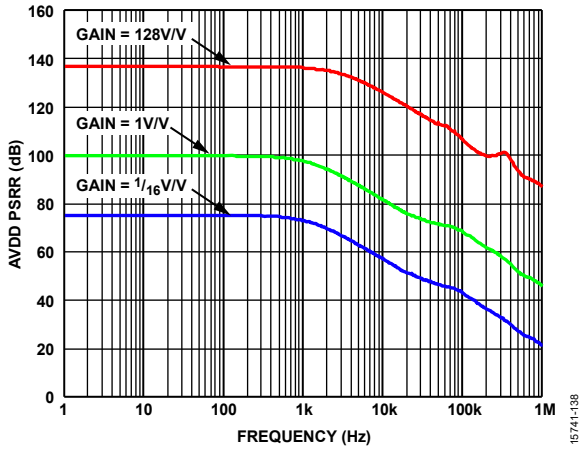


Figure 43. AVDD PSRR vs. Frequency

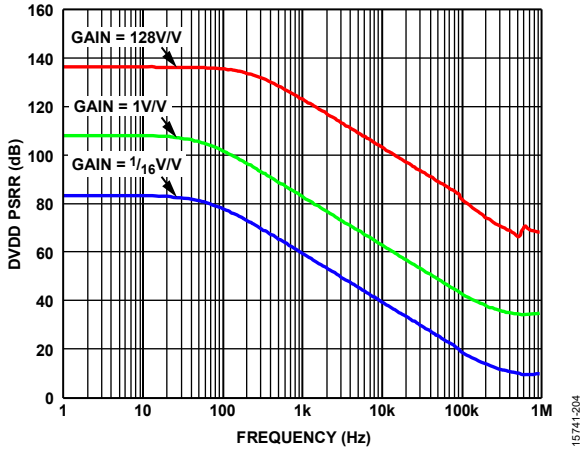


Figure 46. DVDD PSRR vs. Frequency

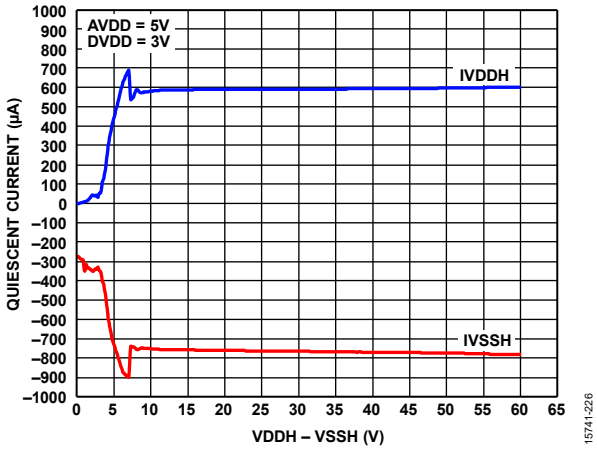


Figure 44. Quiescent Current vs. Supply Voltage (VDDH – VSSH)

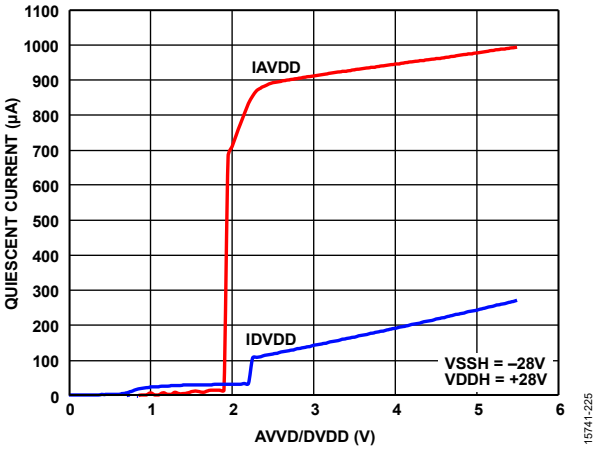


Figure 47. Quiescent Current vs. Supply Voltage (AVDD/DVDD)

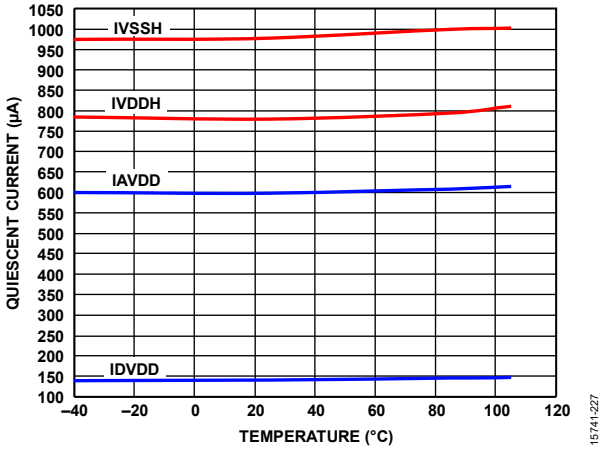


Figure 45. Quiescent Current vs. Temperature

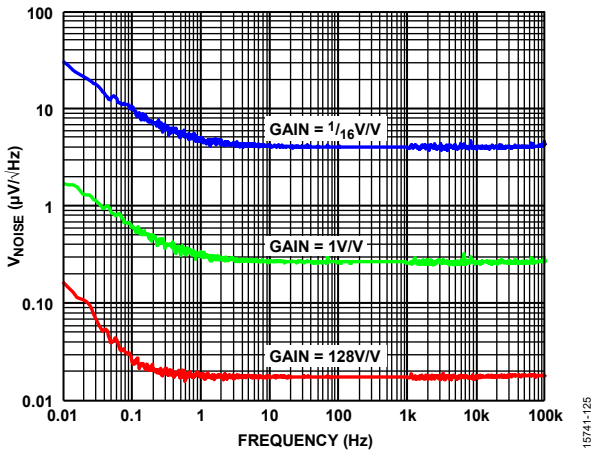


Figure 48. Voltage Noise Spectral Density, RTI

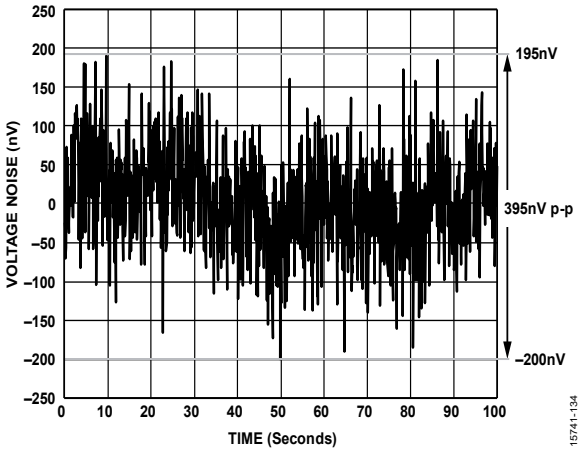


Figure 49. 0.01 Hz to 10 Hz Voltage Noise, RTI (Gain = 128 V/V)

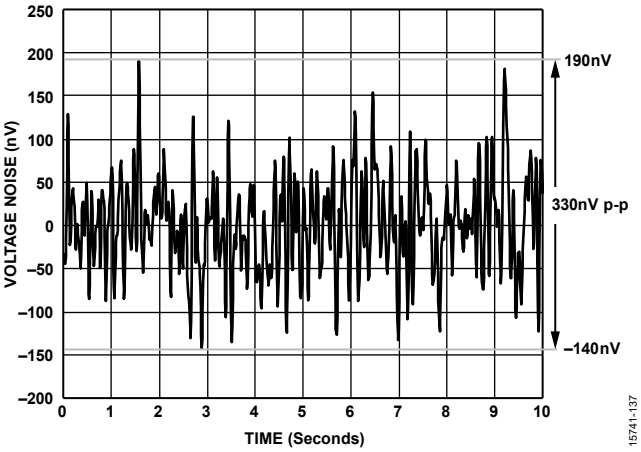


Figure 52. 0.1 Hz to 10 Hz Voltage Noise, RTI (Gain = 128 V/V)

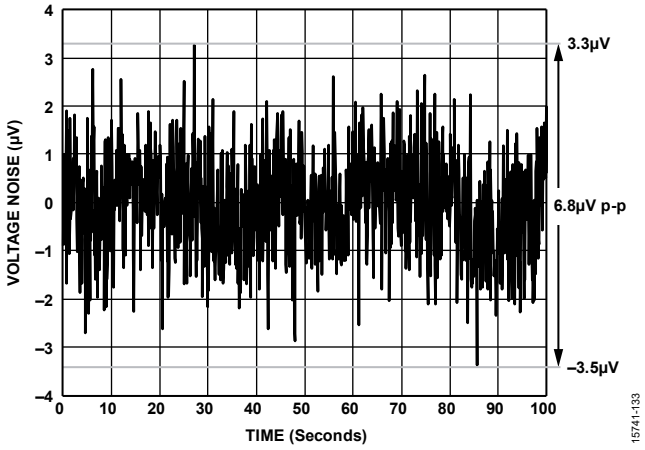


Figure 50. 0.01 Hz to 10 Hz Voltage Noise, RTI (Gain = 1 V/V)

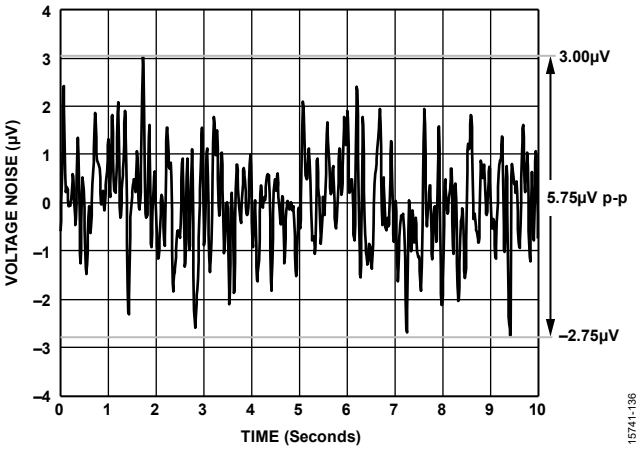


Figure 53. 0.1 Hz to 10 Hz Voltage Noise, RTI (Gain = 1 V/V)

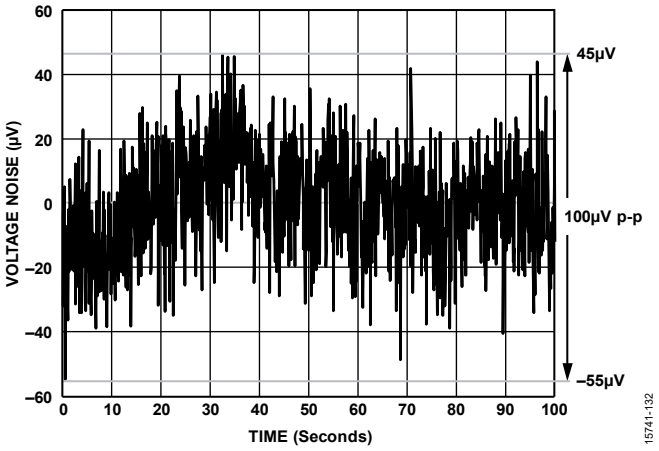


Figure 51. 0.01 Hz to 10 Hz Voltage Noise, RTI (Gain = 1/16 V/V)

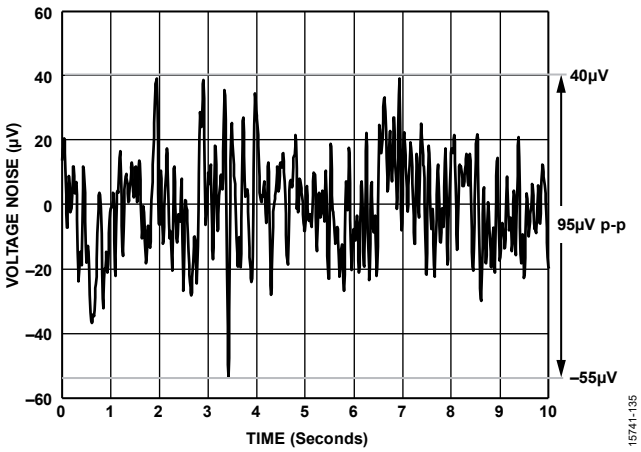


Figure 54. 0.1 Hz to 10 Hz Voltage Noise, RTI (Gain = 1/16 V/V)

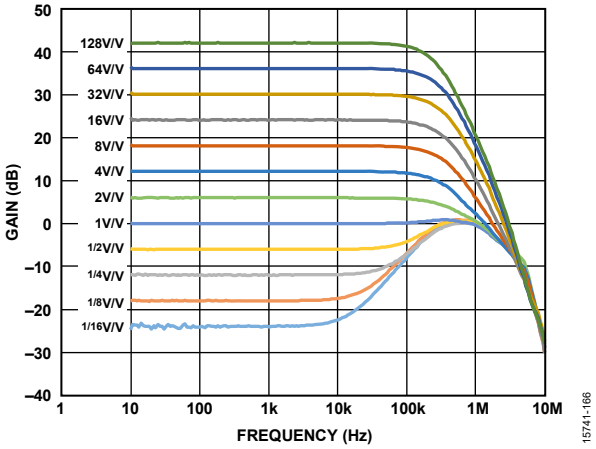


Figure 55. Small Signal Frequency Response

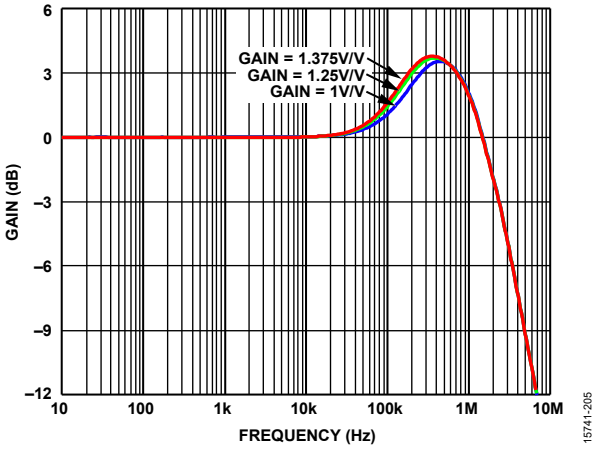


Figure 58. VOCM Small Signal Frequency Response

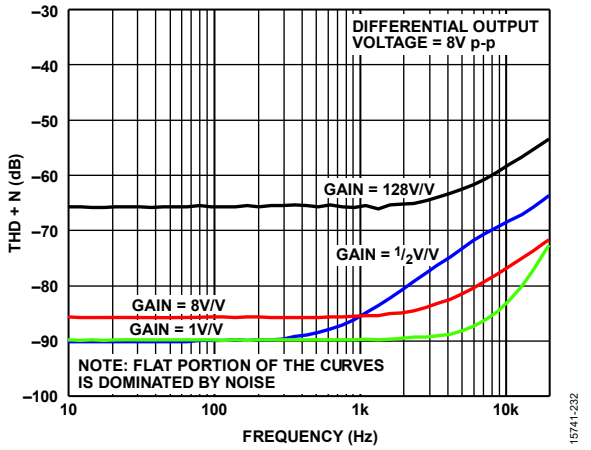


Figure 56. Total Harmonic Distortion Plus Noise (THD + N) vs. Frequency with 100 kHz Filter, Differential Load Resistor ($R_{L, DIFF}$) = 5 kΩ

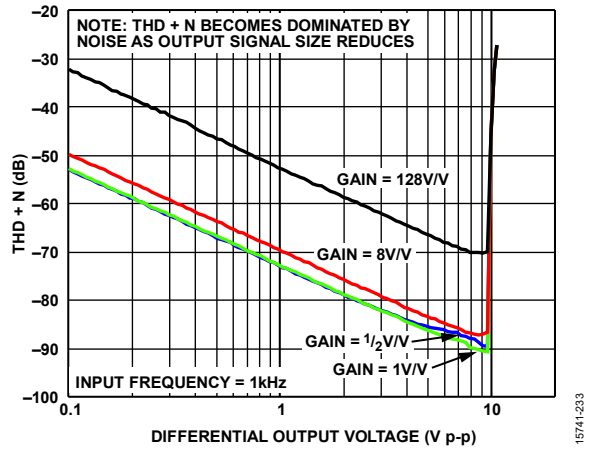


Figure 59. THD + N vs. Differential Output Voltage with 100 kHz Filter, $R_{L, DIFF}$ = 5 kΩ

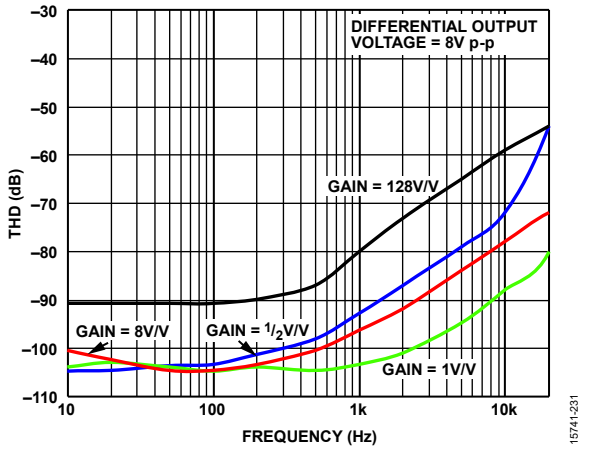


Figure 57. THD vs. Frequency, $R_{L, DIFF}$ = 5 kΩ

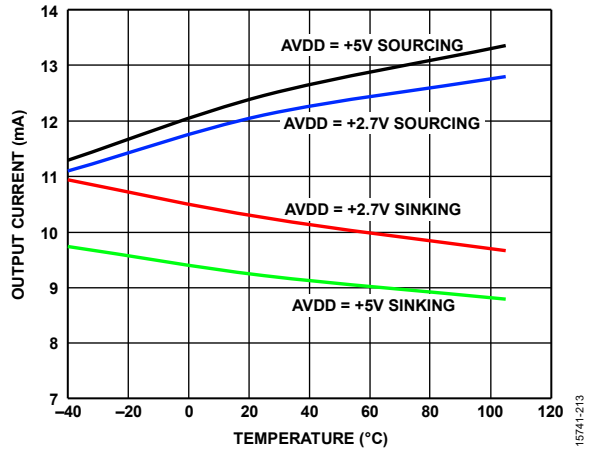


Figure 60. Sinking/Sourcing Short-Circuit Output Current vs. Temperature

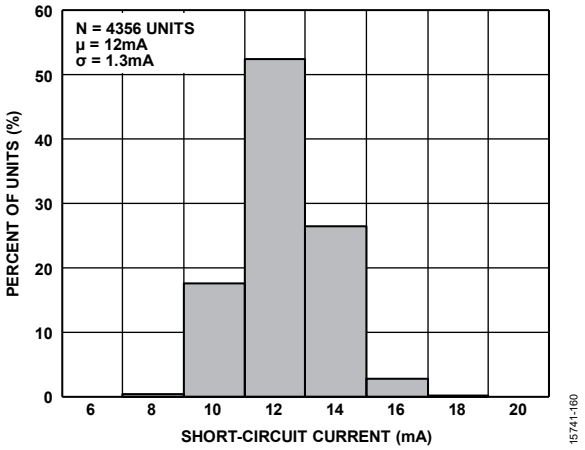


Figure 61. Sourcing Short-Circuit Current Distribution

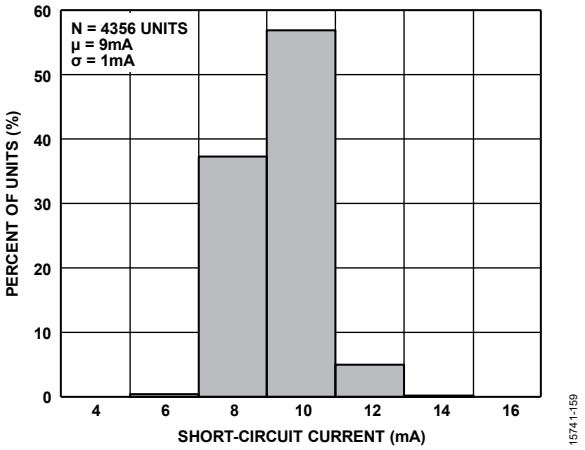


Figure 64. Sinking Short-Circuit Current Distribution

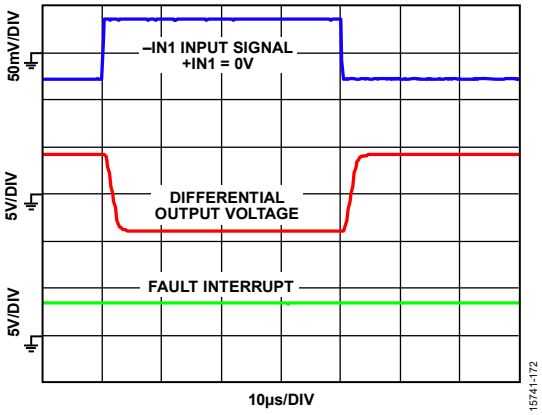


Figure 62. Large Signal Step Response (Gain = 128 V/V)

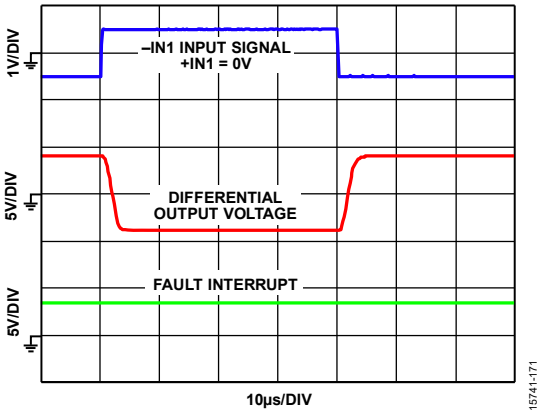


Figure 65. Large Signal Step Response (Gain = 8 V/V)

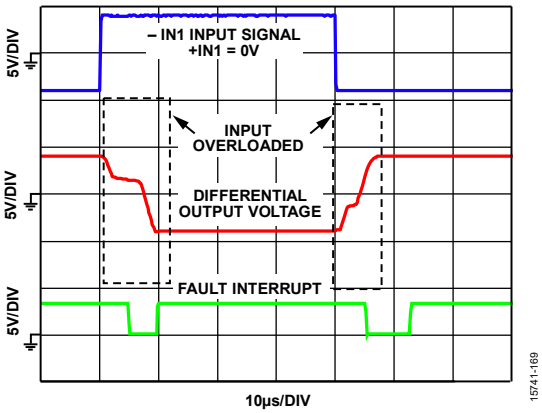


Figure 63. Input Overload Recovery Step Response (Gain = 1 V/V)

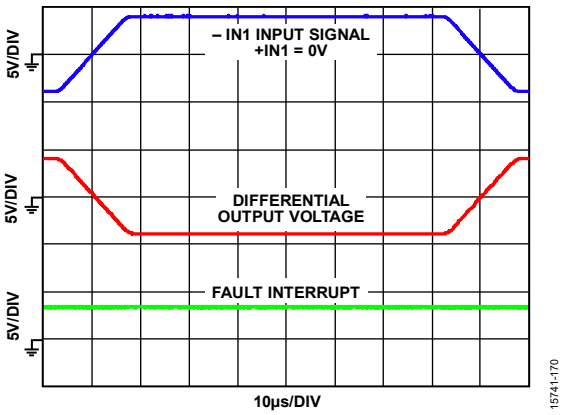


Figure 66. Large Signal Step Response (Gain = 1 V/V)

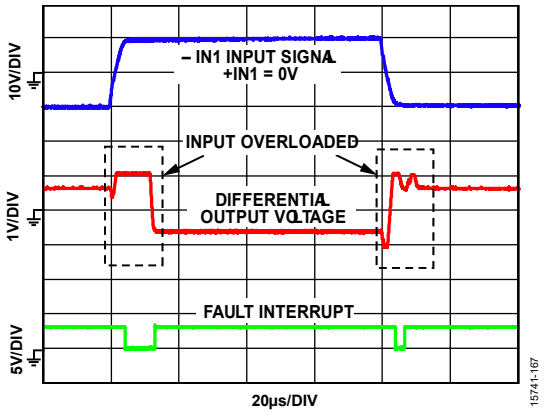


Figure 67. Input Overload Recovery Step Response (Gain = 1/16 V/V)

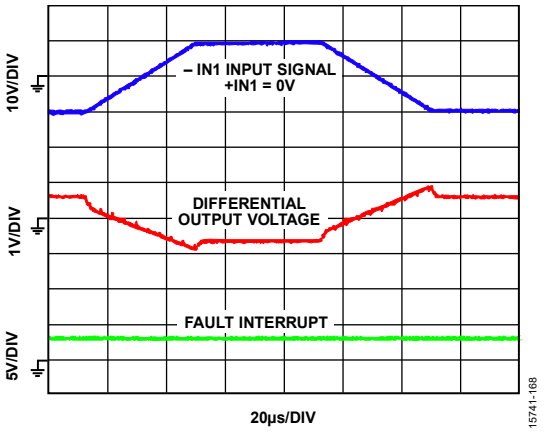


Figure 70. Large Step Response (Gain = 1/16 V/V)

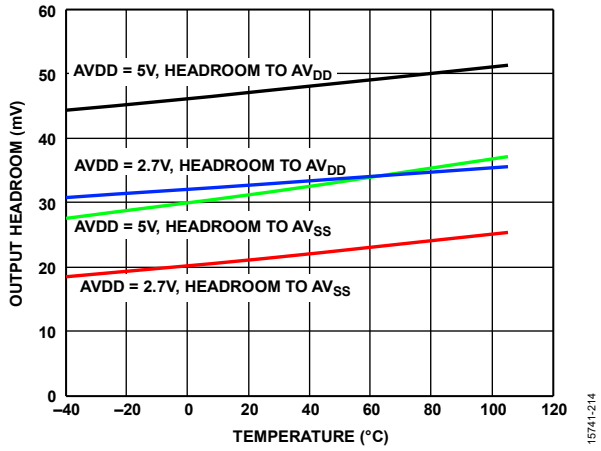


Figure 68. Output Headroom vs. Temperature

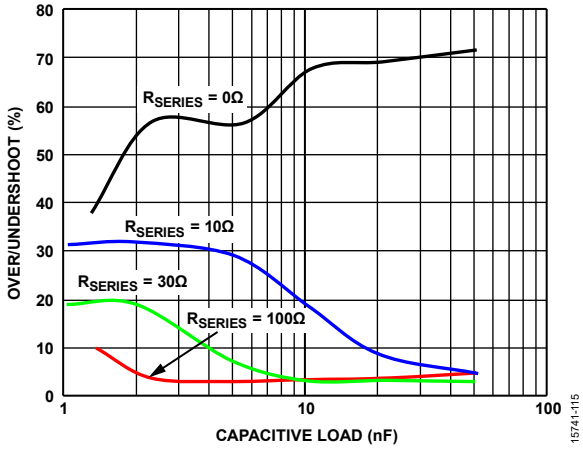


Figure 71. Overshoot/Undershoot vs. Capacitive Load

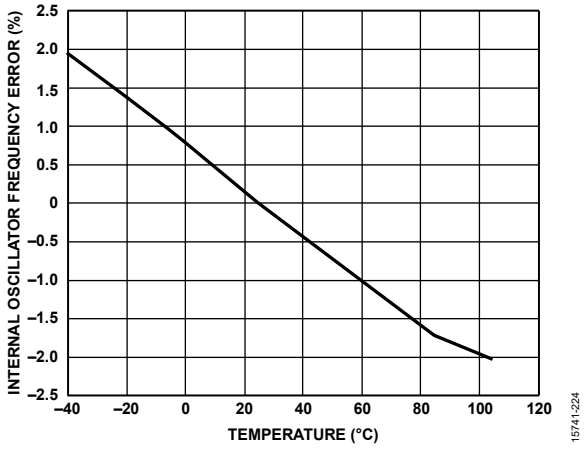


Figure 69. Internal Oscillator Frequency Error vs. Temperature

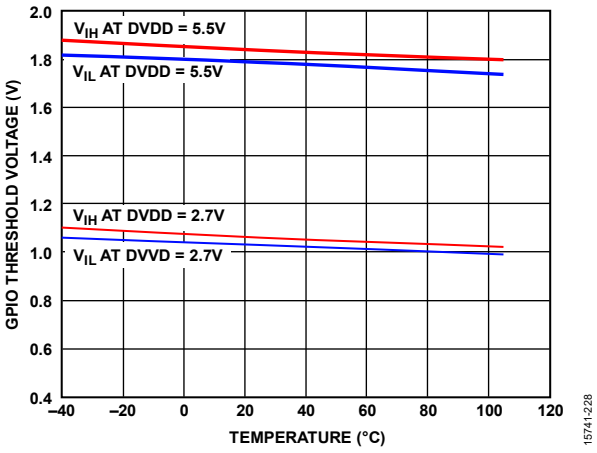


Figure 72. GPIO Threshold Voltage vs. Temperature

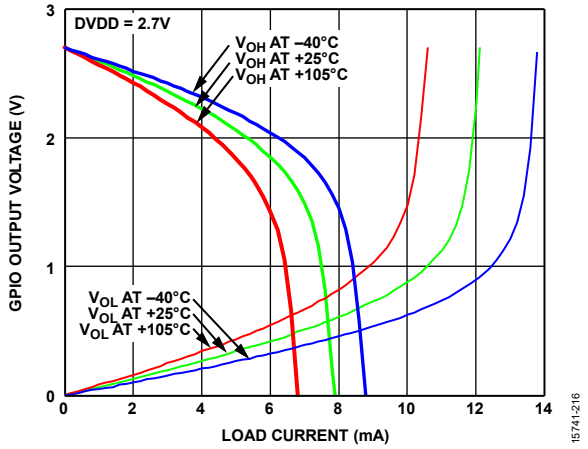


Figure 73. GPIO Output Voltage (V_{OH}/V_{OL}) vs. Load Current for Various Temperatures; DVDD = 2.7 V

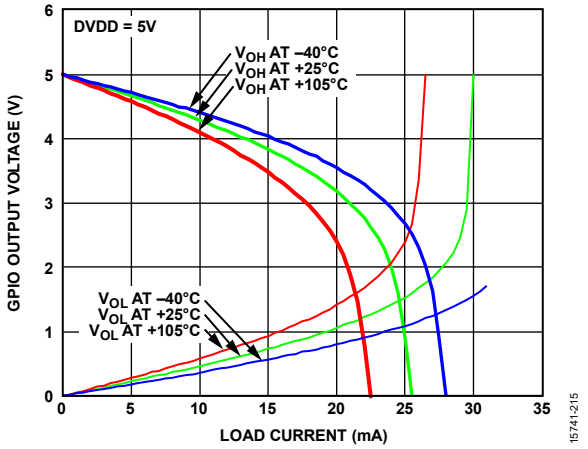


Figure 76. GPIO Output Voltage (V_{OH}/V_{OL}) vs. Load Current for Various Temperatures; DVDD = 5 V

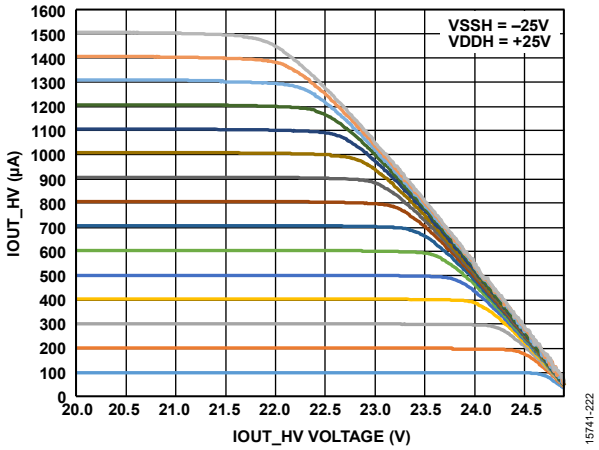


Figure 74. IOUT_HV Current vs. IOUT_HV Output Voltage

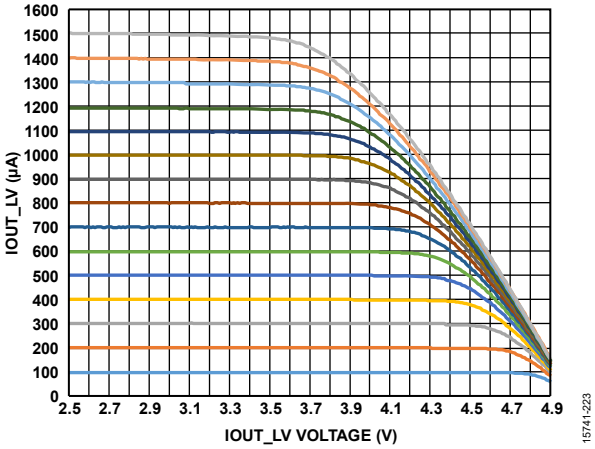


Figure 77. IOUT_LV Current vs. IOUT_LV Output Voltage

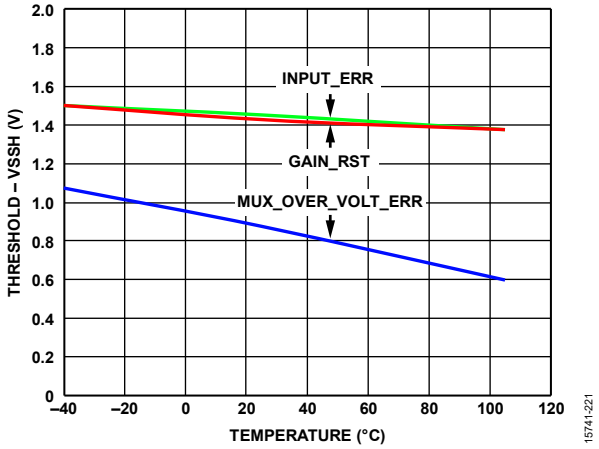


Figure 75. Error Flag Negative Trip Voltage (Threshold – VSSH) vs. Temperature

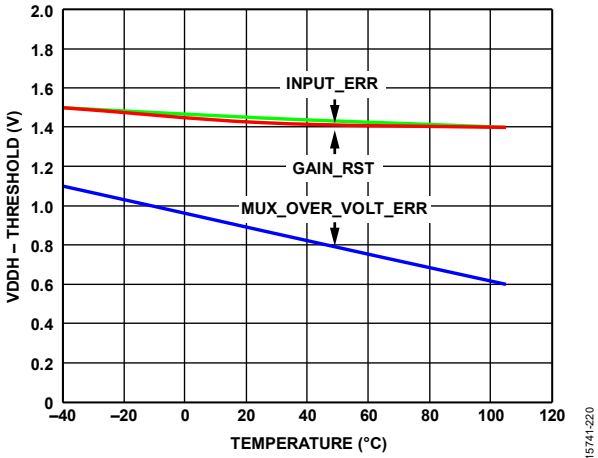


Figure 78. Error Flag Positive Trip Voltage (VDDH – Threshold) vs. Temperature

THEORY OF OPERATION

PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER

The ADA4254 is a direct current mode instrumentation amplifier implemented with zero drift amplifiers. The ADA4254 topology ensures precision operation over temperature. Refer to the simplified architecture shown in Figure 79 to understand the following circuit description.

The input multiplexer connects the inputs to Amplifier A3 and Amplifier A7, which are configured to replicate these input voltages on the R_{IN} input resistor. The A1, A2, A5, and A6 amplifiers are configured to replicate the internal reference voltage, V_{REF}, on R1, R2, R5, and R6, creating four nominally equal dc bias currents in the drains of M1, M2, M5, and M6. Amplifier A4 and Amplifier A8 are configured to replicate the currents in R3 and R7 in the drains of M4 and M8, respectively, forming current mirrors.

When positive voltage is applied to the ADA4254 inputs, a proportional current is conducted by R_{IN}. The drain currents of M3 and M4 increase by this amount, and the drain currents of M7 and M8 reduce by this amount. This portion of the amplifier operates as a transconductance with differential output, each having a gain of $1/R_{IN}$. Output amplifier A9 is configured as a transimpedance amplifier with gain of R_{OUT}. A9 provides a common-mode level shift to the output and produces the differential output voltage ($V_{OUT, DIFF}$) as follows:

$$V_{OUT,\,DIFF} = \frac{(V_{+IN} - V_{-IN}) \times R_{OUT} \times 2}{R_{IN}}$$

where:
V_{+IN} is the positive input voltage.
V_{-IN} is the negative input voltage.

The overall gain of the ADA4254 amplifier is $2 \times R_{OUT}/R_{IN}$. The different gain settings are achieved by internally switching in different values for R_{OUT} and R_{IN}.

The value of R_{IN} can be set to 12 different values via the G3 to G0 bits, resulting in 12 binary weighted input gains. The value of R_{OUT} can also be set to three different values via G4 and G5, resulting in three output scaling gains. Table 6 shows the 36 possible gain configurations, making the ADA4254 versatile when interfacing with a wide selection of sensors and ADCs.

Table 6. Possible Gain Settings

	Output Scaling Gain (V/V)		
Input Gain	**1**	**1.25**	**1.375**
0.0625	0.0625	0.078125	0.085938
0.125	0.125	0.15625	0.171875
0.25	0.25	0.3125	0.34375
0.5	0.5	0.625	0.6875
1	1	1.25	1.375
2	2	2.5	2.75
4	4	5	5.5
8	8	10	11
16	16	20	22
32	32	40	44
64	64	80	88
128	128	160	176

Each amplifier used in the ADA4254 uses a proprietary, zero drift architecture to ensure very low offset voltage, offset voltage drift, and 1/f noise.

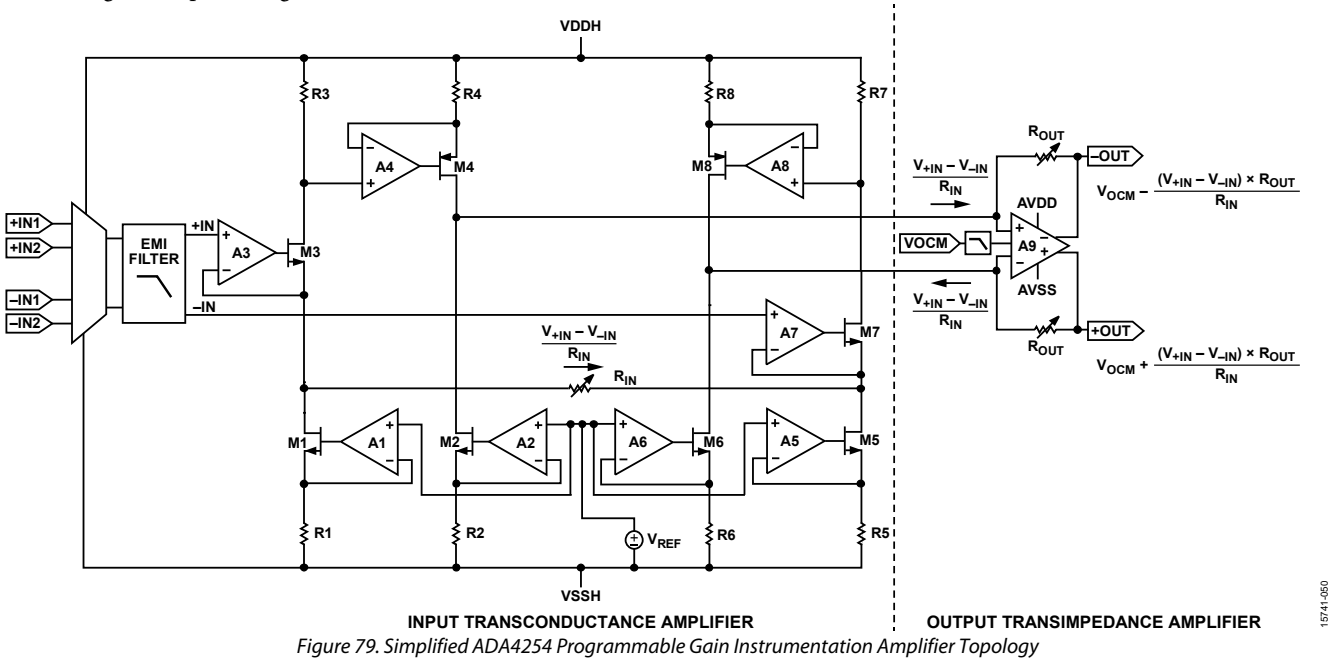


Figure 79. Simplified ADA4254 Programmable Gain Instrumentation Amplifier Topology

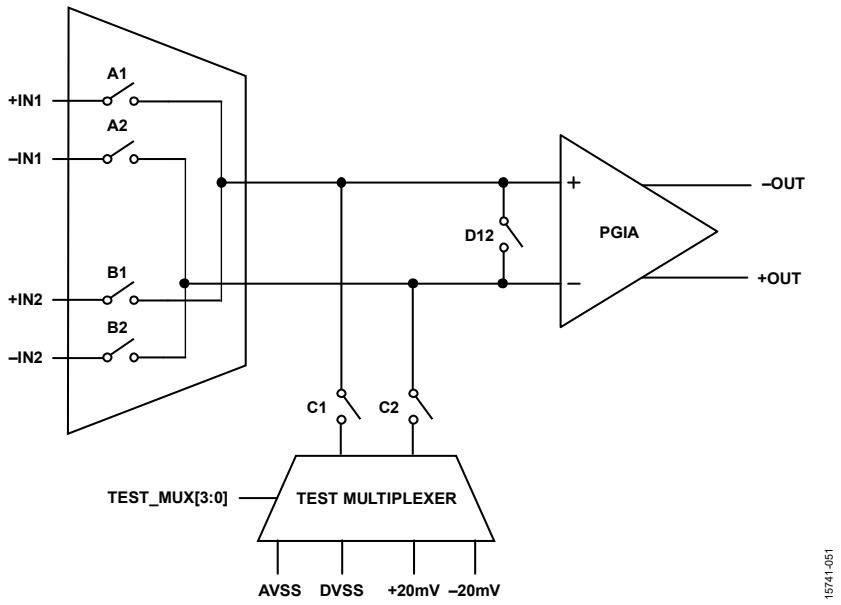


Figure 80. Input Switch Configuration

INPUT MULTIPLEXER

The ADA4254 input multiplexer withstands input voltages up to ±60 V with respect to VSSH, and 60 V differentially. As shown in Figure 80, the multiplexer switches between two sets of inputs and features additional switch functionality on the output of the multiplexer. Input switching is controlled via the INPUT_MUX register. The A1, A2, B1, and B2 switches connect the different inputs to the amplifier. The C1 and C2 switches connect the multiplexer outputs to the test multiplexer. Switch D12 connects both inputs together. The input multiplexer features <140 dB of crosstalk.

If excessive input voltage is detected by the input multiplexer, MUX_OVER_VOLT_ERR in the analog error register trips. When this error flag is set, the multiplexer automatically opens A1, A2, B1, and B2 to protect the input amplifier and input resistor network. This error flag can be disabled by setting MUX_OVER_VOLT_ERR_DIS. By default, both sets of inputs cannot be selected simultaneously. This protection can be overridden via MUX_PROT_DIS.

EMI REDUCTION AND INTERNAL EMI FILTER

In many industrial and data acquisition applications, the ADA4254 amplifies small signals accurately in the presence of large common-mode voltages or high levels of noise. Typically, the sources of these very small signals (in the order of microvolts or millivolts) are sensors that may be a significant distance from the signal conditioning circuit. Although these sensors may be connected to signal conditioning circuitry using shielded or unshielded twisted pair cabling, the cabling may act as an antenna, conveying very high frequency interference directly to the inputs of the ADA4254.

The amplitude and frequency of this high frequency interference can have an adverse effect on the input stage of the instrumentation amplifier due to unwanted dc shift in the input offset voltage of the amplifier. This well known effect is called EMI rectification and is produced when out of band interference is coupled (inductively, capacitively, or via radiation) and rectified by the input transistors of the instrumentation amplifier. These transistors act as high frequency signal detectors, in the same way diodes were used as RF envelope detectors in early radio designs. Regardless of the type of interference or the method by which it is coupled to the circuit, an out of band error signal appears in series with the inputs of the instrumentation amplifier.

To minimize this effect, the ADA4254 has 35 MHz on-chip EMI filters to attenuate high frequencies before interacting with the input transistors. These on-chip filters are well matched due to their monolithic construction, which minimizes degradation in ac CMRR. To reduce any further effect of these out of band signals on the input offset voltage of the ADA4254, an additional external low-pass filter can be used at the inputs. Locate the filter very close to the input pins of the circuit. An effective filter configuration is shown in Figure 81 where three capacitors are added to the ADA4254 inputs. The filter limits the input signal according to the following relationship:

$$Filter\ Frequency_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$Filter\ Frequency_{CM} = \frac{1}{2\pi RC_C}$$

where:
C_D is the differential capacitor and is ≥ 10 C_C.
C_C is the common-mode capacitor.

C_D affects the difference signal. C_C affects the common-mode signal. Any mismatch in R × C_C degrades the ADA4254 CMRR. To avoid inadvertently reducing CMRR bandwidth performance,

ensure that C_C is at least one magnitude smaller than C_D. The effect of mismatched C_C values is reduced with a larger C_D:C_C ratio.

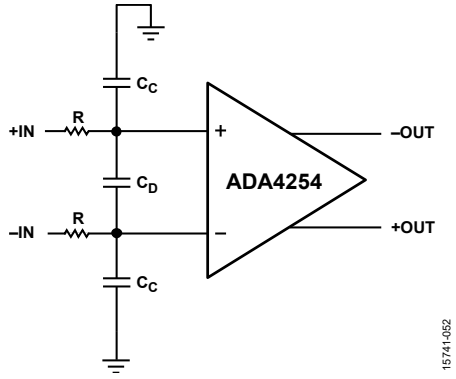


Figure 81. External EMI Filter Improves Noise Rejection

INPUT AMPLIFIER

The ADA4254 input amplifier operates on high voltage power supplies, VDDH and VSSH. The input amplifiers are monitored for clipping due to excessive signal swing. If excessive output swing is detected by an input amplifier (A3 and A7 in Figure 79), the INPUT_ERR flag trips. If INPUT_ERR is tripped for more than 200 µs, the gain settings in the GAIN_MUX register are reset to their default values and the G_RST flag trips. This setup protects the input amplifiers and the input resistor network. The gain reset function can be disabled via the G_RST_DIS bit.

OUTPUT AMPLIFIER

The ADA4254 features a fully differential output amplifier running from dedicated low voltage supplies, AVDD and AVSS. Use AVDD and AVSS in a single-supply configuration. By running the output amplifier on low voltage supplies, circuitry connected to the output of the ADA4254 is inherently protected. The common-mode output voltage is set by the VOCM input voltage. VOCM has a high input impedance and is not biased internally. VOCM also features a 29 MHz EMI filter to minimize EMI interference. Typically, VOCM is biased to midsupply through a voltage divider between AVDD and AVSS to allow the widest swing on the output. The output amplifier can be set to three different scaling gains via G4 or G5: 1 V/V, 1.25 V/V, or 1.375 V/V. On power-up or soft reset, the output amplifier scaling gain defaults to 1 V/V. The output amplifier is monitored for clipping due to excessive signal swing. When the output saturates to either supply, the OUTPUT_ERR error flag trips.

The differential output stage of the ADA4254 allows the device to be directly connected to high precision ADCs, such as the AD7768 and the AD4007. When making such a connection, it is recommended to use a low-pass filter to minimize noise and aliasing, as shown in Figure 82. The LTC6363 is configured as a three-pole, low-pass filter with a cutoff frequency of 40 kHz.

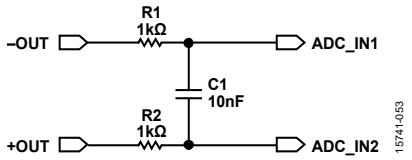


Figure 82. Simple Output Filter Preventing Aliasing and Filters Switching Noise

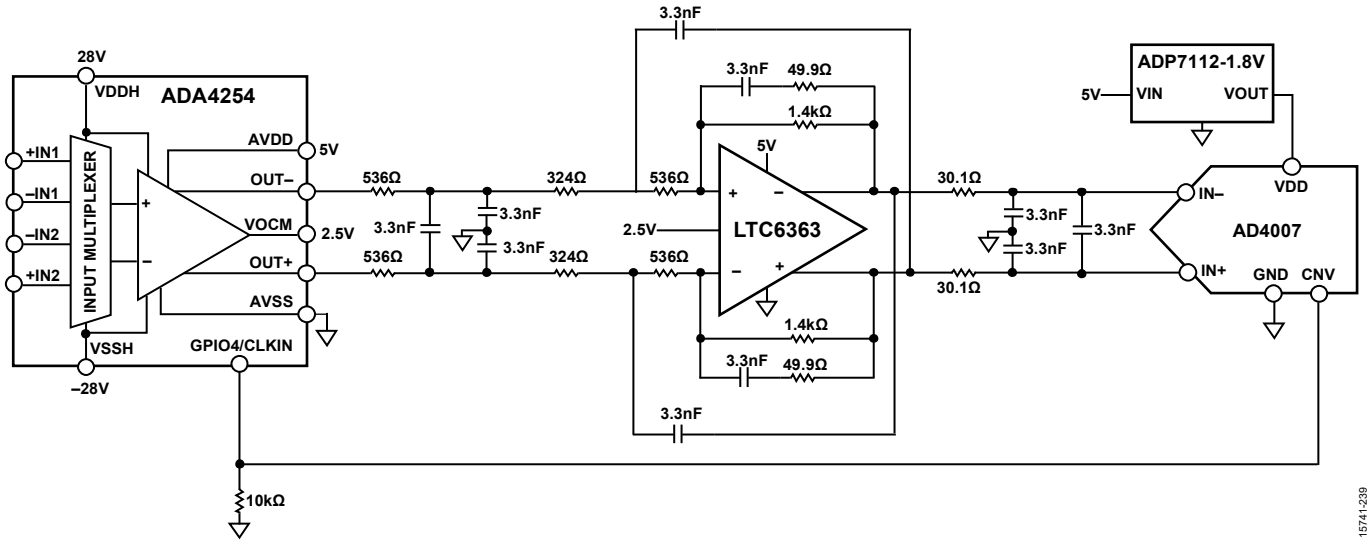


Figure 83. LTC6363 Used as a Low-Pass Filter/Driver

POWER SUPPLIES

The ADA4254 has three supply voltage domains: the high voltage analog input amplifier supply, the low voltage analog output amplifier supply, and the low voltage digital supply.

The high voltage analog supplies, VDDH and VSSH, power the input section of the ADA4254. VSSH is connected to the substrate of the ADA4254. Therefore, VSSH must be connected to the most negative supply voltage in the circuit and VSSH must not exceed AVSS. It is recommended to use a Schottky diode to clamp VSSH to AVSS. The Schottky diode must have a forward bias voltage of 0.3 V or lower at 1 mA and withstand −28 V of reverse voltage. The ADA4254 monitors the VDDH and VSSH supplies to detect if the VDDH or VSSH drops below 8 V and sets the POR_HV flag. VDDH and VSSH must be decoupled with 0.1 µF and 1 µF to ground, as close to the pins as possible.

The low voltage analog output amplifier supply, AVDD and AVSS, powers the output amplifier of the ADA4254. AVSS must be within VSSH − 0.3 V to VSSH + 30 V and VDDH − 30 V to VDDH + 0.3 V. AVDD − AVSS is typically a 5 V single supply, compatible with most high precision ADCs. Use 0.1 µF and 10 µF decoupling capacitors between AVDD and AVSS as close as possible to the AVDD and AVSS supply pins.

The digital supplies, DVDD and DVSS, power the digital circuitry inside the ADA4254. DVSS must be the same potential as AVSS.

Use 0.1 µF and 1 µF decoupling capacitors from DVDD to DVSS as close as possible to the DVDD and DVSS supply pins. Figure 84 shows a typical ADA4254 supply configuration. The recommended decoupling values described in this section are minimum recommendations. Depending on amplifier loading and system noise, higher capacitance values and/or additional lower capacitor values may improve performance.

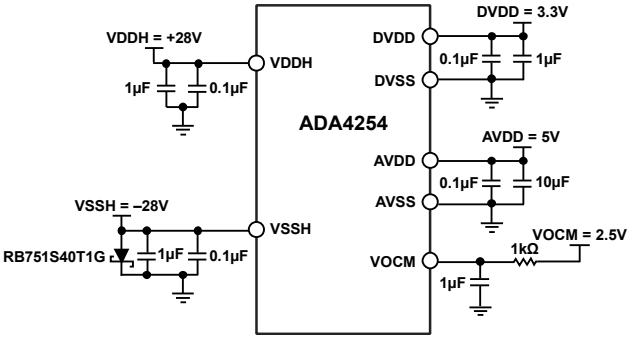


Figure 84. Typical ADA4254 Power Supply Configuration

ESD MAP

Figure 85 shows the various ESD diode paths inside the ADA4254. Figure 85, in conjunction with the Absolute Maximum Ratings section, helps in understanding current paths during power-on and fault conditions.

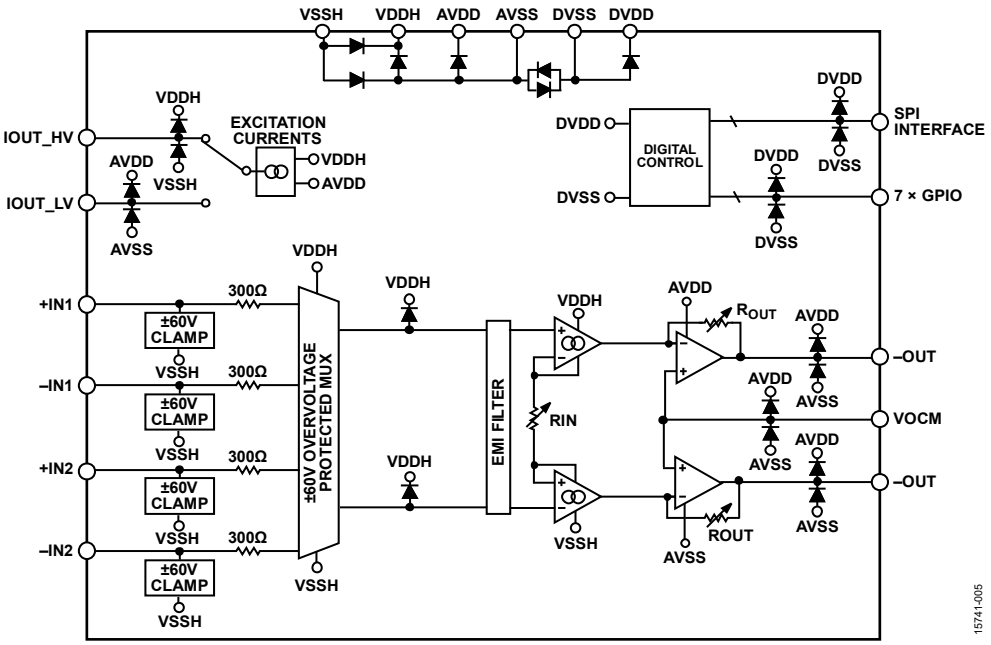


Figure 85. ESD Map

OUTPUT RIPPLE CALIBRATION CONFIGURATION

The amplifiers inside the ADA4254 achieve zero drift by using a technique commonly referred to as chopping. When chopping is used to null the offset of an amplifier, the unchopped offsets are modulated to the frequency at which the chopping is performed. All chopping amplifiers feature this phenomenon, which is commonly referred to as ripple.

The ADA4254 instrumentation amplifier features a proprietary calibration routine that reduces the residual voltage ripple at the output of the ADA4254 by nulling the internal offsets of all amplifiers. This calibration occurs automatically when the ADA4254 is initially powered on, after a POR_HV event, or after a soft reset occurs. Further calibrations can be performed either on a scheduled or triggered basis.

While the ADA4254 is calibrating, SW_A1, SW_A2, SW_B1, and SW_B2 are temporarily opened and the amplifier inputs are internally connected to AVSS through SW_C1 and SW_C2. After a calibration completes, the switches return to their previous states. Two calibration types can be selected via CAL_SEL: full calibration or quick calibration.

A full calibration sequentially calibrates each individual amplifier and fully computes a new calibration code. This calibration takes approximately 85 ms. Full calibration always occurs after power-up, after a POR_HV event, or after a soft reset.

A quick calibration calculates a new calibration code for all amplifiers at the same time. The calibration code of each amplifier is then adjusted by an incremental amount. This type of calibration takes approximately 8 ms.

By default, calibrations only occur after power-up, after a POR_HV event, or after a reset. Additional scheduled calibrations are configured via CAL_EN, or are triggered via the TRIG_CAL bit.

When scheduled calibrations are configured via CAL_EN, the selected calibration type occurs at the rate configured via CAL_EN.

Calibrations can also be manually triggered via TRIG_CAL.

The internal offsets, which are nulled by the ADA4254 calibration routine, can change when the circuit or the environmental conditions change. Changes in temperature, supply voltage, common-mode input voltage, time, and so on, can all cause an increase in output ripple. Recalibrations, either triggered or scheduled, renull internal offsets and reduce residual output ripple.

During a calibration, noise can limit the ability of the ADA4254 to fully null internal offsets and fully reduce the residual output ripple. Proper decoupling and shielding techniques help ensure accurate calibrations. Avoid large input transients during calibrations. Calibrations typically reduce the output ripple to <200 μV rms, but results as high as 5 mV rms can be observed in the presence of noise or input transients. If excessive residual ripple is detected, subsequent calibrations can be performed to reduce the output ripple.

ADC synchronization and simple filtering, either passive or active, are also effective methods in reducing residual output ripple. These techniques are discussed in detail in the External Clock Synchronization section and the Output Amplifier section.

GENERAL-PURPOSE INPUTS/OUTPUTS (GPIOs)

The ADA4254 features several multifunction GPIOs. There are five GPIOs on the TSSOP and seven on the LFCSP package. These GPIOs can be configured to either read a logic input or output a logic signal. A GPIO pin is configured as an input or an output using the GPIO_DIR register. The bit position in the GPIO_DIR register corresponds to the GPIO pin number. For example, the bit at Position 0 controls the GPIO0 direction.

The GPIO_DATA register sets the GPIO output when a GPIO is configured as an output. The GPIO_DATA register also reads the data at the GPIO pin when a GPIO is configured as an input. The bit field position in the GPIO_DATA register corresponds to the GPIO pin number. For example, the bit at Position 0 corresponds to GPIO0.

The ADA4254 GPIOs can be configured to perform additional special functions.

Each GPIO can be configured as an output to extend the chip select signal from the SPI master to other slave devices. This special functionality is referred to as sequential chip select. This special functionality is controlled by the SCS register.

GPIO0 and GPIO1 can also be configured as external multiplexer control signals. This function is enabled in the special function register, SF_CFG. After GPIO0 and GPIO1 are configured as outputs, the EXT_MUX bit field in the GAIN_MUX register controls the state of GPIO0 and GPIO1, allowing the gain and the external mux setting to be modified with one write operation.

GPIO2 can be configured to output a calibration busy signal. This function is enabled via CAL_BUSY_OUT. The calibration busy signal indicates that the ADA4254 is performing a calibration routine. GPIO2 must be configured as an output to use this special function.

GPIO3 can be configured to output a fault interrupt signal. This signal is an OR function of all the analog and digital error indicators found in the ANALOG_ERR and DIGITAL_ERR registers. This function is enabled via FAULT_INT_OUT. GPIO3 must be configured as an output to use this special function.

When configured as an output, GPIO4 can be configured to output the 1 MHz master clock or the 125 kHz chopping clock. This is configured via INT_CLK_OUT and CLK_OUT_SEL. When configured as an input, GPIO4 can also accept an external clock. This function is configured via EXT_CLK_IN.

EXCITATION CURRENTS

The ADA4254 contains two software configurable excitation current sources, IOUT_LV and IOUT_HV. These current sources can be used to excite external circuitry, such as resistive bridges or RTD sensors. IOUT_LV is sourced from AVDD and IOUT_HV is

sourced from VDDH (see Figure 86). Only one of the sources can be on at one time. The source can be selected via EX_CURRENT_SEL.

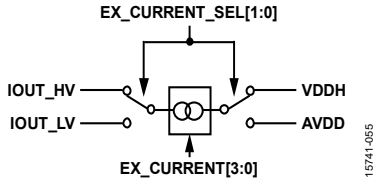


Figure 86. Excitation Current Configuration

The excitation currents can be programmed to a value from 100 µA to 1.5 mA in increments of 100 µA. The current output is controlled via EX_CURRENT.

EXTERNAL CLOCK SYNCHRONIZATION

The ADA4254 uses an internal 1 MHz master clock. The master clock is used to derive the 125 kHz chopping clock used by the internal amplifiers. Either clock can be brought out on the GPIO4 pin to allow synchronization of external systems. Use the following procedure to enable the external clock synchronization feature:

1. Configure GPIO4 as an output by setting Bit 4 in the GPIO_DIR register to 1.
2. Enable the internal oscillator output special function by setting the INT_CLK_OUT bit to 1 and the EXT_CLK_IN bit to 0 in the SF_CFG register.
3. To output the 125 kHz clock, set the CLK_OUT_SEL bit in the SYNC_CFG register to 1. To output the 1 MHz clock, set the CLK_OUT_SEL bit to 0.

The ADA4254 can alternatively be configured to accept an external clock on GPIO4. The ADA4254 allows external clocks ranging from 1 MHz up to 32 MHz. In the case of an external clock that is higher than 1 MHz, the input clock must be divided down to 1 MHz using the internal clock divider. The edge on which the ADA4254 synchronizes can also be configured.

Use the following procedure to configure the ADA4254 to accept an external clock on GPIO4:

1. Configure GPIO4 as an input by setting Bit 4 in the GPIO_DIR register to 0.
2. Set the EXT_CLK_IN bit to 1 and ensure that the INT_CLK_OUT bit is set to 0 in the SF_CFG register.
3. Depending on the frequency of the input clock, configure the internal clock divider value such that the resulting clock is 1 MHz. The internal clock divider value is controlled by the SYNC bits in the SYNC_CFG register.
4. For synchronizing on the rising edge, set the SYNC_POL bit in the SYNC_CFG register to 1. For synchronizing on the falling edge, set SYNC_POL to 0.

To maintain the performance of the ADA4254, the external clock must in the specified range. The quality of the clock used may affect the device performance. Prevent any overshoot or undershoot on the clock used, and provide an equal rise and fall to minimize the impact on the offset voltage.

SEQUENTIAL CHIP SELECT (SCS)

SCS is one of the special functions on the ADA4254 that can be configured on the GPIO pins. This mode simplifies isolation requirements by allowing multiple slave devices to communicate over the SPI using a single host chip select ($\overline{CS}$) line. This communication also supports CRC checksums transparently.

A GPIO is configured for SCS by first setting the GPIO as an output using a GPIO_DIR bit, and then setting the respective bit in the SCS register. Configuring a GPIO for SCS mode is blocked if the GPIO is already configured for another function from the special functions register, SF_CFG.

When using SCS, the $\overline{CS}$ signal from the SPI host controller is provided to the ADA4254 $\overline{CS}$ pin. The serial data input (SDI), serial data output (SDO), and serial clock (SCLK) are shared connections with other SPI devices. The ADA4254 SDO pin supports tristate operation. Slave SDO pins can be directly connected to SDO if the slave pins support tristate operation. For slave devices with SDO pins that do not support tristate operation, an OR gate can be used to combine the SDO signals. If external logic is used to combine SDO lines, pull-down or pull-up resistors are recommended to avoid floating logic gate inputs. Figure 87 and Figure 88 show typical implementations. It is recommended to place pull-up resistors on the GPIOs configured in SCS mode to prevent any unintended communication with slave devices when configuring the ADA4254 in SCS mode.

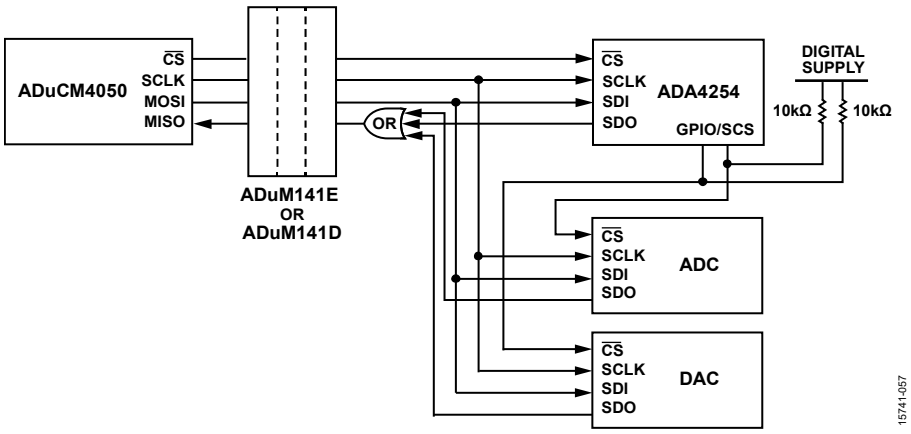


Figure 87. Typical SCS Implementation with Devices Without SDO Tristate Support

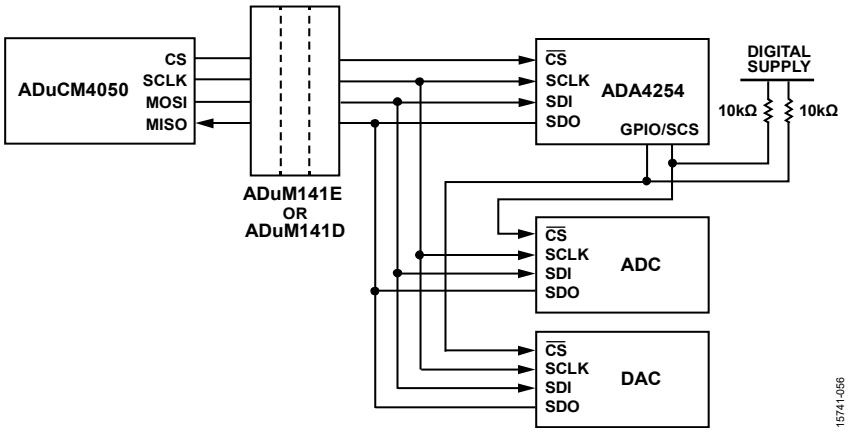


Figure 88. Typical SCS Implementation with All Devices Supporting SDO Tristate

When configured for SCS, communication with the ADA4254 and all slave devices follows a predefined pattern. The first $\overline{CS}$ pulse is passed to the first GPIO that is set up for SCS, effectively communicating with the first slave device. Subsequent $\overline{CS}$ pulses progress through any GPIOs configured for SCS in ascending order. The last $\overline{CS}$ pulse addresses the ADA4254 itself. This pattern repeats until SCS is disabled.

Figure 87 and Figure 88 show the ADA4254 operating in SCS mode with GPIO0 and GPIO1 communicating with two slave devices. GPIO0 is connected to the $\overline{CS}$ line of an ADC. GPIO1 is connected to the $\overline{CS}$ line of a DAC.

In Figure 89, five distinct $\overline{CS}$ pulses can be seen. The first $\overline{CS}$ pulse writes 0x03 to the GPIO_DIR register to configure GPIO0 and GPIO1 as outputs. The second $\overline{CS}$ pulse writes 0x03 to SCS to configure GPIO0 and GPIO1 for SCS. The third $\overline{CS}$ pulse is replicated on GPIO0 and communicates with the first slave device, an ADC in this case. The fourth $\overline{CS}$ pulse is replicated on GPIO1 and communicates with the second slave device, a DAC in this case. The fifth $\overline{CS}$ pulse communicates with the ADA4254 itself. This pattern of communication continues in order of ADC, DAC, and ADA4254 until SCS is changed.

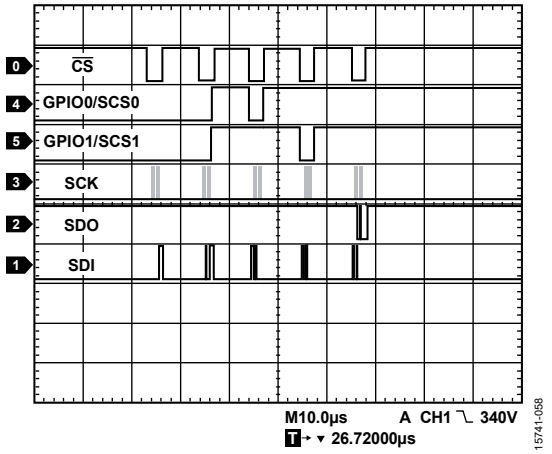


Figure 89. SCS Configuration and Operation with Two Slave Devices

GAIN ERROR CALIBRATION

The ADA4254 includes measured gain errors for all 32 gain combinations, readable from the on-chip ROM. These errors are measured at 25°C and are stored in Register 0x10 through Register 0x27 at the time of production. Using this technology improves gain accuracy by a factor of 5, improving system accuracy and reducing additional calibration requirements.

Each register contains 5 bits. The most significant bit (MSB) represents the polarity of the error, with a setting of 1 indicating a negative polarity and a setting of 0 indicating a positive polarity.

The remaining 4 bits contain the magnitude based on a least significant bit (LSB) of 100 ppm for GAIN_CAL1 through GAIN_CAL12 and 50 ppm for GAIN_CAL13 through GAIN_CAL24.

GAIN_CAL1 through GAIN_CAL12 directly provide the measured gain errors of all 12 gain values with the scaling gain set to 1 V/V. GAIN_CAL13 through GAIN_CAL24 provide additional gain error incurred when using other scalar gains. This is tabulated in Table 7.

Table 7. Gain Calibration Register Contents[1]

Register	Name	G[3:0]	G4	G5	Contents
0x10	GAIN_CAL1	0b0000	0	0	Gain error for G = 1/16 V/V × 1 V/V
0x11	GAIN_CAL2	0b0001	0	0	Gain error for G = 1/8 V/V × 1 V/V
0x12	GAIN_CAL3	0b0010	0	0	Gain error for G = 1/4 V/V × 1 V/V
0x13	GAIN_CAL4	0b0011	0	0	Gain error for G = 1/2 V/V × 1 V/V
0x14	GAIN_CAL5	0b0100	0	0	Gain error for G = 1 V/V × 1 V/V
0x15	GAIN_CAL6	0b0101	0	0	Gain error for G = 2 V/V × 1 V/V
0x16	GAIN_CAL7	0b0110	0	0	Gain error for G = 4 V/V × 1 V/V
0x17	GAIN_CAL8	0b0111	0	0	Gain error for G = 8 V/V × 1 V/V
0x18	GAIN_CAL9	0b1000	0	0	Gain error for G = 16 V/V × 1 V/V
0x19	GAIN_CAL10	0b1001	0	0	Gain error for G = 32 V/V × 1 V/V
0x1A	GAIN_CAL11	0b1010	0	0	Gain error for G = 64 V/V × 1 V/V
0x1B	GAIN_CAL12	0b1011	0	0	Gain error for G = 128 V/V × 1 V/V
0x1C	GAIN_CAL13	0b000x	1	X	Additional gain error for G = 1/16 V/V × 1.375 V/V or G = 1/8 V/V × 1.375 V/V
0x1D	GAIN_CAL14	0b001x	1	X	Additional gain error for G = 1/4 V/V × 1.375 V/V or G = 1/2 V/V × 1.375 V/V
0x1E	GAIN_CAL15	0b010x	1	X	Additional gain error for G = 1 V/V × 1.375 V/V or G = 2 V/V × 1.375 V/V
0x1F	GAIN_CAL16	0b011x	1	X	Additional gain error for G = 4 V/V × 1.375 V/V or G = 8 V/V × 1.375 V/V
0x20	GAIN_CAL17	0b100x	1	X	Additional gain error for G = 16 V/V × 1.375 V/V or G = 32 V/V × 1.375 V/V
0x21	GAIN_CAL18	0b101x	1	X	Additional gain error for G = 64 V/V × 1.375 V/V or G = 128 V/V × 1.375 V/V
0x22	GAIN_CAL19	0b000x	0	1	Additional gain error for G = 1/16 V/V × 1.25 V/V or G = 1/8 V/V × 1.25 V/V
0x23	GAIN_CAL20	0b001x	0	1	Additional gain error for G = 1/4 V/V × 1.25 V/V or G = 1/2 V/V × 1.25 V/V
0x24	GAIN_CAL21	0b010x	0	1	Additional gain error for G = 1 V/V × 1.25 V/V or G = 2 V/V × 1.25 V/V
0x25	GAIN_CAL22	0b011x	0	1	Additional gain error for G = 4 V/V × 1.25 V/V or G = 8 V/V × 1.25 V/V
0x26	GAIN_CAL23	0b100x	0	1	Additional gain error for G = 16 V/V × 1.25 V/V or G = 32 V/V × 1.25 V/V
0x27	GAIN_CAL24	0b101x	0	1	Additional gain error for G = 64 V/V × 1.25 V/V or G = 128 V/V × 1.25 V/V

[1] X means don't care.

For all gains using 1 V/V scalar, calculate the gain error using the following equation:

Gain Error = ((−1) × *GAIN_CALx, Bit 4* + (100) × *GAIN_CALx, Bits[3:0]*) (ppm)

For all gain values using 1.375 V/V or 1.25 V/V scalars, an additional gain error (GE') must be added, using this equation:

GE' = *Gain Error* + ((−1) × *GAIN_CALx, Bit 4* + (50) × *GAIN_CALx, Bits[3:0]*) (ppm)

For example, assume that the ADA4254 is set to a gain of 32 V/V and a scaling gain of 1.375 V/V. To calculate the stored gain error, read the gain error stored in the GAIN_CAL10 register and calculate the error in ppm. In this example, assume this readback is 10101, corresponding to a gain error of −500 ppm.

Then, read the additional gain error stored in GAIN_CAL17 and calculate the error in ppm. In this example, assume this readback is 00010, corresponding to an additional gain error of 100 ppm. The two errors are added to give a total gain error of −400 ppm.

WIRE BREAK DETECTION

The ADA4254 contains two programmable current sources that can be configured to 0.25 µA, 2 µA, 4 µA, or 16 µA via WB_CURRENT. Both currents are conducted from VDDH. These currents, in conjunction with the on-chip comparators, enable continuity testing on the ADA4254 inputs.

The currents are switched to the amplifier inputs using F1 and F2, as shown in Figure 90. The voltage to which these currents bias the amplifier inputs is monitored internally by the ADA4254. When this voltage is within 4 V of VDDH, the WB_ERR flag trips.

When F1 or F2 are closed, the amplifier gain settings in the GAIN_MUX register are temporarily overridden to the default values to avoid saturating the amplifier output in the event of an open circuit input. Reads of the GAIN_MUX register during this time do not reflect this. When F1 and F2 are open, the GAIN_MUX values automatically return to the previous values. This override can be disabled via WB_G_RST_DIS.

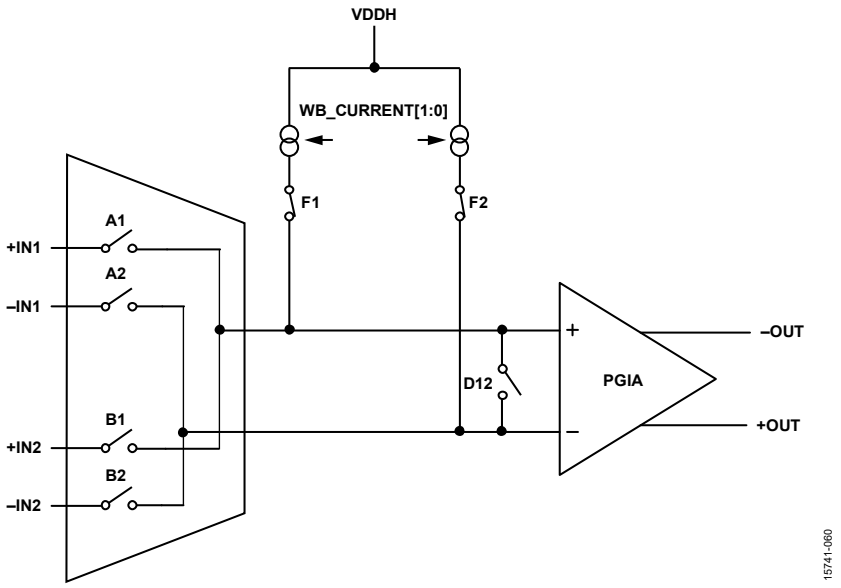


Figure 90. Wire Break Current Connectivity

TEST MULTIPLEXER

The ADA4254 contains an internal test multiplexer, as shown in Figure 91, that connects the inputs of the ADA4254 to useful voltages. To use the test multiplexer, the C1 and C2 switches must be closed. These switches are controlled using the INPUT_MUX register. It is recommended that the input multiplexer be disconnected from any external inputs by opening the A1, A2, B1, and B2 switches.

The TEST_MUX bits in the TEST_MUX register control the test multiplexer. The test multiplexer can be configured in three different states, as follows:

- In the default state, the test multiplexer connects the ADA4254 inputs to AVSS. This configuration can be used during a full system calibration to null out errors, such as offset voltage.
- The test multiplexer can connect the noninverting input to DVSS and the inverting input to AVSS, or vice versa. This configuration can be used to detect any voltage difference between AVSS and DVSS, which indicates poor connection.
- The test multiplexer can also provide a 20 mV or −20 mV differential signal to the inputs of the ADA4254. This configuration can be used to verify the gain setting of the ADA4254 and the PGIA functionality without applying an external signal.

EXTERNAL MUX CONTROL

The ADA4254 is able to configure GPIO0 and GPIO1 to control an external multiplexer. Writes to the EXT_MUX bits in the GAIN_MUX register set the state of GPIO0 and GPIO1, which in turn controls an external multiplexer. This setup allows amplifier gain and external multiplexer settings to be configured with a single SPI write, avoiding overload conditions. The external mux special function can be configured via EXT_MUX_EN and setting GPIO0 and GPIO1 to outputs, as shown in Figure 92.

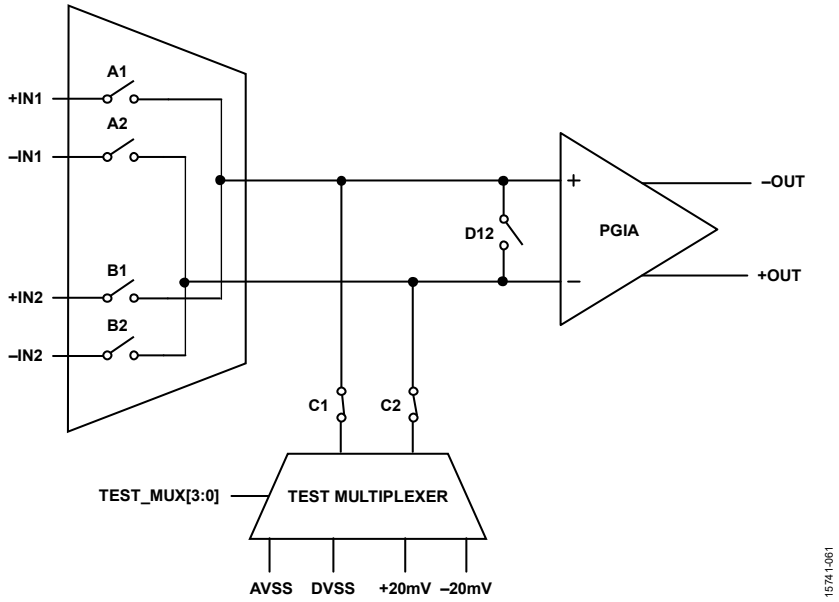


Figure 91. Text Multiplexer Connectivity

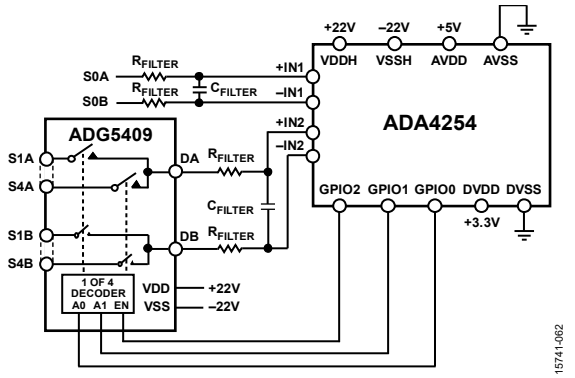


Figure 92. External Multiplexer Control Example

DIGITAL INTERFACE

SPI INTERFACE

The ADA4254 features a 4-wire SPI interface. This interface operates in SPI Mode 0 and can be operated with $\overline{CS}$ tied low. In SPI Mode 0, SCLK idles low, the falling edge of SCLK is the driving edge, and the rising edge of SCLK is the sampling edge. This setup means that data is clocked out on the falling (driving) edge and data is clocked in on the rising (sampling) edge.

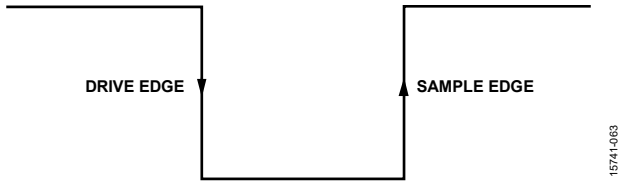


Figure 93. SPI Mode 0 SCLK Edges

ACCESSING THE ADA4254 REGISTER MAP

The ADA4254 SPI interface uses 16-bit instructions, plus an optional 8-bit CRC checksum. Each instruction contains a read/write bit, a 7-bit address, 8 bits of data, and an 8-bit CRC checksum if the SPI_CRC_ERR bit is configured.

Table 8. ADA4254 Instruction Format

RW	ADDR[6:0]	DATA[7:0]	CRC[7:0]

RW determines whether a read or write operation is performed (1 means read and 0 means write). ADDR[6:0] is the register address being read from or written to. RW and the ADDR[6:0] together are referred to as an 8-bit command. For write operations, DATA[7:0] is the data being written and CRC[7:0] is a user provided checksum for that data.

The ADA4254 internal address counter is automatically incremented after each read/write operation, allowing a continuous read/write mode. After an initial read operation, if $\overline{CS}$ stays low, the next 8 SCLK pulses read back the contents of the next register address. After an initial write operation, if $\overline{CS}$ stays low, the next 8 SCLK pulses load the data on SDI to the next register address.

CHECKSUM PROTECTION

The ADA4254 features a checksum mode that can be used to improve interface robustness. Using the checksum ensures that only valid data is written to a register and allows data read from a register to be validated. If an error occurs during a register write, SPI_CRC_ERR trips and no data is written. To ensure that a register write is successful, the register contents can be read, and the checksum can be verified.

For CRC checksum calculations, the following polynomial is always used:

$$x^8 + x^2 + x + 1$$

SPI_CRC_ERR_DIS enables and disables this checksum. The 8-bit checksum is appended to the end of each read and write transaction. The checksum calculation for the write transaction is calculated using the 8-bit command word and the 8-bit data. For a read transaction, the checksum is calculated using the command word and the 8-bit data output. Figure 94 and Figure 95 show SPI write and read transactions, respectively.

In continuous write mode, the first write command CRC is calculated as described previously in this section. Subsequent CRCs are clocked in after every register data. CRC in continuous write mode is calculated based on the register value it is associated with. In continuous read mode, the first read command CRC is calculated as described previously. Subsequent CRCs are clocked out after every register data. CRC in continuous read mode is calculated based only on the register value it is associated with. Figure 96 and Figure 97 show SPI continuous write and read transactions, respectively.

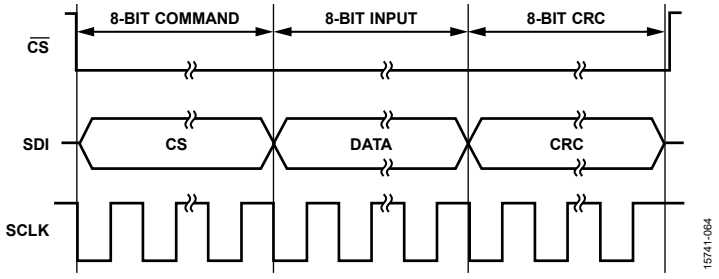


Figure 94. Writing to a Register with CRC

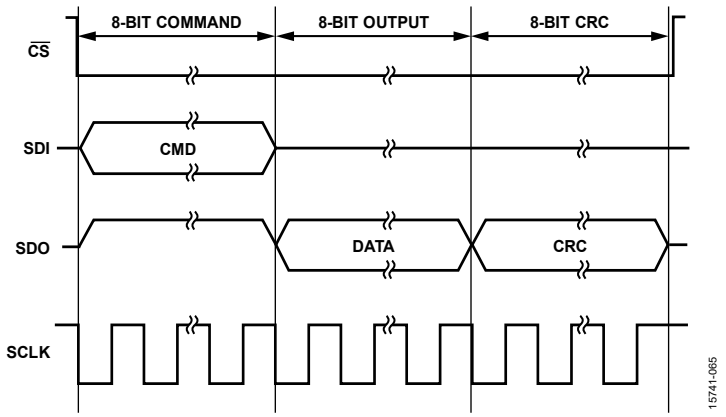


Figure 95. Reading from a Register with CRC

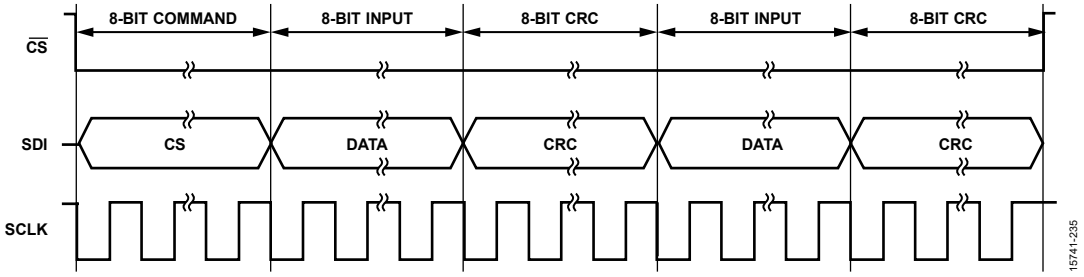


Figure 96. Continuous Write Mode with CRC

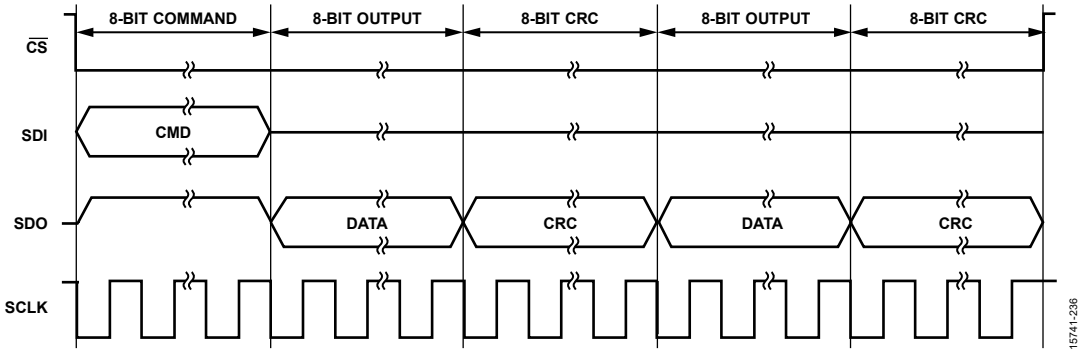


Figure 97. Continuous Read Mode with CRC

CRC CALCULATION

The checksum, which is 8 bits wide, is generated using the following polynomial (with a seed of 0x00):

$x^8 + x^2 + x + 1$ (0b100000111)

To generate the checksum, the data is left shifted by 8 bits to create a number ending in eight Logic 0s. The polynomial is aligned so that its MSB is adjacent to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process is repeated until the original data is reduced to a value less than the polynomial. This is the 8-bit checksum.

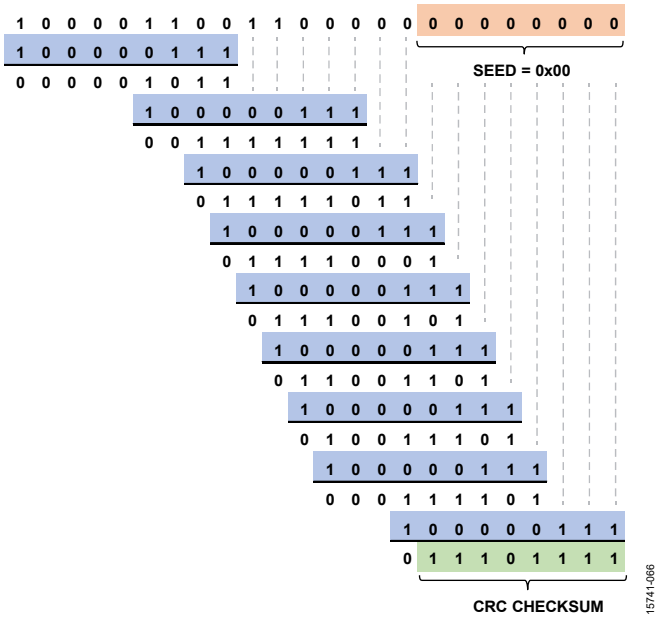


Figure 98. Calculating a CRC Checksum

MEMORY MAP CHECKSUM PROTECTION

For added robustness, a CRC calculation is performed on the on-chip registers as well. Register 0x03, Register 0x04, and Register 0x05 are not included in this check because the contents of these registers change, independent of SPI writes. The CRC is performed at a rate of 15.26 Hz. Each time the register map is changed using an SPI write, the CRC is recalculated.

The memory map CRC function is enabled by default. It can be disabled via MM_CRC_ERR_DIS. If an error occurs, MM_CRC_ERR trips.

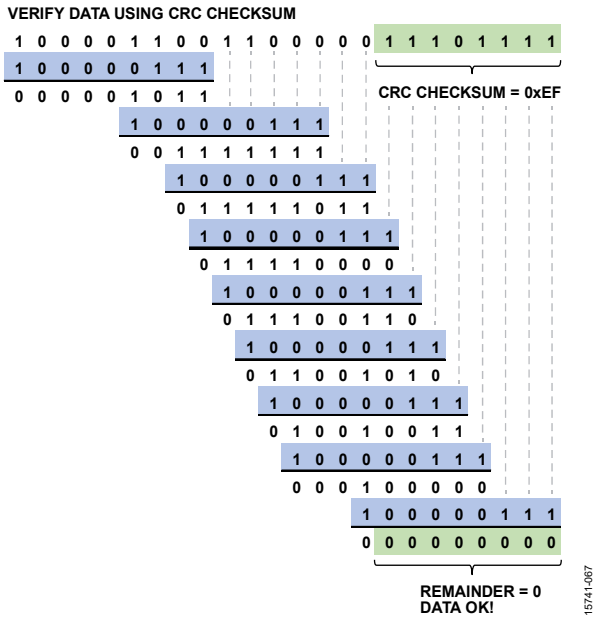


Figure 99. Verifying Data with a CRC Checksum

READ-ONLY MEMORY (ROM) CHECKSUM PROTECTION

On power-up, all fuse registers are set to the default values. These default values are held in ROM. For added robustness, a CRC calculation is performed on the ROM contents as well. This CRC check is performed on power-up. The ROM CRC function is enabled by default. It can be disabled via ROM_CRC_ERR_DIS. If an error occurs, the ROM_CRC_ERR trips.

SPI READ/WRITE ERROR DETECTION

The ADA4254 can detect if an invalid register is being addressed. A read or write to an invalid address trips SPI_RW_ERR. SPI_RW_ERR is enabled by default. It can be disabled via SPI_RW_ERR_DIS.

SPI COMMAND LENGTH ERROR DETECTION

When communicating with the ADA4254, the number of clock edges on SCLK is monitored to ensure that, when $\overline{CS}$ returns high, the total number of clock edges received is divisible by 8. If the number of SCLK edges is insufficient or in excess, SPI_SCLK_CNT_ERR trips. The SPI_SCLK_CNT_ERR is enabled by default. It can be disabled via SPI_SCLK_CNT_ERR_DIS.

APPLICATIONS INFORMATION

INPUT AND OUTPUT OFFSET VOLTAGE AND NOISE

The offset voltage of the ADA4254 has two main components: the input offset voltage due to the input amplifiers and the output offset due to the output amplifier. The total offset voltage RTI is found by dividing the output offset by the programmed gain and adding to the input offset voltage. At high gains the input offset voltage dominates, whereas at low gains the output offset voltage dominates. The total offset voltage is

$$Total\ Input\ Offset\ Voltage\ (RTI) = V_{OSI} + (V_{OSO}/GAIN)$$

$$Total\ Output\ Offset\ Voltage\ (Referred\ to\ Output\ (RTO)) = V_{OSI} \times Gain + V_{OSO}$$

The preceding equations can also be used to calculate the offset drift in a similar manner.

The ADA4254 has extremely low input offset voltage long-term drift, as shown in Figure 100. This high level of stability is due to the zero drift architecture of the ADA4254 amplifiers. This testing is performed at 25°C with the ADA4254 devices submerged in an oil bath.

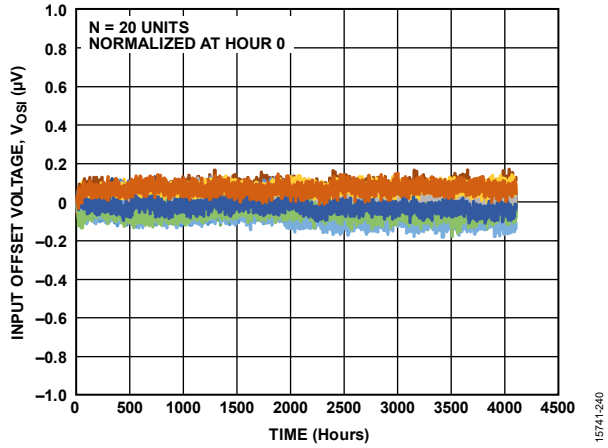


Figure 100. Input Offset Voltage Long-Term Drift

The noise of the ADA4254 behaves similarly to the voltage offset. There are two components: the input voltage noise due to the input amplifiers and the output voltage noise due to the output amplifiers. The total noise RTI is found by dividing the output voltage noise by the programmed gain and root-sum-squaring with the input voltage noise. At high gains the input voltage noise dominates, whereas at low gains the output voltage noise dominates. The total voltage noise is

$$Total\ Input\ Voltage\ Noise\ (RTI) = \sqrt{e_{ni}^{\ 2} + \left(\frac{e_{no}}{Gain}\right)^2}$$

$$Total\ Output\ Voltage\ Noise\ (RTO) = \sqrt{(e_{ni} \times Gain)^2 + (e_{no})^2}$$

ADC CLOCK SYNCHRONIZATION

The ADA4254 incorporates several clock synchronization features that allow the internal clock to be synchronized with other circuitry, such as an ADC. Synchronizing the system filters residual ripple due to the internal chopping of the ADA4254. When using these synchronization features, GPIO4 is configured to accept an external clock signal or output one of the internal clock signals.

When an external clock is provided to the AD4254, an on-chip clock divider is configured via SYNC to achieve a nominal 1 MHz clock. The 1 MHz clock is further divided by 8 to 125 kHz and controls the device chopping. The chopping clock edges can be configured to coincide with either the rising or falling edges of the provided clock via SYNC_POL. This configuration is recommended for ADC synchronization.

Alternatively, the internal clock can be output to GPIO4 so that other circuits can use it. Either 1 MHz or 125 kHz can be selected via CLK_OUT_SEL.

When ADA4254 is driving the AD4007 1 MSPS successive approximation register (SAR) ADC as shown in Figure 101, the recommended configuration is to provide the convert signal to the ADA4254 as a clock input. In this case, SYNC is set to 0b000 because the CNV period is 1 µs. Set SYNC_POL to 1 to synchronize the chopping clock to the rising edge of the CNV signal. When configured in this way, the output of the ADA4254 has the maximum time to settle after a chopping edge and chopping edges do not occur during the ADC conversion phase. It is recommended to enable the high-Z mode of the AD4007 to maximize system performance.

When the ADA4254 is driving the AD7768 Σ-Δ ADC as shown in Figure 102, the recommended configuration is to provide the internal 32 MHz clock of the AD7768 to the ADA4254 as a clock input. In this case, SYNC is set to 0b101 to divide 32 MHz down to 1 MHz for the ADA4254. The SYNC setting has no impact on performance with Σ-Δ converters due to the way the converters operate internally. When driving the AD7768 directly with the ADA4254, enable the internal buffers of the AD7768. Alternatively, a dedicated ADC driver/amplifier can be configured between the ADA4254 and the AD7768.

In both configurations, it is recommended that two reads from the M_CLK_CNT register are performed to ensure that the master clock counter is incrementing, indicating that the ADA4254 is receiving an external clock.

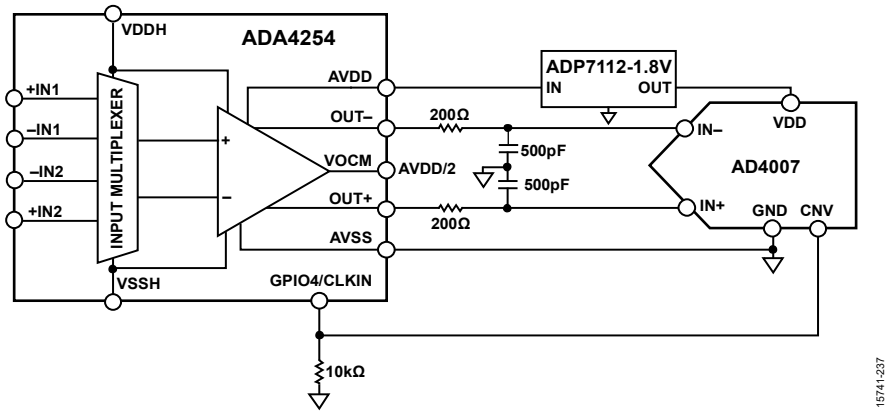


Figure 101. Clock Synchronization with the AD4007

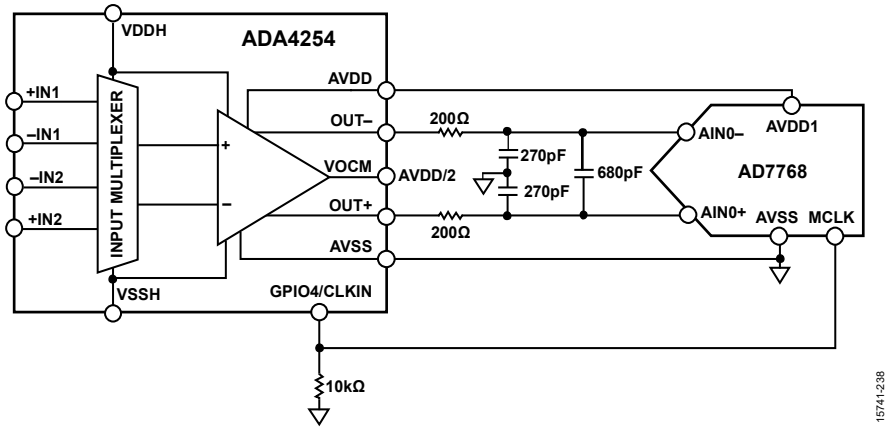


Figure 102. Clock Synchronization with the AD7768

PROGRAMMABLE LOGIC CONTROLLER (PLC) VOLTAGE/CURRENT INPUT

The circuit in Figure 103 shows the ADA4254 used to convert typical PLC input signal ranges (±10 V, ±5 V, or 20 mA) to an output voltage from 0 V to 5 V, compatible with high precision ADCs, such as the AD7768. To perform a voltage measurement, the ADA4254 input multiplexer is configured to Channel 1, +IN1 and –IN1, by writing 0x60 to the INPUT_MUX register. The MOSFET switch must be turned off by setting GPIO0 to logic level low. GPIO0 must be configured as an output by setting the corresponding bit field to 1 in the GPIO_DIR register. The state of GPIO0 is controlled by the corresponding bit field in the GPIO_DATA register. The ADA4254 gain can be configured through the GAIN_MUX register, depending on the input voltage level.

To perform a current measurement, the circuit shown in Figure 103 provides two different shunt resistors, 250 Ω and 100 Ω. To select a 250 Ω resistor, the MOSFET switch must be switched on by setting GPIO0 to logic level high using the GPIO_DATA register. The measurement is performed using Channel 1 of the ADA4254. To select 100 Ω, the MOSFET must be turned off by setting GPIO0 to logic level low. Channel 2 must be selected in this mode by writing 0x18 to the INPUT_MUX register.

The ADA4254 internal chopping circuitry can be synchronized to the companion ADC. This keeps the residual chopping noise at the correct frequency and prevents it from folding back to a frequency band of interest. To use the synchronization functionality, configure GPIO4 to be an input by setting the corresponding bit field in the GPIO_DIR register. Set the ADA4254 to accept an external clock by setting the EXT_CLK_IN bit field in the SF_CFG register. Adjust the clock divider such that the resulting clock is equal to 1 MHz. The divider can be adjusted in the SYNC_CFG register. The SYNC_CFG register also controls the synchronizing edge polarity. It is recommended that two reads from the M_CLK_CNT register are performed to ensure that the master clock counter is incrementing, indicating that the ADA4254 is receiving an external clock.

The ADA4254 on-chip diagnostics allow the user to check the circuit connections. In PLC applications, the circuit connections are verified using the wire break detection capabilities of the ADA4254. The WB_DETECT flag is set if one of the input connections is missing. Finally, the CRC check, SCLK counter, and SPI read/write check make the interface more robust as any read/write operations that is not valid is detected. The CRC check highlights if any bits are corrupted when being transmitted between the processor and the ADA4254.

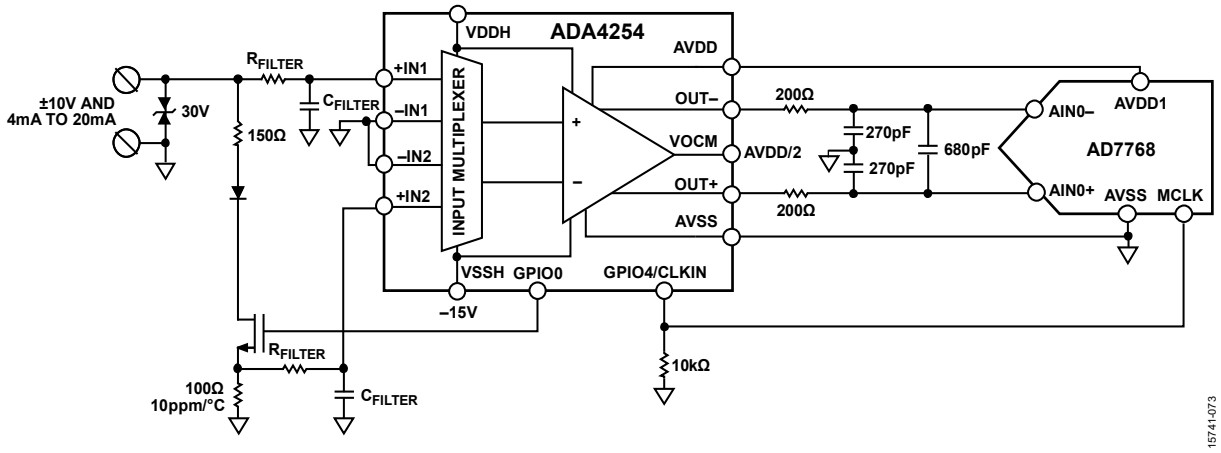


Figure 103. Voltage/Current Input Application

3-WIRE RTD WITH CURRENT EXCITATION

For a 3-wire RTD configuration, as shown in Figure 104, one current source is needed to perform the measurement. In this example circuit, IOUT_LV is used. The excitation current flows through RL1, RTD, and RL3 reference resistor (R_{REF}). Assuming that RL1, RL2, and RL3 are equal, the error voltages due to all the leads are equal. The voltage between +IN1 and –IN1 measures the voltage drop due to RL1 and the RTD. The voltage between +IN1 and –IN2 can be used to calculate the lead resistor. The second channel, +IN2 and –IN2, has a precision reference resistor used to measure the absolute value of the current flowing from IOUT_LV. A typical procedure for reading the RTD current is as follows:

1. Run a calibration to null any offset voltage error in the system by shorting the input of the instrumentational amplifier to ground.
2. Set the ADA4254 input multiplexer to Channel 1, +IN1 and –IN1, by writing 0x60 to the INPUT_MUX register.
3. Switch IOUT_LV on by writing 0x40 to the EX_CURRENT_CFG register. Also, set the current by writing to the EX_CURRENT[3:0] bits.
4. Set the gain of the ADA4254 to the appropriate gain via the GAIN_MUX register.
5. Take a reading on the ADC. This reading shows the voltage drop across RL1, the RTD element.
6. Switch the ADA4254 input mux to Channel 2, +IN2 and –IN2, by writing 0x18 to the INPUT_MUX register.
7. Take a reading on the ADC. This reading is the voltage drop across R_{REF}. IOUT_LV can be calculated from this reading.
8. Measure between –IN1 and +IN2. First the input multiplexer protection is disabled by setting the MUX_PROT_DIS bit to allow a –IN1 and +IN2 configuration.
9. Set the INPUT_MUX register to 0x30.
10. Repeat Step 4.
11. Take a reading on the ADC. This reading is the voltage drop across RL3 and R_{REF}.

Use the measurement from Step 11, the absolute value of IOUT_LV, and the R_{REF} value to calculate the lead resistance. The lead resistance is subtracted from the measurement in Step 5 to calculate the voltage drop across the RTD element. After the RTD voltage is calculated, the RTD resistance can be calculated.

The ADA4254 internal chopping circuitry can be synchronized to the companion ADC. This helps keep the residual chopping noise at its frequency and prevents it from folding back into a frequency band of interest. To use the sync functionality, configure GPIO4 to be an input by setting its corresponding bit field in the GPIO_DIR register. Set the ADA4254 to accept an external clock by setting the EXT_CLK_IN bit field in the SF_CFG register. Adjust the clock divider such that the resulting clock is equal to 1 MHz. The divider can be adjusted in SYNC_CFG register. The SYNC_CFG register also controls the syncing edge polarity. It is recommended that two reads from the M_CLK_CNT register are performed to ensure that the master clock counter is incrementing indicating that the ADA4254 is getting an external clock.

The ADA4254 on-chip diagnostics allow the user to check the circuit connections. In RTD applications, the circuit connections are verified using the wire break detection capabilities of the ADA4254. The WB_DETECT flag is set if one of the RTD wires is missing. Finally, the CRC check, SCLK counter, and SPI read/write check make the interface more robust because any read/write operations that are not valid are detected. The CRC check highlights if any bits are corrupted when being transmitted between the processor and the ADA4254.

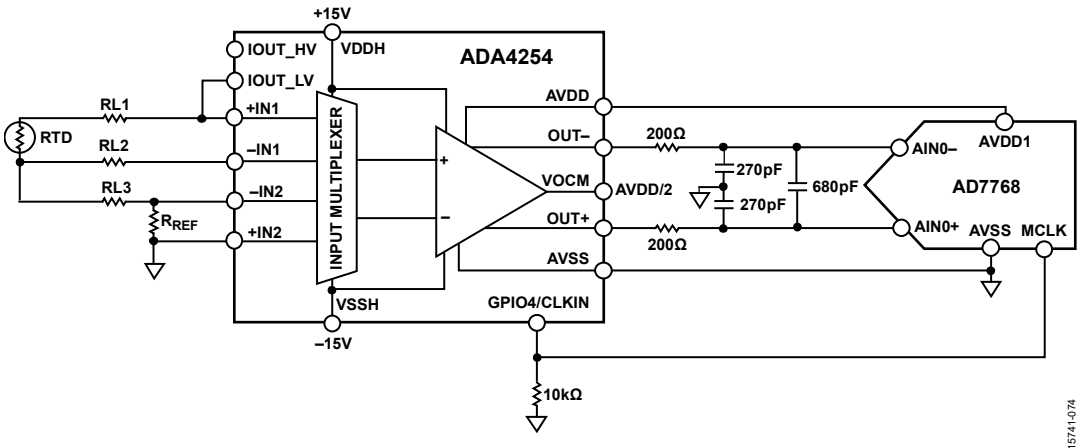


Figure 104. 3-Wire RTD Application

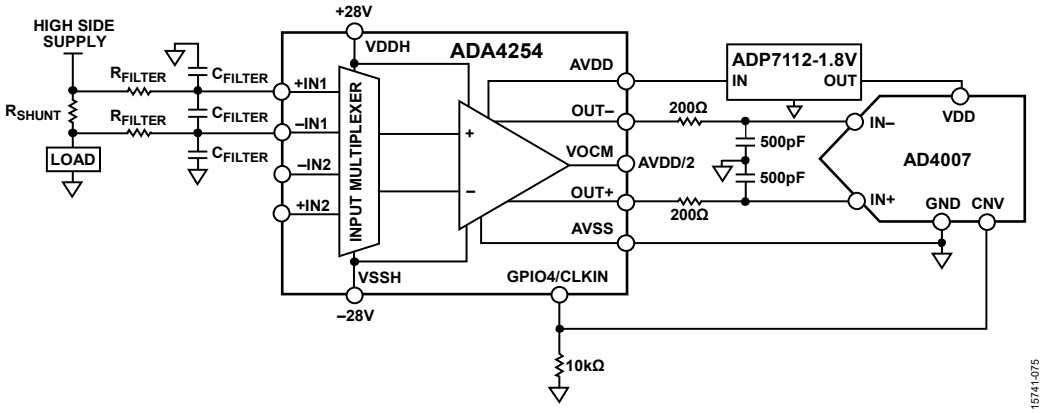


Figure 105. Current Sense Application

HIGH RAIL CURRENT SENSING

In high side configuration (current sensing configuration), the shunt resistor is referenced to the high supply side. High voltage is present at the inputs of the ADA4254. With the high common-mode voltage range, the ADA4254 multiplexer can withstand up to ±25 V on a ±28 V supply. The ADA4254 is ideal for measuring currents with a wide dynamic range because of the featured gain values, ranging from attenuation gains as low as 1/16 V/V to high gains up to 176 V/V with excellent gain linearity and low offset voltage over temperature.

A low-pass filter minimizes the noise coupling in the measurements. The ADA4254 has very low input bias current and input bias offset current, which minimizes the error introduced by the input bias current flowing through the resistor filter. The matching of the filter resistors is required to minimize the error contribution. The filter capacitors matching is also important. Any mismatch in the capacitor value results in a degradation in the CMMR of the ADA4254.

The ADA4254 internal chopping circuitry can be synchronized to the companion ADC. This keeps the residual chopping noise at the correct frequency and prevents it from folding back to a frequency band of interest. To use the synchronization functionality, configure GPIO4 to be an input by setting the corresponding bit field in the GPIO_DIR register. Set the ADA4254 to accept an external clock by setting the EXT_CLK_IN bit field in the SF_CFG register. Adjust the clock divider such that the resulting clock is equal to 1 MHz. The divider can be adjusted in SYNC_CFG register. The SYNC_CFG register also controls the syncing edge polarity. It is recommended that two reads from the M_CLK_CNT register are performed to ensure that the master clock counter is incrementing, indicating that the ADA4254 is receiving an external clock.

The ADA4254 on-chip diagnostics allow the user to check the circuit connections. In current sensing applications, the circuit connections are verified using the wire break detection capabilities of the ADA4254. The WB_DETECT flag is set if one of the connections to the shunt resistors is missing. Finally, the CRC check, SCLK counter, and SPI read/write check make the interface more robust because any read/write operations that are not valid are detected. The CRC check highlights if any bits are corrupted when being transmitted between the processor and the ADA4254.

REGISTER SUMMARY

Table 9. Register Summary

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	GAIN_MUX	G4	G[3:0]				Reserved	EXT_MUX[1:0]	
0x01	Reset	Reserved							RST
0x02	SYNC_CFG	Reserved	CLK_OUT_SEL	Reserved	SYNC_POL	Reserved	SYNC[2:0]		
0x03	DIGITAL_ERR	Reserved	CAL_BUSY	SPI_CRC_ERR	SPI_RW_ERR	SPI_SCLK_CNT_ERR	Reserved	MM_CRC_ERR	ROM_CRC_ERR
0x04	ANALOG_ERR	G_RST	POR_HV	Reserved	WB_ERR	FAULT_INT	OUTPUT_ERR	INPUT_ERR	MUX_OVER_VOLT_ERR
0x05	GPIO_DATA	Reserved	GPIO_DATA[6:0]						
0x06	INPUT_MUX	Reserved	SW_A1	SW_A2	SW_B1	SW_B2	SW_C1	SW_C2	SW_D12
0x07	WB_DETECT	WB_G_RST_DIS	Reserved			SW_F1	SW_F2	WB_CURRENT[1:0]	
0x08	GPIO_DIR	Reserved	GPIO_DIR[6:0]						
0x09	SCS	Reserved	SCS[6:0]						
0x0A	ANALOG_ERR_DIS	G_RST_DIS	POR_HV_DIS	Reserved	WB_ERR_DIS	MUX_PROT_DIS	OUTPUT_ERR_DIS	INPUT_ERR_DIS	MUX_OVER_VOLT_ERR_DIS
0x0B	DIGITAL_ERR_DIS	Reserved	CAL_BUSY_DIS	SPI_CRC_ERR_DIS	SPI_RW_ERR_DIS	SPI_SCLK_CNT_ERR_DIS	M_CLK_CNT_ERR_DIS	MM_CRC_ERR_DIS	ROM_CRC_ERR_DIS
0x0C	SF_CFG	Reserved		INT_CLK_OUT	EXT_CLK_IN	FAULT_INT_OUT	CAL_BUSY_OUT	EXT_MUX_EN[1:0]	
0x0D	ERR_CFG	ERR_LATCH_DIS	Reserved			ERR_DELAY[3:0]			
0x0E	TEST_MUX	G5	CAL_SEL	CAL_EN[1:0]		TEST_MUX[3:0]			
0x0F	EX_CURRENT_CFG	EX_CURRENT_SEL[1:0]		Reserved		EX_CURRENT[3:0]			
0x10	GAIN_CALx	Reserved				GAIN_CAL1[4:0]			
0x11		Reserved				GAIN_CAL2[4:0]			
0x12		Reserved				GAIN_CAL3[4:0]			
0x13		Reserved				GAIN_CAL4[4:0]			
0x14		Reserved				GAIN_CAL5[4:0]			
0x15		Reserved				GAIN_CAL6[4:0]			
0x16		Reserved				GAIN_CAL7[4:0]			
0x17		Reserved				GAIN_CAL8[4:0]			
0x18		Reserved				GAIN_CAL9[4:0]			
0x19		Reserved				GAIN_CAL10[4:0]			
0x1A		Reserved				GAIN_CAL11[4:0]			
0x1B		Reserved				GAIN_CAL12[4:0]			
0x1C		Reserved				GAIN_CAL13[4:0]			
0x1D		Reserved				GAIN_CAL14[4:0]			
0x1E		Reserved				GAIN_CAL15[4:0]			
0x1F		Reserved				GAIN_CAL16[4:0]			
0x20		Reserved				GAIN_CAL17[4:0]			
0x21		Reserved				GAIN_CAL18[4:0]			
0x22		Reserved				GAIN_CAL19[4:0]			
0x23		Reserved				GAIN_CAL20[4:0]			
0x24		Reserved				GAIN_CAL21[4:0]			
0x25		Reserved				GAIN_CAL22[4:0]			
0x26		Reserved				GAIN_CAL23[4:0]			
0x27		Reserved				GAIN_CAL24[4:0]			

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2A	TRIG_CAL	Reserved							TRIG_CAL
0x2E	M_CLK_CNT	M_CLK_CNT[7:0]							
0x2F	DIE_REV_ID	DIE_REV_ID[7:0]							
0x64	PART_ID	PART_ID[39:32]							
0x65		PART_ID[31:24]							
0x66		PART_ID[23:16]							
0x67		PART_ID[15:8]							
0x68		PART_ID[7:0]							

REGISTER DETAILS

GAIN_MUX REGISTER DETAILS

Table 10. GAIN_MUX Register Details (Register 0x00)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	G4	G[3:0]				Reserved	EXT_MUX[1:0]	
Access	RW	RW				Reserved	RW	
Reset	0	0	0	0	0	Reserved	0	0

Bit 7, G4—Output Amplifier Scaling Gain (1.375 V/V)

Setting the G4 bit to 1 configures the output amplifier in a scaling gain of 1.375 V/V. This configuration scales the input amplifier gain, G[3:0] (Bits[6:3]), by 1.375 V/V. The G4 bit takes precedence over the G5 bit, located in the TEST_MUX register. Setting the G4 bit to 0 configures the output amplifier in either a gain of 1 V/V or 1.25 V/V, depending on the value written to the G5 bit. These gain setting are summarized in Table 11.

Table 11. Output Amplifier Scaling Gain Settings

G5 Bit	G4 Bit	Output Amplifier Scaling Gain (V/V)
0	0	1
X	1	1.375
1	0	1.25

Bits[6:3], G[3:0]—Input Amplifier Gain Setting

The G[3:0] bits set the gain of the input amplifier, as shown in Table 12. The overall gain is scaled by the output amplifier scaling gain, which is configured using the G4 bit and the G5 bit. The default input amplifier gain is 1/16 V/V.

Table 12. Register Values for Input Amplifier Gains

	Bits in the G[3:0] Bit Field			
Input Amplifier Gain (V/V)	**G3**	**G2**	**G1**	**G0**
1/16	0	0	0	0
1/8	0	0	0	1
1/4	0	0	1	0
1/2	0	0	1	1
1	0	1	0	0
2	0	1	0	1
4	0	1	1	0
8	0	1	1	1
16	1	0	0	0
32	1	0	0	1
64	1	0	1	0
128	1	0	1	1
Reserved	1	1	0	0
Reserved	1	1	0	1
Reserved	1	1	1	0
Reserved	1	1	1	1

Bits[1:0], EXT_MUX[1:0]—External Multiplexer Control

When external multiplexer control is enabled using the EXT_MUX_EN bits in Register 0x0C, and GPIO1 and/or GPIO0 are configured as outputs using the GPIO_DIR bits in Register 0x08, EXT_MUX[1:0] sets the output of GPIO1 and/or GPIO0. This setup simplifies communication in externally multiplexed applications because both the gain and the external multiplexer can be configured with a single SPI write to the GAIN_MUX register. Multiplexers larger than 4-to-1 are supported by using additional GPIO pins and additional SPI writes.

SOFTWARE RESET REGISTER (RESET) DETAILS

Table 13. Reset Register Details (Register 0x01)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved							RST
Access	Reserved							W
Reset	Reserved							0

Bit 0, RST—Soft Reset

A soft reset can be initiated by setting the RST bit to 1. A soft reset clears all internal registers and sets them to their default values. The RST bit is self-clearing. This bit performs the same operation as a power-on reset and start-up calibration occurs.

CLOCK SYNCHRONIZATION CONFIGURATION REGISTER (SYNC_CFG) DETAILS

Table 14. SYNC_CFG Register Details (Register 0x02)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved	CLK_OUT_SEL	Reserved	SYNC_POL	Reserved	SYNC[2:0]		
Access	Reserved	RW	Reserved	RW	Reserved	RW		
Reset	Reserved	0	Reserved	0	Reserved	1	0	0

Bit 6, CLK_OUT_SEL—Clock Output Select

The ADA4254 1 MHz master clock is divided down to 125 kHz internally and is used by the zero drift amplifiers. When the INT_CLK_OUT bit in Register 0x0C is set to 1, setting CLK_OUT_SEL to 1 outputs the divided down 125 kHz clock on GPIO4. Clearing CLK_OUT_SEL to 0 outputs the 1 MHz master clock on GPIO4.

Bit 4, SYNC_POL—Clock Synchronization Polarity

When an external clock source is provided to the ADA4254, this bit is used to configure whether the rising or falling edge is used for synchronization. The synchronization edge is the edge at which the ADA4254 performs the chopping. Writing a 1 to this bit synchronizes the ADA4254 to the positive edge of the provided clock. Writing a 0 synchronizes the ADA4254 to the negative edge of the provided clock.

Bits[2:0], SYNC[2:0]—Internal Clock Divider Value

When an external clock is provided to the ADA4254, the SYNC[2:0] bits set the internal clock divider value. If an external clock is being supplied to the ADA4254, the clock value must be 1 MHz, or must be divided down by the ADA4254 to 1 MHz using the clock divider. Table 15 lists the available divider values.

Table 15. Clock Divider Values

	Bits in the SYNC[2:0] Bit Field		
Divider Value	**SYNC2**	**SYNC1**	**SYNC0**
÷1	0	0	0
÷2	0	0	1
÷4	0	1	0
÷8	0	1	1
÷16	1	0	0
÷32	1	0	1
Reserved	1	1	0
Reserved	1	1	1

DIGITAL ERROR REGISTER (DIGITAL_ERR) DETAILS

Table 16. DIGITAL_ERR Register Details (Register 0x03)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved	CAL_BUSY	SPI_CRC_ERR	SPI_RW_ERR	SPI_SCLK_CNT_ERR	Reserved	MM_CRC_ERR	ROM_CRC_ERR
Access	Reserved	R	RW	RW	RW	Reserved	RW	RW
Reset	Reserved	0	0	0	0	Reserved	0	0

Bit 6, CAL_BUSY—Calibration Busy (Read Only)

CAL_BUSY indicates that the PGIA is undergoing a calibration and self trim operation. Until this flag is clear, the ADA4254 output is not accurate. Writing a 1 or 0 to CAL_BUSY has no effect. CAL_BUSY can be output on GPIO2 when GPIO2 is configured as an output using the corresponding GPIO_DIR bit and when the CAL_BUSY_OUT bit is set to 1.

Bit 5, SPI_CRC_ERR—SPI CRC Error

The SPI_CRC_ERR error flag indicates that an error occurred during SPI communication with the ADA4254. This error occurs when the user provided CRC does not match the ADA4254 CRC calculation. Clear this error flag by writing a 1 to the SPI_CRC_ERR bit.

Bit 4, SPI_RW_ERR—SPI Read/Write Error

The SPI_RW_ERR error flag indicates that a SPI read/write operation is attempted on an invalid address. This error flag can be cleared by writing a 1 to this bit.

Bit 3, SPI_SCLK_CNT_ERR—SPI SCLK Count Error

The SPI_SCLK_CNT_ERR error flag indicates that, during SPI communication while $\overline{CS}$ is low, the number of SCLK edges is either insufficient or excessive. This error flag can be cleared by writing a 1 to this bit.

Bit 1, MM_CRC_ERR—Memory Map CRC Error

The MM_CRC_ERR error flag indicates that the current internal memory map does not match the result from the previous SPI write. If this error occurs, it is recommended to reprogram the ADA4254 registers. This error flag can be cleared by writing a 1 to this bit.

Bit 0, ROM_CRC_ERR—ROM CRC Error

The ROM_CRC_ERR error flag indicates that the internal ROM did not pass the CRC check. If this error occurs, it is strongly recommended to reset or power cycle the device. If the error does not reset with a power cycle or a soft reset, it is possible that the device is permanently damaged.

ANALOG ERROR REGISTER (ANALOG_ERR) DETAILS

Table 17. ANALOG_ERR Register Details (Register 0x04)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	G_RST	POR_HV	Reserved	WB_ERR	FAULT_INT	OUTPUT_ERR	INPUT_ERR	MUX_OVER_VOLT_ERR
Access	RW	RW	Reserved	RW	RW	RW	RW	RW
Reset	0	0	Reserved	0	0	0	0	0

Bit 7, G_RST—Gain Reset Flag

The G_RST flag indicates that the gain settings in the GAIN_MUX register have been reset to their defaults due to an overvoltage event in one or more of the input amplifiers that lasted more than 200 µs. Bit G5 in the TEST_MUX register is not reset by this event. This safety measure protects the input resistor network from overvoltage. This flag can be cleared by writing a 1 to this bit. Clearing this flag does not restore gain settings to the previous values.

Bit 6, POR_HV—Power-On Reset HV Supply

The POR_HV flag indicates that an event occurred on VDDH or VSSH, causing the power-on reset circuit to trip. When the supply voltage returns to a valid state, the ADA4254 runs a calibration. Clear this error flag by writing a 1 to this bit position.

Bit 4, WB_ERR—Wire Break Detect Error

When performing a wire break test using the WB_DETECT register, the WB_ERR flag indicates a fault on the inputs of the amplifier. Clear this error by writing a 1 to this bit position.

Bit 3, FAULT_INT—Fault Interrupt

An OR function is performed on all unmasked error flags in the ANALOG_ERR register and the DIGITAL_ERR register to generate the FAULT_INT fault interrupt. Configuring GPIO3 as an output using the corresponding GPIO_DIR bit and setting FAULT_INT_OUT to 1 outputs this signal to GPIO3. Clear this error by writing a 1 to this bit position. In this mode, GPIO3 is active low.

Bit 2, OUTPUT_ERR—Output Amplifier Error

The OUTPUT_ERR flag indicates that the output amplifier is overloaded. The cause of this overload condition is either the output voltage saturating or excessive current being conducted from the output of the amplifier. Clear this error by writing a 1 to this bit position.

Bit 1, INPUT_ERR—Input Amplifier Error

This flag indicates that one of the input amplifiers is overloaded. The cause of this overload condition is either saturation of one of the amplifier outputs, or a violation of the input voltage range. When this error flag is tripped for longer than 200 µs, gain settings in the GAIN_MUX register reset to the default values and the G_RST flag is set to 1. Bit G5 is not reset. Clear this error by writing a 1 to this bit position.

Bit 0, MUX_OVER_VOLT_ERR—Input Multiplexer Overvoltage Error

The MUX_OVER_VOLT_ERR flag indicates that excessive voltage is detected by the input multiplexer. The multiplexer turns all channels off to protect the input amplifier. Reads of the INPUT_MUX register during this time do not reflect this. The threshold for this detection is typically VSSH + 0.9 V and VDDH − 0.9 V. When the input voltage returns to the valid range after 20 µs, the multiplexer returns to the previous settings. If latched mode is in use, the error flag remains until reset. If nonlatched mode is used, the error flag clears when the multiplexer returns to the previous settings.

GPIO DATA REGISTER (GPIO_DATA) DETAILS

Table 18. GPIO_DATA Register Details (Register 0x05)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved	GPIO_DATA[6:0]						
Access	Reserved	RW						
Reset	Reserved	0	0	0	0	0	0	0

Bits[6:0], GPIO_DATA[6:0]—GPIO Data Values

When a GPIO pin is configured as an output, writing a 1 to the corresponding GPIO_DATA bit causes that GPIO pin to output a logic high. Conversely, writing a 0 to the corresponding GPIO_DATA bit causes that GPIO pin to output a logic low.

When a GPIO pin is configured as an input, each GPIO_DATA bit indicates whether the voltage on the corresponding GPIO pin is a logic high or logic low. Reading a 1 indicates a logic high. Reading a 0 indicates a logic low. Writing to the GPIO_DATA bits that are configured as inputs has no effect.

INTERNAL MUX CONTROL REGISTER (INPUT_MUX) DETAILS

Table 19. INPUT_MUX Register Details (Register 0x06)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved	SW_A1	SW_A2	SW_B1	SW_B2	SW_C1	SW_C2	SW_D12
Access	Reserved	RW	RW	RW	RW	RW	RW	RW
Reset	Reserved	1	1	0	0	0	0	0

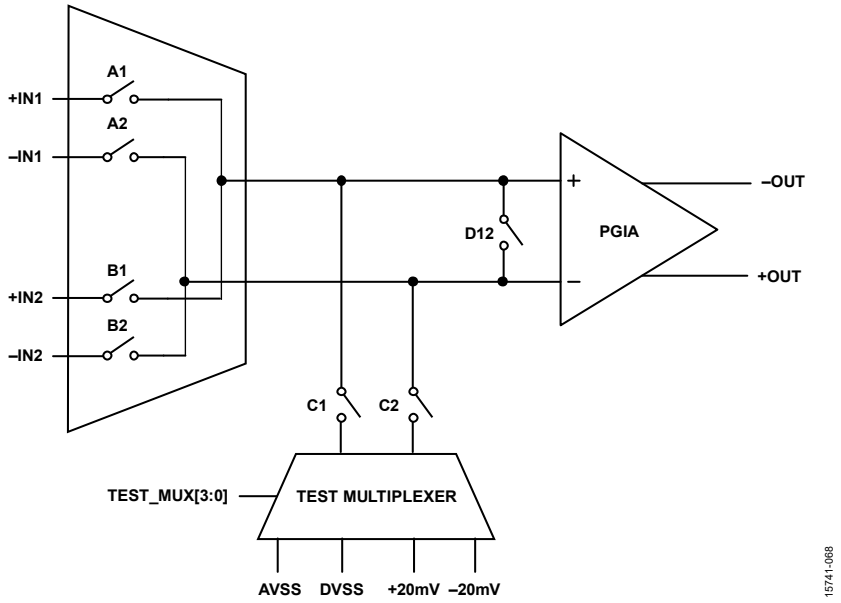


Figure 106. Input Mux Switch Configuration

Bit 6, SW_A1, and Bit 5, SW_A2—Channel 1 Input Switches

The SW_A1 bit and the SW_A2 bit control the Channel 1 input switches, A1 and A2, respectively (see Figure 106). Setting these bits to 1 closes the respective switch. SW_A1 and SW_A2 cannot be connected at the same time as SW_B1 and SW_B2, unless the MUX_PROT_DIS bit is set to 1.

Bit 4, SW_B1, and Bit 3, SW_B2—Channel 2 Input Switches

The SW_B1 bit and the SW_B2 bit control the Channel 2 input switches, B1 and B2, respectively (see Figure 106). Setting these bits to 1 closes the respective switch. SW_B1 and SW_B2 cannot be connected at the same time as SW_A1 and SW_A2, unless the MUX_PROT_DIS bit is set to 1.

Bit 2, SW_C1, and Bit 1, SW_C2—PGIA Input Test Multiplexer Switches

The SW_C1 bit and the SW_C2 bit can be set to 1 to connect either PGIA input to the output of the input test multiplexer (which is AVSS by default) via the C1 and C2 switches (see Figure 106).

Bit 0, SW_D12—PGIA Input Short Switch

The SW_D12 bit can be set to 1 to connect both PGIA inputs together via the D12 switch.

WIRE BREAK DETECT REGISTER (WB_DETECT) DETAILS

Table 20. WB_DETECT Register Details (Register 0x07)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	WB_G_RST_DIS	Reserved			SW_F1	SW_F2	WB_CURRENT[1:0]	
Access	RW	Reserved			RW	RW	RW	
Reset	0	Reserved			0	0	1	0

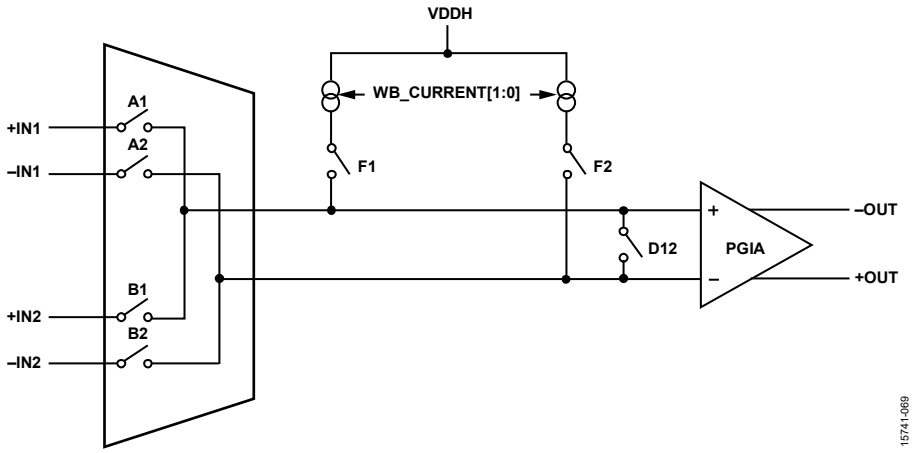


Figure 107. Wire Break Current Connectivity

Bit 7, WB_G_RST_DIS—Wire Break Gain Reset Disable

The WB_G_RST_DIS bit can be set to 1 to prevent the gain settings in the GAIN_MUX register from being overridden to 1/16 V/V when the SW_F1 bit or the SW_F2 bit are set to 1.

Bit 3, SW_F1, and Bit 2, SW_F2—Fault Switch Selection

The SW_F1 bit and the SW_F2 bit are used to connect the wire break current sources to the inputs, as shown in Figure 107. Setting SW_F1 or SW_F2 to 1 closes each corresponding switch. Both switches can be closed simultaneously. When SW_F1 or SW_F2 are set to 1 and WB_G_RST_DIS is cleared to 0, the gain settings in the GAIN_MUX register are temporarily overridden to the default values. Reading GAIN_MUX while SW_F1 or SW_F2 are set to 1 does not show this temporary override. When SW_F1 or SW_F2 are cleared to 0, the gain is also restored to the previous value.

Bits[1:0], WB_CURRENT—Detection Current Selection

Table 21 shows four different current values that can be used for wire break detection. Both current sources are set to the programmed value. The comparator used to detect a wire break event has a threshold at approximately 4 V from VDDH.

Table 21. Wire Break Detect Current Values

WB_CURRENT[1:0] Bits		Current Source Value	Threshold VDDH = 15 V
Bit 1	Bit 0		
0	0	250 nA	44 MΩ
0	1	2 µA	5.5 MΩ
1	0	4 µA (default)	2.75 MΩ
1	1	16 µA	688 kΩ

GPIO DIRECTION REGISTER (GPIO_DIR) DETAILS

Table 22. GPIO_DIR Register Details (Register 0x08)

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	GPIO_DIR[6:0]						
Access	Reserved	RW						
Reset	Reserved	0	0	0	0	0	0	0

Bits[6:0], GPIO_DIR—GPIO Direction Configuration

The GPIO_DIR bit field is used to configure each GPIO as either an input or an output. Setting a bit in this bit field to 1 configures the corresponding GPIO as an output. Clearing a bit in this bit field to 0 configures the corresponding GPIO as an input.

SEQUENTIAL CHIP SELECT REGISTER (SCS) DETAILS

Table 23. SCS Register Details (Register 0x09)

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Reserved	SCS[6:0]						
Access	Reserved	RW						
Reset	Reserved	0	0	0	0	0	0	0

Bits[6:0], SCS—Sequential Chip Select Configuration

Bits[6:0] configure the GPIO pins as sequential chip select (SCS) pins. Setting any bit in SCS[6:0] to 1 and configuring the respective GPIO as an output via the GPIO_DIR register makes that GPIO function as a chip select pin for a slave device. When SCS is used, the first $\overline{CS}$ pulse addresses the first GPIO configured for SCS. Subsequent $\overline{CS}$ pulses address the remainder of the GPIOs configured for SCS, and the last $\overline{CS}$ pulse addresses the ADA4254. This sequence repeats in a round robin format until the ADA4254 is configured otherwise. This process is shown in Figure 108.

Slave SCS lines may require pull-up resistors to avoid inadvertently communicating with slave devices during SCS configuration.

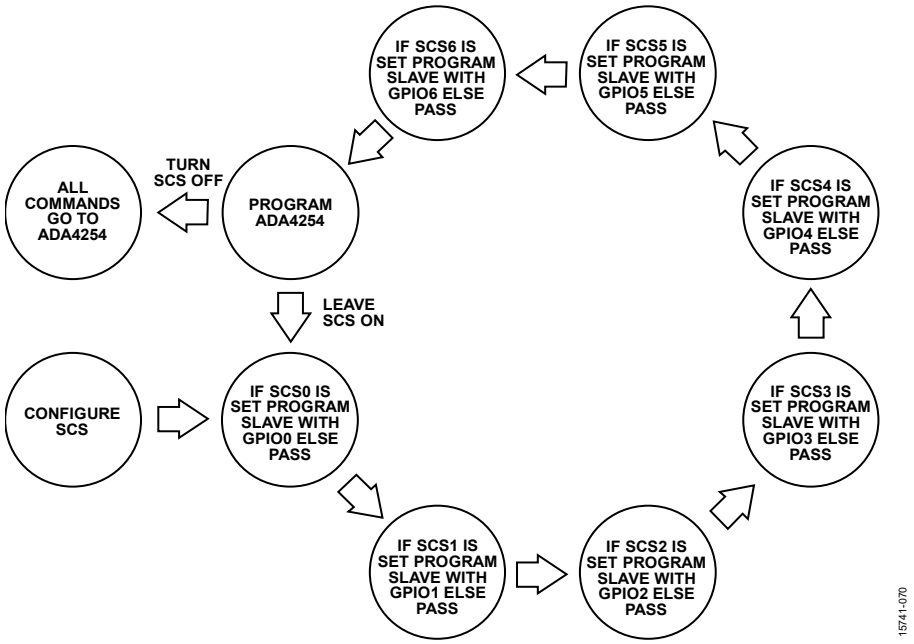


Figure 108. Sequential Chip Select Flowchart

ANALOG ERROR MASK REGISTER (ANALOG_ERR_DIS) DETAILS

The ANALOG_ERR_DIS register can be used to mask individual error flags in the ANALOG_ERR register. Setting bits in ANALOG_ERR_DIS to 1 disables the corresponding error flag.

Bit 7, G_RST_DIS—Disable Gain Reset Error Flag

This bit disables the G_RST error flag

Bit 6, POR_HV_DIS—Disable High Voltage Power Reset Flag

This bit disables the POR_HV error flag.

Bit 4, WB_ERR_DIS—Disable Wire-Break Detection Flag

This bit disables the WB_ERR error flag.

Bit 3, MUX_PROT_DIS—Disable Input Multiplexer Protection

By default, the input multiplexer does not allow both sets of inputs to be connected at the same time (this is a safety feature). This protection can be disabled by setting MUX_PROT_DIS to 1.

Bit 2, OUTPUT_ERR_DIS—Disable Output Amplifier Error Flag

This bit disables the OUTPUT_ERR error flag.

Bit 1, INPUT_ERR_DIS—Disable Input Amplifier Error Flag

This bit disables the INPUT_ERR error flag.

Bit 0, MUX_OVER_VOLT_ERR_DIS—Disable Multiplexer Overvoltage Flag.

This bit disables the MUX_OVER_VOLT error flag.

Table 24. ANALOG_ERR_DIS Register Details (Register 0x0A)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	G_RST_DIS	POR_HV_DIS	Reserved	WB_ERR_DIS	MUX_PROT_DIS	OUTPUT_ERR_DIS	INPUT_ERR_DIS	MUX_OVER_VOLT_ERR_DIS
Access	RW	RW	Reserved	RW	RW	RW	RW	RW
Reset	0	0	Reserved	0	0	0	0	0

DIGITAL ERROR MASK REGISTER (DIGITAL_ERR_DIS) DETAILS

The DIGITAL_ERR_DIS register can be used to mask individual error flags in the DIGITAL_ERR register. Setting bits in the DIGITAL_ERR_DIS register to 1 disables the error flag.

Table 25. DIGITAL_ERR_DIS Register Details (Register 0x0B)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved	CAL_ BUSY_DIS	SPI_CRC_ERR_DIS	SPI_RW_ ERR_DIS	SPI_SCLK_CNT_ ERR_DIS	M_CLK_CNT_ ERR_DIS	MM_CRC_ ERR_DIS	ROM_CRC_ ERR_DIS
Access	Reserved	RW	RW	RW	RW	RW	RW	RW
Reset	Reserved	0	1	0	0	0	0	0

Bit 6, CAL_BUSY_DIS—Disable Calibration Busy Error Flag

This bit disables the CAL_BUSY error flag.

Bit 5, SPI_CRC_ERR_DIS—Disable SPI CRC Error Flag

When SPI_CRC_ERR_DIS is cleared to 0, the ADA4254 expects an additional checksum byte with write commands and transmits an extra checksum byte with read commands. By default, SPI_ CRC_ERR_DIS is set to 1 and this functionality is disabled. After enabling CRC, a manual check can be performed to ensure that the CRC configuration command was properly communicated. If the CRC is used, it is recommended to configure the CRC before other registers so that all subsequent communication receives the CRC.

Bit 4, SPI_RW_ERR_DIS—Disable SPI Read/Write Error Flag

This bit disables the SPI_RW_ERR error flag.

Bit 3, SPI_SCLK_CNT_ERR_DIS—Disable SPI SCLK Count Error Flag

This bit disables the SPI_SCLK_CNT_ERR error flag.

Bit 2, M_CLK_CNT_ERR_DIS—Disable Master Clock Count Output

When this bit is set to 0, the master clock is updated in the M_CLK_CNT register. Setting this bit to 1 stops M_CLK_CNT from incrementing.

Bit 1, MM_CRC_ERR_DIS—Disable Memory Map CRC Error Flag

This bit disables the MEM_MAP_ERR error flag.

Bit 0, ROM_CRC_ERR_DIS—Disable ROM CRC Error Flag

This bit disables the ROM_CRC_ERR error flag.

SPECIAL FUNCTION CONFIGURATION REGISTER (SF_CFG) DETAILS

Table 26. SF_CFG Register Details (Register 0x0C)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved		INT_CLK_OUT	EXT_CLK_IN	FAULT_INT_OUT	CAL_BUSY_OUT	EXT_MUX[1:0]	
Access	Reserved		RW	RW	RW	RW	RW	
Reset	Reserved		0	0	0	0	0	0

Bit 5, INT_CLK_OUT—Internal Oscillator Output

When GPIO4 is configured as an output via GPIO_DIR and INT_CLK_OUT is set to 1, one of the internal clocks is output to GPIO4. CLK_OUT_SEL in the SYNC_CFG register determines which internal clock is on GPIO4.

Bit 4, EXT_CLK_IN—External Oscillator Input

When GPIO4 is configured as an input via GPIO_DIR and EXT_CLK_IN is set to 1, an external clock can be provided via GPIO4. If this clock frequency is not 1 MHz, the on-chip clock divider must be used to divide the clock via the SYNC[2:0] bits. The default setting for the internal clock divider is 16.

Bit 3, FAULT_INT_OUT—Fault Interrupt Output

When GPIO3 is configured as an output via GPIO_DIR and FAULT_INT_OUT is set to 1, the value in FAULT_INT appears on GPIO3.

Bit 2, CAL_BUSY_OUT—Calibration Busy Output

When GPIO2 is configured as an output via GPIO_DIR and CAL_BUSY_OUT is set to 1, the value in CAL_BUSY appears on GPIO2.

Bits[1:0], EXT_MUX_EN[1:0]—Enable External Multiplexer Control

Each bit in the EXT_MUX_EN[1:0] bit range enables GPIO1 and/or GPIO0 to be controlled via EXT_MUX in the GAIN_MUX register.

ERROR CONFIGURATION REGISTER

Table 27. CFG_C Register Details (Register 0x0D)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	ERR_LATCH_DIS	Reserved			ERR_DELAY[3:0]			
Access	RW	Reserved			RW	RW	RW	RW
Reset	0	Reserved			0	1	0	0

Bit 7, ERR_LATCH_DIS—Disable Error Latching

By default, ERR_LATCH_DIS is cleared to 0 and error flags are latched and require resetting. Setting ERR_LATCH_DIS to 1 makes the errors appear transparently (nonlatching) on the respective outputs. When ERR_LATCH_DIS is set to 1, errors can be suppressed for the time interval configured by ERR_DELAY.

Bits[3:0], ERR_DELAY[3:0] —Error Suppression Time

When ERR_LATCH_DIS is set to 1, ERR_DELAY determines the number of clock cycles an error must remain present before the error flag is tripped, which eliminates false trips due to noise and transients.

Table 28. Error Flag Suppression Time

ERR_DELAY[3:0]	Clock Cycles (µS)
0x0	0
0x1	1
0x2	2
0x3	3
0x4	4
0x5	5
0x6	6
0x7	7
0x8	8
0x9	12
0xA	16
0xB	24
0xC	32
0xD	48
0xE	64
0xF	127

TEST MULTIPLEXER REGISTER (TEST_MUX) DETAILS

Table 29. TEST_MUX Register Details (Register 0x0E)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	G5	CAL_SEL	CAL_EN[1:0]		TEST_MUX[3:0]			
Access	RW	RW	RW		RW			
Reset	0	0	0	0	0	0	0	0

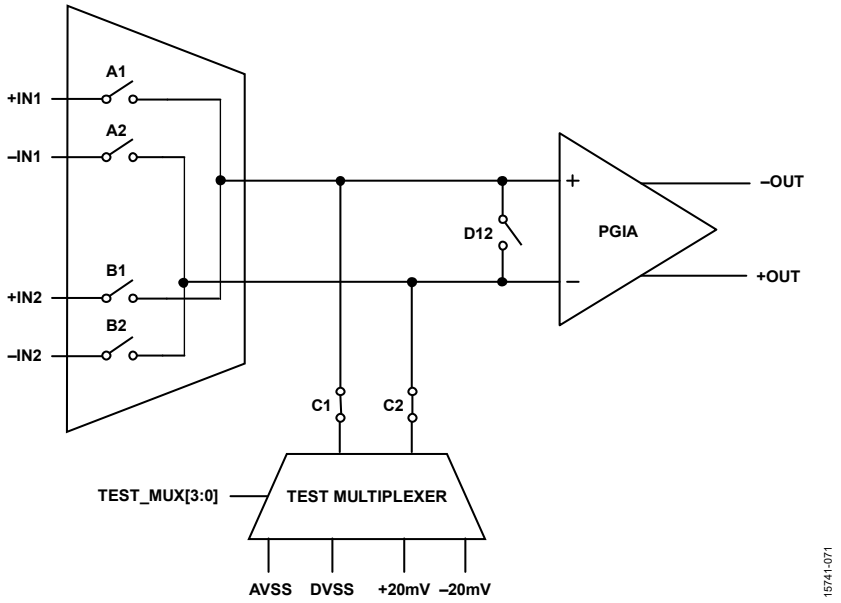


Figure 109. Test Multiplexer Connectivity

Bit 7, G5—Output Amplifier Scaling Gain = 1.25 V/V

Clearing Bit G4 to 0 and setting Bit G5 to 1 configures the output amplifier to a scaling gain value of 1.25 V/V. This setting scales the input amplifier gain configured in the GAIN_MUX register by 1.25 V/V.

Table 30. Output Amplifier Scaling Gain Settings

G5	G4	Output Amplifier Scaling Gain (V/V)
0	0	1
X	1	1.375
1	0	1.25

Bit 6, CAL_SEL—Calibration Type Configuration

Clearing the CAL_SEL bit to 0 configures the ADA4254 to perform quick calibrations. Setting CAL_SEL to 1 configures the ADA4254 to perform full calibrations.

Bits[5:4], CAL_EN[1:0]—Scheduled Calibration Enable and Interval

CAL_EN enables scheduled calibrations and configures the interval on which these calibrations execute. While calibrations are executing, the inputs of the PGIA are not connected to the input pins. The CAL_BUSY signal indicates when a calibration is executing. CAL_BUSY can be output to GPIO2 by configuring GPIO2 as an output via GPIO_DIR and setting CAL_BUSY_OUT to 1. Minimize and avoid noise and input transients during calibrations.

Table 31. Scheduled Calibration Configurations

CAL_EN, Bit 1	CAL_EN, Bit 0	Scheduled Calibration Configuration
0	0	Disabled
0	1	Enabled, 33 sec interval
1	0	Enabled, 132 sec interval
1	1	Enabled, 495 sec interval

Bits[3:0], TEST_MUX[3:0]—Input Test Multiplexer Configuration

The TEST_MUX[3:0] bits are used to configure the input test multiplexers, which can switch four different signals to either of the inputs for diagnostic and calibration purposes. These potentials are AVSS, DVSS, +20 mV, and −20 mV. SW_C1 and SW_C2 must also be set to 1 for the outputs of these multiplexers to be connected to the amplifier inputs.

Table 32. Test Multiplexer Configurations

TEST_MUX[3:0]	Noninverting Input	Inverting Input
0000	AVSS	AVSS
0001	DVSS	AVSS
0100	AVSS	DVSS
0101	DVSS	DVSS
1010	+20 mV	
1111	−20 mV	

EXCITATION CURRENT CONFIGURATION REGISTER (EX_CURRENT_CFG) DETAILS

Table 33. EX_CURRENT_CFG Register Details (Register 0x0F)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	EX_CURRENT_SEL[1:0]		Reserved		EX_CURRENT[3:0]			
Access	RW		Reserved		RW			
Reset	0	0	Reserved		0	0	0	0

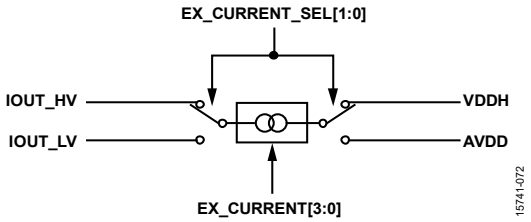


Figure 110. Excitation Current Connectivity

Bits[7:6], EX_CURRENT_SEL[1:0]—Excitation Current Connection Configuration

EX_CURRENT_SEL[1:0] configures an internal current source to either IOUT_LV or IOUT_HV. Table 34 shows all available configurations. When IOUT_LV is used, the source of this current is AVDD. When IOUT_HV is used, the source of this current is VDDH.

Table 34. Excitation Current Source Connections

EX_CURRENT_SEL[1:0]	Current Source
0b00	None
0b01	IOUT_LV
0b10	IOUT_HV
0b11	IOUT_LV

Bits[3:0], EX_CURRENT[3:0]—Excitation Current Value

The EX_CURRENT[3:0] bits configure the current source value connected via EX_CURRENT_SEL. Table 35 shows all the possible current values.

Table 35. Excitation Current Values

EX_CURRENT[3:0]	Excitation Current Value
0x0	0 µA
0x1	100 µA
0x2	200 µA
0x3	300 µA
0x4	400 µA
0x5	500 µA
0x6	600 µA
0x7	700 µA
0x8	800 µA
0x9	900 µA
0xA	1 mA
0xB	1.1 mA
0xC	1.2 mA
0xD	1.3 mA
0xE	1.4 mA
0xF	1.5 mA

GAIN CALIBRATION REGISTERS (GAIN_CALx) DETAILS

The gain calibration registers contain the measured gain error of each individual ADA4254. Refer to the Gain Error Calibration section for details on how to use these values. GAIN_CAL1 through GAIN_CAL12 store gain error results for each input gain setting with a scaling gain of 1 V/V. When a scaling gain of 1 V/V is used, these gain error values are used directly. GAIN_CAL13 through GAIN_CAL24 store any additional gain error incurred when 1.375 V/V or 1.25 V/V scaling gains are used. When scaling gains other than 1 V/V are used, the gain error read from the appropriate GAIN_CAL1 through GAIN_CAL12 register must be summed with the corresponding additional gain error read from the appropriate GAIN_CAL13 through GAIN_CAL24. For example, if the input gain is 2 V/V and the 1.25 V/V scalar is used, the total gain error is GAIN_CAL6 + GAIN_CAL21.

Table 36. GAIN_CAL Registers Details (Register 0x10 to Register 0x27)

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10	GAIN_CALx	Reserved			GAIN_CAL1[4:0]				
0x11		Reserved			GAIN_CAL2[4:0]				
0x12		Reserved			GAIN_CAL3[4:0]				
0x13		Reserved			GAIN_CAL4[4:0]				
0x14		Reserved			GAIN_CAL5[4:0]				
0x15		Reserved			GAIN_CAL6[4:0]				
0x16		Reserved			GAIN_CAL7[4:0]				
0x17		Reserved			GAIN_CAL8[4:0]				
0x18		Reserved			GAIN_CAL9[4:0]				
0x19		Reserved			GAIN_CAL10[4:0]				
0x1A		Reserved			GAIN_CAL11[4:0]				
0x1B		Reserved			GAIN_CAL12[4:0]				
0x1C		Reserved			GAIN_CAL13[4:0]				
0x1D		Reserved			GAIN_CAL14[4:0]				
0x1E		Reserved			GAIN_CAL15[4:0]				
0x1F		Reserved			GAIN_CAL16[4:0]				
0x20		Reserved			GAIN_CAL17[4:0]				
0x21		Reserved			GAIN_CAL18[4:0]				
0x22		Reserved			GAIN_CAL19[4:0]				
0x23		Reserved			GAIN_CAL20[4:0]				
0x24		Reserved			GAIN_CAL21[4:0]				
0x25		Reserved			GAIN_CAL22[4:0]				
0x26		Reserved			GAIN_CAL23[4:0]				
0x27		Reserved			GAIN_CAL24[4:0]				
Access		Reserved			R				

TRIGGER CALIBRATION REGISTER (TRIG_CAL) DETAILS

Table 37. TRIG_CAL Registers Details (Register 0x2A)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	Reserved							TRIG_CAL
Access	Reserved							W
Reset	Reserved							0

Bit 0, TRIG_CAL—Trigger Calibration Input

Setting TRIG_CAL to 1 initiates a calibration sequence when scheduled calibrations are disabled via CAL_EN. The type of calibration that is triggered can be configured via CAL_SEL. The TRIG_CAL bit is self clearing.

MASTER CLOCK COUNT REGISTER (M_CLK_CNT) DETAILS

Table 38. M_CLK_CNT Registers Details (Register 0x2E)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	M_CLK_CNT[7:0]							
Access	R							

Bits[7:0], M_CLK_CNT[7:0]—Master Clock Count

M_CLK_CNT contains a master clock counter that increments when M_CLK_CNT_ERR is cleared to 0. The counter is updated every 512 µs. Setting M_CLK_CNT_ERR to 1 stops this register from updating.

DIE REVISION IDENTIFICATION REGISTER (DIE_REV_ID) DETAILS

Table 39. DIE_REV_ID Registers Details (Register 0x2F)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	DIE_REV_ID[7:0]							
Access	R							
Reset	0	0	1	1	0	0	0	0

Bits[7:0], DIE_REV_ID[7:0]—Die Revision Identification Number

DIE_REV_ID contains a fixed value of 0x30 that can be used to verify the SPI communication with the ADA4254.

DEVICE IDENTIFICATION REGISTERS (PART_ID) DETAILS

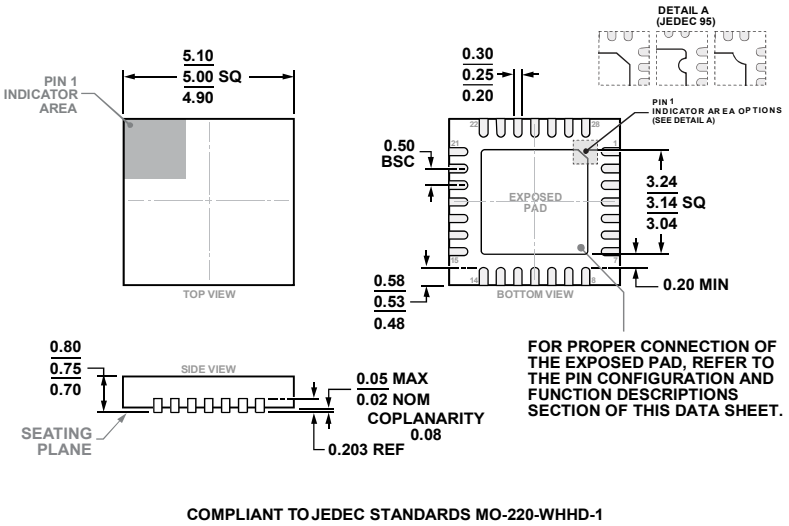
Table 40. PART_ID Registers Details (Register 0x2A)[1]

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x64	PART_ID[39:32]							
0x65	PART_ID[31:24]							
0x66	PART_ID[23:16]							
0x67	PART_ID[15:8]							
0x68	PART_ID[7:0]							
Access	R							

PART_ID[39:0]—Part ID Number

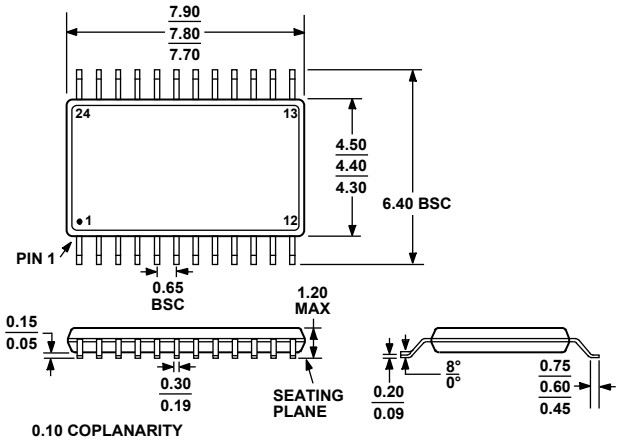
The PART_ID register contains a unique device identification number that is programmed at the factory.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-1

Figure 111. 28-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-28-10)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AD

Figure 112. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADA4254ACPZ	−40°C to +105°C	28-Lead Lead Frame Chip Scale Package [LFCSP]	CP-28-10
ADA4254ACPZ-R7	−40°C to +105°C	28-Lead Lead Frame Chip Scale Package [LFCSP]	CP-28-10
ADA4254ACPZ-RL	−40°C to +105°C	28-Lead Lead Frame Chip Scale Package [LFCSP]	CP-28-10
ADA4254ARUZ	−40°C to +105°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADA4254ARUZ-R7	−40°C to +105°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADA4254ARUZ-RL	−40°C to +105°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADA4254RU-EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.