

March 1997

Features

- Industry Standard Pinout
- Very Low Operating Current 8mA at $V_{DD} = 5V$ and Cycle Time = 1 μ s
- Two Chip Select Inputs Simple Memory Expansion
- Memory Retention for Standby 2V (Min) Battery Voltage
- Output Disable for Common I/O Systems
- Three-State Data Output for Bus Oriented Systems
- Separate Data Inputs and Outputs
- TTL Compatible (MWS5101A)

Description

The MWS5101 and MWS5101A are 256 word by 4-bit static random access memories designed for use in memory systems where high speed, very low operating current, and simplicity in use are desirable. They have separate data inputs and outputs and utilize a single power supply of 4V to 6.5V. The MWS5101 and MWS5101A differ in input voltage characteristics (MWS5101A is TTL compatible).

Two Chip Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems by forcing the output into a high impedance state during a write operation independent of the Chip Select input condition. The output assumes a high impedance state when the Output Disable is at high level or when the chip is deselected by $\overline{CS1}$ and/or $CS2$.

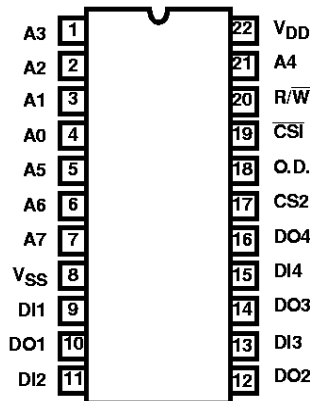
The high noise immunity of the CMOS technology is preserved in this design. For TTL interfacing at 5V operation, excellent system noise margin is preserved by using an external pull-up resistor at each input.

For applications requiring wider temperature and operating voltage ranges, the mechanically and functionally equivalent static RAM, CDP1822 may be used.

The MWS5101 and MWS5101A types are supplied in 22 lead hermetic dual-in-line, sidebraced ceramic packages (D suffix), in 22 lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Pinout

MWS5101, MWS5101A
(PDIP, SBDIP)
TOP VIEW



Ordering Information

PACKAGE	TEMP. RANGE	MWS5101		MWS5101A		PKG. NO.
		250ns	350ns	250ns	350ns	
PDIP Burn-In	0°C to +70°C	MWS5101EL2	MWS5101ELS	MWS5101AEL2	MWS5101AEL3	E22.4
					MWS5101AEL3X	E22.4
SBDIP Burn-In	0°C to +70°C	-	MWS5101DL3X	-	MWS5101ADL3	D22.4A
						D22.4A

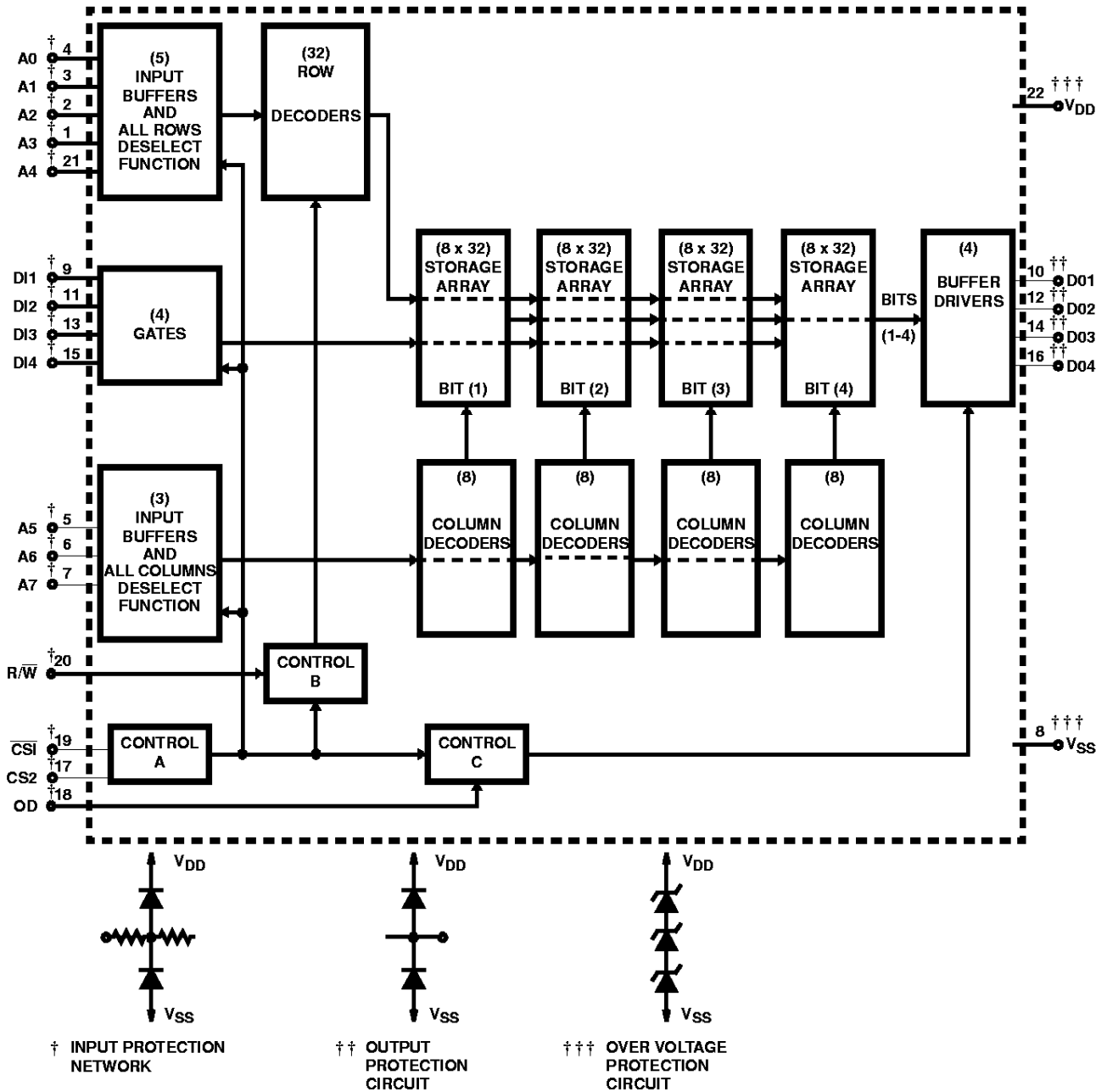
MWS5101, MWS5101A

OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	CHIP SELECT 1 (CS ₁)	CHIP SELECT 2 (CS ₂)	OUTPUT DISABLE (OD)	READ/WRITE (R/W)	
Read	0	1	0	1	Read
Write	0	1	0	0	Data In
Write	0	1	1	0	High Impedance
Standby	1	X	X	X	High Impedance
Standby	X	0	X	X	High Impedance
Output Disable	X	X	1	X	High Impedance

NOTE: Logic 1 = High, Logic 0 = Low, X = Don't Care.

Functional Block Diagram



MWS5101, MWS5101A

Dynamic Electrical Specifications at $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = 5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS (NOTE 1)						UNITS
		L2 TYPES			L3 TYPES			
		(NOTE 2) MIN	(NOTE 3) TYP	MAX	(NOTE 2) MIN	(NOTE 3) TYP	MAX	
READ CYCLE TIMES (FIGURE 1)								
Read Cycle	t_{RC}	250	-	-	350	-	-	ns
Access from Address	t_{AA}	-	150	250	-	200	350	ns
Output Valid from $\overline{\text{Chip Select 1}}$	t_{DOA1}	-	150	250	-	200	350	ns
Output Valid from Chip Select 2	t_{DOA2}	-	150	250	-	200	350	ns
Output Valid from Output Disable	t_{DOA3}	-	-	110	-	-	150	ns
Output Hold from $\overline{\text{Chip Select 1}}$	t_{DOH1}	20	-	-	20	-	-	ns
Output Hold from Chip Select 2	t_{DOH2}	20	-	-	20	-	-	ns
Output Hold from Output Disable	t_{DOH3}	20	-	-	20	-	-	ns
WRITE CYCLE TIMES (FIGURE 2)								
Write Cycle	t_{WC}	300	-	-	400	-	-	ns
Address Setup	t_{AS}	110	-	-	150	-	-	ns
Write Recovery	t_{WR}	40	-	-	50	-	-	ns
Write Width	t_{WRW}	150	-	-	200	-	-	ns
Input Data Setup Time	t_{DS}	150	-	-	200	-	-	ns
Data in Hold	t_{DH}	40	-	-	50	-	-	ns
$\overline{\text{Chip Select 1}}$ Setup	t_{CS1S}	110	-	-	150	-	-	ns
Chip Select 2 Setup	t_{CS2S}	110	-	-	150	-	-	ns
$\overline{\text{Chip Select 1}}$ Hold	t_{CS1H}	0	-	-	0	-	-	ns
Chip Select 2 Hold	t_{CS2H}	0	-	-	0	-	-	ns
Output Disable Setup	t_{ODS}	110	-	-	150	-	-	ns

NOTES:

1. MWS5101: $t_R, t_F = 20\text{ns}$, $V_{IH} = 0.7V_{DD}$, $V_{IL} = 0.3V_{DD}$; $C_L = 100\text{pF}$ and MWS5101A: $t_R, t_F = 20\text{ns}$, $V_{IH} = 2.2\text{V}$, $V_{IL} = 0.65\text{V}$; $C_L = 50\text{pF}$ and 1 TTL Load.
2. Time required by a limit device to allow for the indicated function.
3. Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

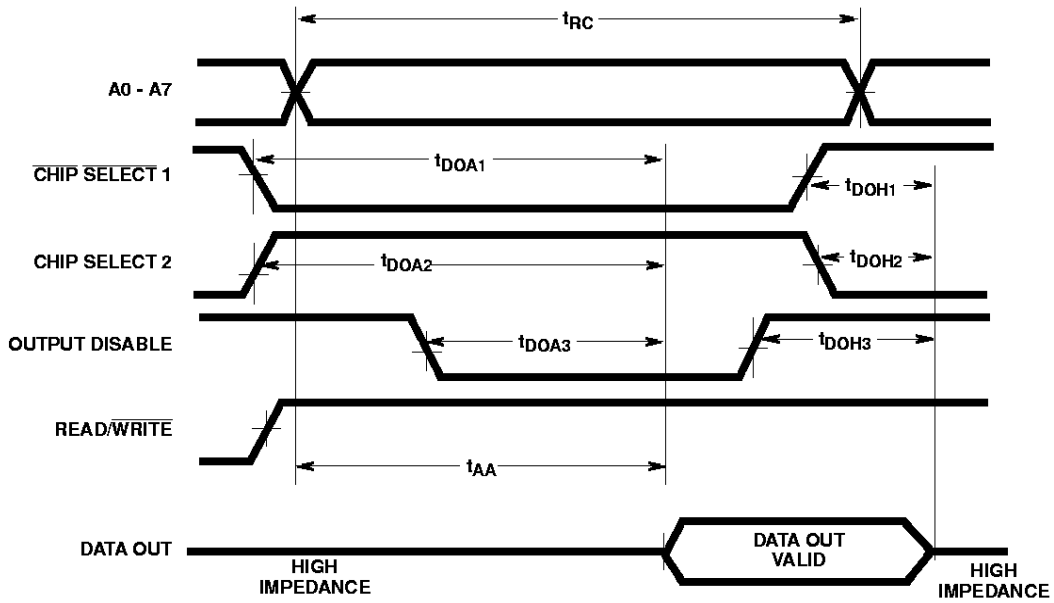
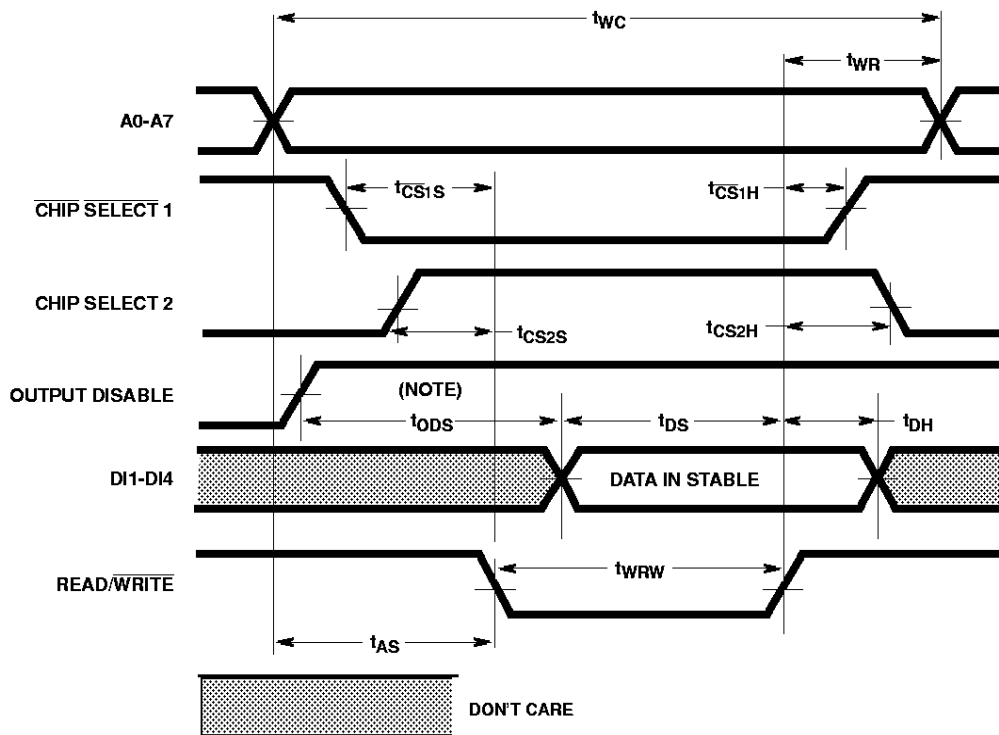


FIGURE 1. READ CYCLE TIMING WAVEFORMS



NOTE: t_{ODS} is required for common I/O operation only; for separate I/O operations, output disable is "don't care".

FIGURE 2. WRITE CYCLE TIME WAVEFORMS

MWS5101, MWS5101A

Data Retention Specifications at $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; See Figure 3

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS			UNITS	
		V_{DR} (V)	V_{DD} (V)	ALL TYPES				
				MIN	(NOTE 1) TYP	MAX		
Minimum Data Retention Voltage	V_{DR}	-	-	-	1.5	2	V	
Data Retention Quiescent Current	L2 Types	I_{DD}	2	-	-	2	10	μA
	L3 Types							
Chip Deselect to Data Retention Time	t_{CDR}	-	5	600	-	-	ns	
Recovery to Normal Operation Time	t_{RC}	-	5	600	-	-	ns	
V_{DD} to V_{DR} Rise and Fall Time	t_R, t_F	2	5	1	-	-	μs	

NOTE:

1. Typical Values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

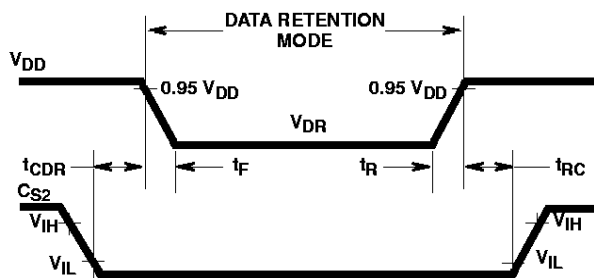


FIGURE 3. LOW V_{DD} DATA RETENTION TIMING WAVEFORMS

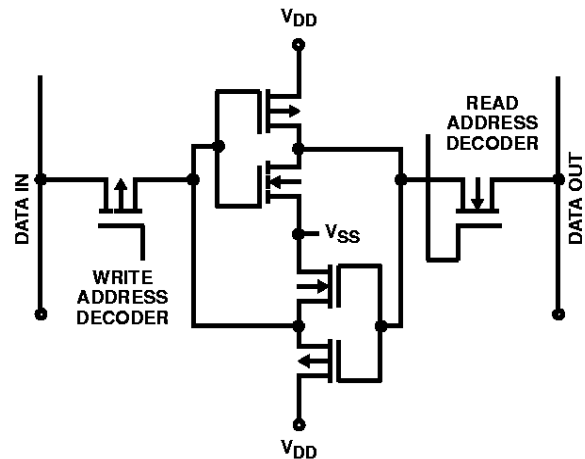


FIGURE 4. MEMORY CELL CONFIGURATION

MWS5101, MWS5101A

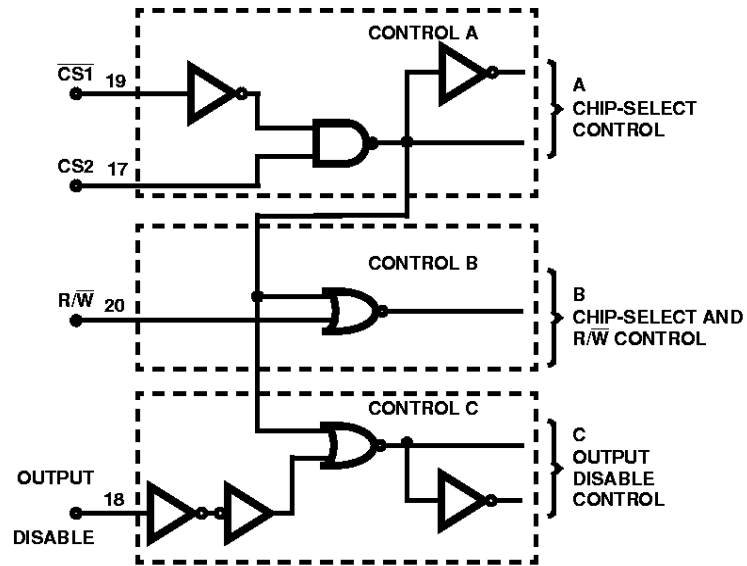


FIGURE 5. LOGIC DIAGRAM OF CONTROLS FOR MWS5101, MWS5101A