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Bipolar Power Transistors

40 V, 3.0 A, Low $V_{CE(sat)}$

PNP Transistor

NSS40300CT

ON Semiconductor's e²PowerEdge family of low $V_{CE(sat)}$ transistors are surface mount devices featuring ultra-low saturation voltage, $V_{CE(sat)}$, and high current gain capability. These are designed for use in lower voltage, high speed switching applications where affordable efficient energy control is important.

Housed in an ultra slim LFAK4 5x6 package, typical applications are DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, digital cameras and MP3 players where PCB space is at a premium. The LFAK4 5x6 package also contains wettable flanks which are a requirement for the automotive industry's optical inspection methods that are implemented in end applications such as air bag deployment, powertrain control units, and instrument clusters.

Features

- Complement to NSS40301CT
- Ultra-slim LFAK4 Package (5 x 6 mm) with Wettable Flanks
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	6.0	Vdc
Base Current - Continuous	I_B	1.0	Adc
Collector Current - Continuous	I_C	3.0	Adc
Collector Current - Peak	I_{CM}	5.0	Adc
Total Power Dissipation Total P_D @ $T_A = 25^\circ\text{C}$ (Note 1) Total P_D @ $T_A = 25^\circ\text{C}$ (Note 2)	P_D	2.0 0.80	W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

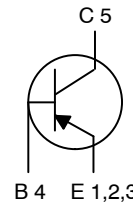
1. Mounted on 1" sq. (645 sq. mm) Collector pad on FR-4 bd material.
2. Mounted on 0.012" sq. (7.6 sq. mm) Collector pad on FR-4 bd material.



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PNP TRANSISTOR
3.0 AMPERES
40 VOLTS

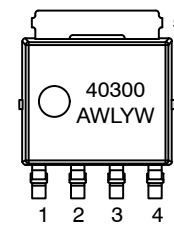


Schematic



LFAK4 5x6
CASE 760AB

MARKING DIAGRAM



(Top View)

40300 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NSS40300CT

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case			°C/W
Junction-to-Ambient on 1" sq. (645 sq. mm) Collector pad on FR-4 bd material	$R_{\theta JA}$	58	
Junction-to-Ambient on 0.012" sq. (7.6 sq. mm) Collector pad on FR-4 bd material	$R_{\theta JA}$	149	

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ($I_C = 10\text{ mAdc}$, $I_B = 0\text{ Adc}$)	$V_{CEO(sus)}$	40	-	-	Vdc
Emitter-Base Voltage ($I_E = 50\ \mu\text{Adc}$, $I_C = 0\text{ Adc}$)	V_{EBO}	6.0	-	-	Vdc
Collector Cutoff Current ($V_{CB} = 40\text{ Vdc}$)	I_{CBO}	-	-	100	nAdc
Emitter Cutoff Current ($V_{BE} = 6.0\text{ Vdc}$)	I_{EBO}	-	-	100	nAdc

ON CHARACTERISTICS (Note 3)

Collector-Emitter Saturation Voltage ($I_C = 0.5\text{ Adc}$, $I_B = 50\text{ mAdc}$) ($I_C = 1.0\text{ Adc}$, $I_B = 20\text{ mAdc}$) ($I_C = 3.0\text{ Adc}$, $I_B = 0.3\text{ Adc}$)	$V_{CE(sat)}$	-	-	0.070 0.150 0.400	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}$, $I_B = 0.1\text{ Adc}$)	$V_{BE(sat)}$	-	-	1.0	Vdc
Base-Emitter On Voltage ($I_C = 1.0\text{ Adc}$, $V_{CE} = 2.0\text{ Vdc}$)	$V_{BE(on)}$	-	-	0.9	Vdc
DC Current Gain ($I_C = 0.5\text{ Adc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 1.0\text{ Adc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 3.0\text{ Adc}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}	200 175 100	- - -	- 600 -	-

DYNAMIC CHARACTERISTICS

Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $f = 1.0\text{ MHz}$)	C_{ob}	-	40	-	pF
Input Capacitance ($V_{EB} = 5.0\text{ Vdc}$, $f = 1.0\text{ MHz}$)	C_{ib}	-	130	-	pF
Current-Gain - Bandwidth Product (Note 4) ($I_C = 500\text{ mA}$, $V_{CE} = 10\text{ V}$, $F_{test} = 1.0\text{ MHz}$)	f_T	-	160	-	MHz

3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

4. $f_T = |h_{FE}| \cdot f_{test}$

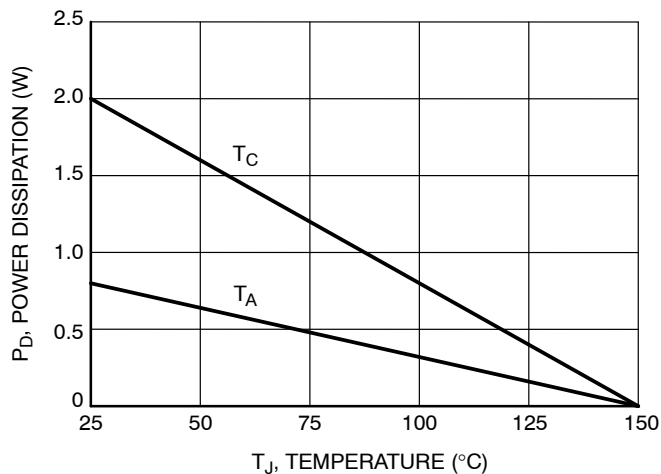


Figure 1. Power Derating

TYPICAL CHARACTERISTICS

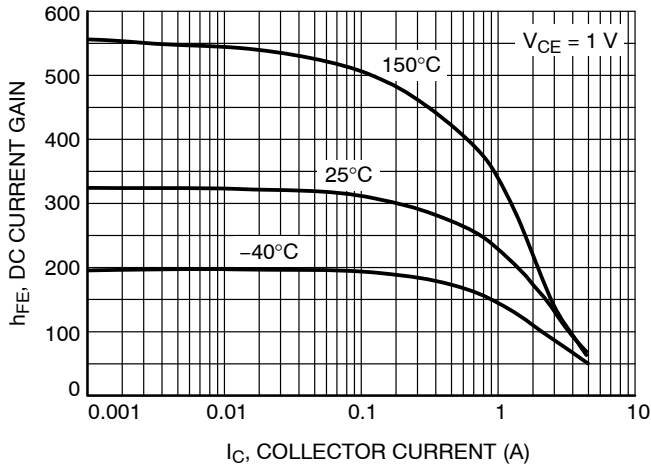


Figure 2. DC Current Gain

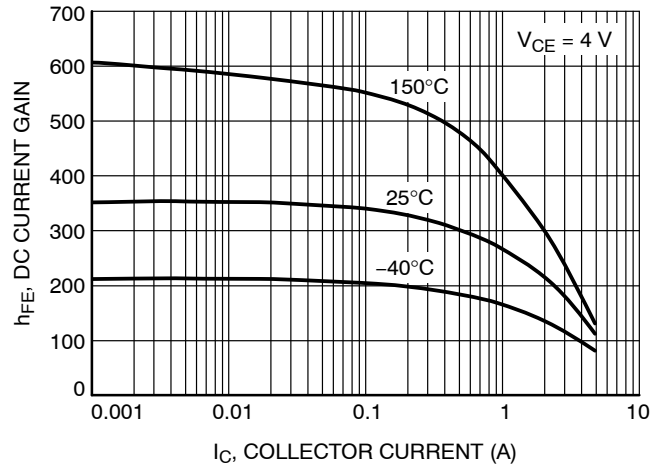


Figure 3. DC Current Gain

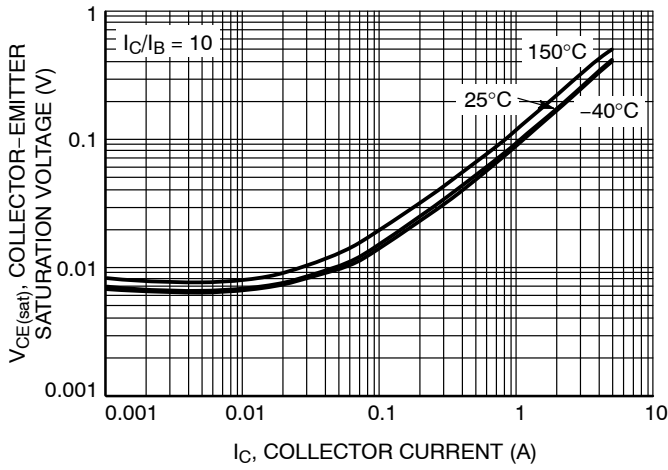


Figure 4. Collector-Emitter Saturation Voltage

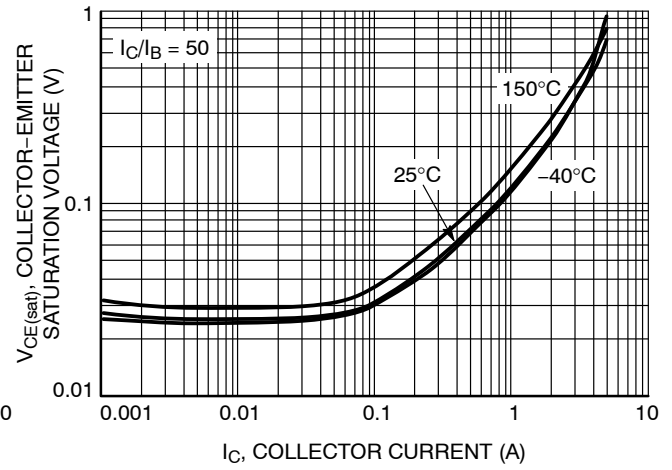


Figure 5. Collector-Emitter Saturation Voltage

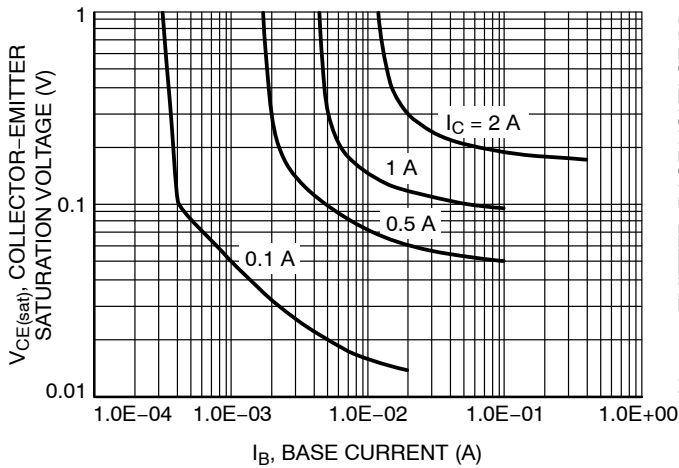


Figure 6. Collector Saturation Region

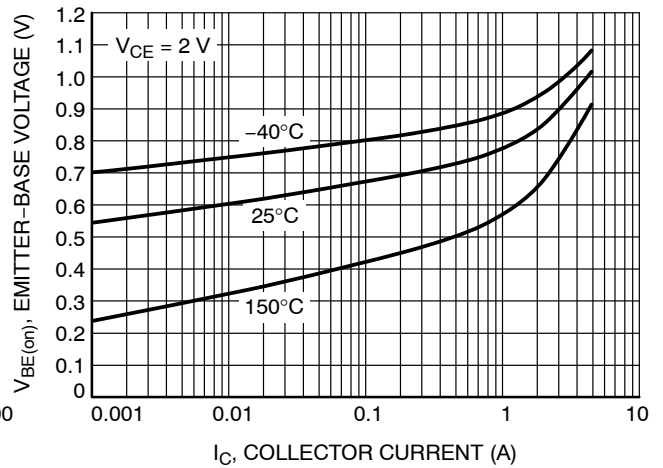


Figure 7. $V_{BE(on)}$ Voltage

TYPICAL CHARACTERISTICS

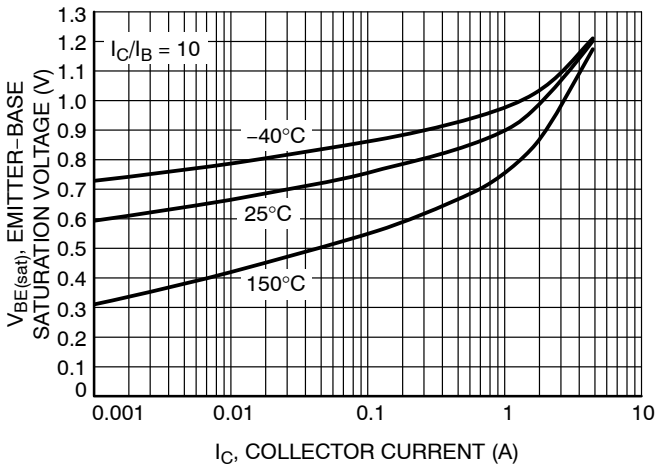


Figure 8. Base-Emitter Saturation Voltage

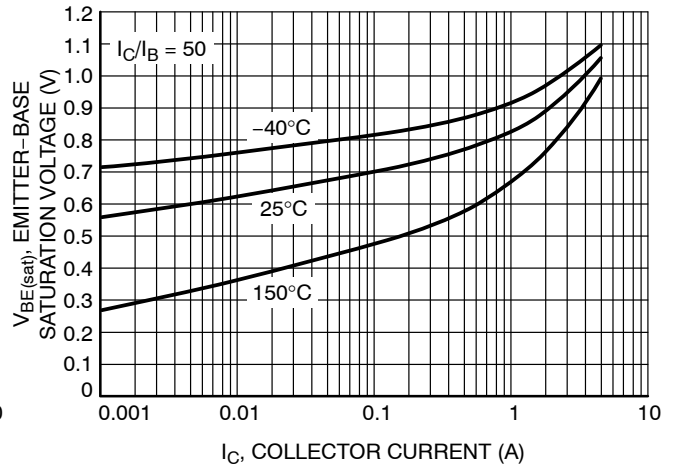


Figure 9. Base-Emitter Saturation Voltage

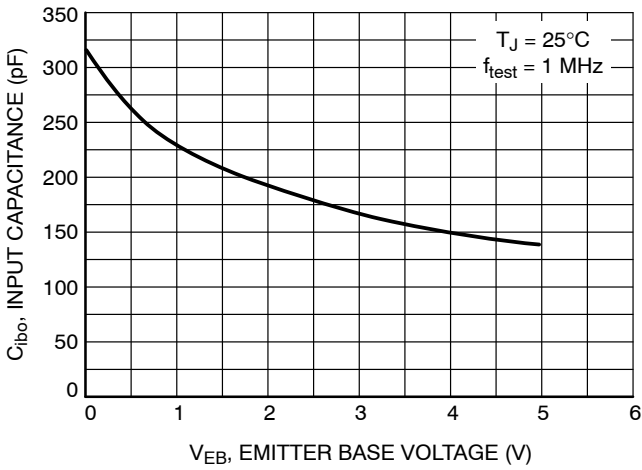


Figure 10. Input Capacitance

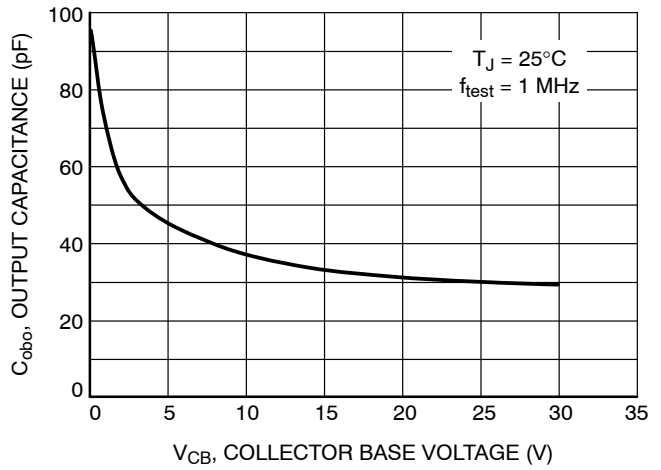


Figure 11. Output Capacitance

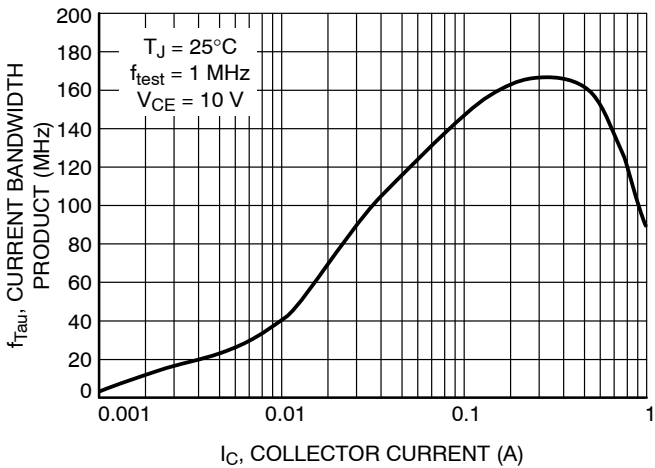


Figure 12. Current-Gain Bandwidth Product

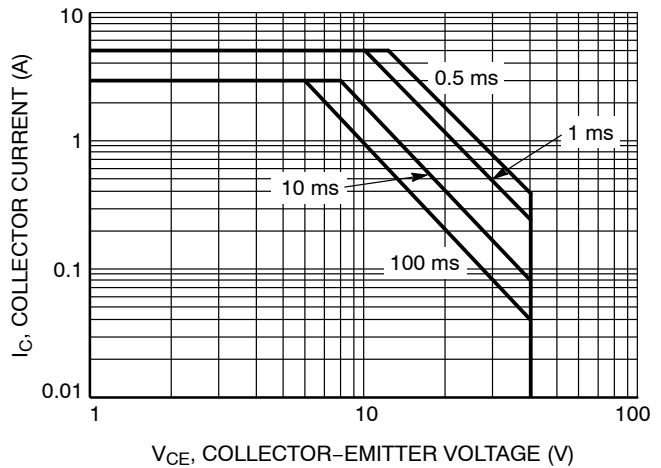


Figure 13. Safe Operating Area

NSS40300CT

ORDERING INFORMATION

Device	Package	Shipping [†]
NSS40300CTWG	LFPAK4 5x6 (Pb-Free)	3,000 / Tape & Reel
NSV40300CTWG*	LFPAK 5x6 (Pb-Free)	3,000 / Tape & Reel

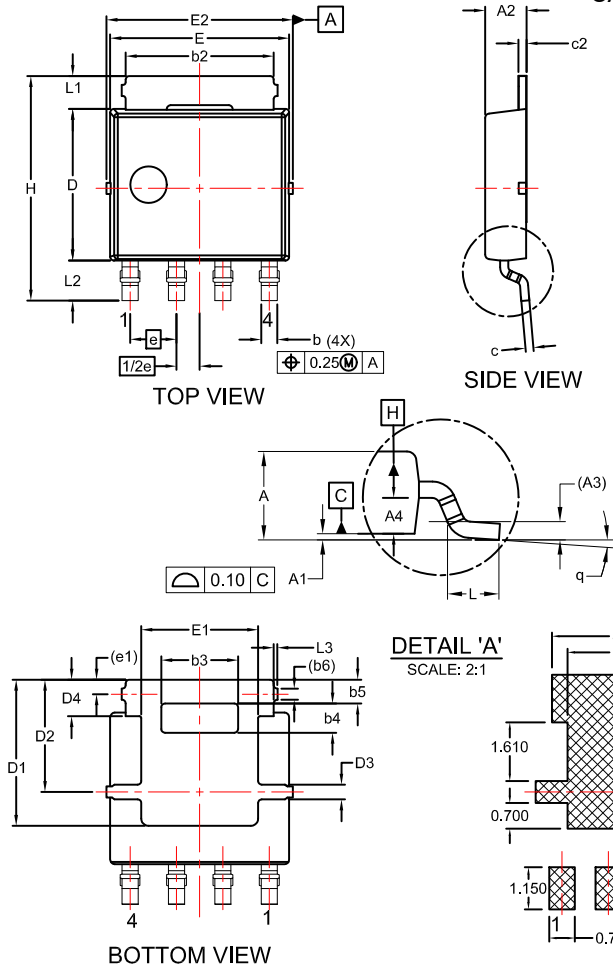
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable

NSS40300CT

PACKAGE DIMENSIONS

LFFPAK4 5x6 CASE 760AB ISSUE C



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

UNIT IN MILLIMETER			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25 REF		
A4	0.45	0.50	0.55
b	0.40	0.45	0.50
b2	3.80	4.10	4.40
b3	2.00	2.10	2.20
b4	0.70	0.80	0.90
b5	0.55	0.65	0.75
b6	0.31 REF		
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.05	4.15	4.25
D1	3.80	4.00	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
D4	0.90	1.00	1.10
E	4.80	4.90	5.00
E1	3.10	3.20	3.30
E2	5.00	5.15	5.30
e	1.27 BSC		
1/2e	0.635 BSC		
e1	0.40 REF		
H	6.00	6.15	6.30
L	0.40	0.65	0.85
L1	0.80	0.90	1.00
L2	0.90	1.10	1.30
L3	0.00	0.10	0.20
q	0°	4°	8°

RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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