STB10N95K5, STF10N95K5, STP10N95K5, STW10N95K5

N-channel 950 V, 0.65 Ω typ., 8 A Zener-protected SuperMESH™ 5 Power MOSFETs in D²PAK, TO-220FP, TO-220 and TO-247

Datasheet - production data

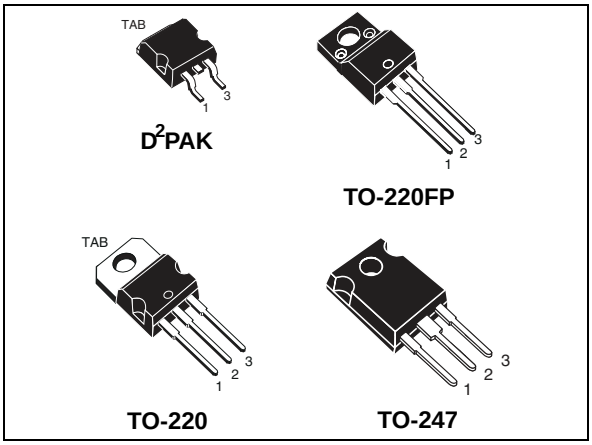
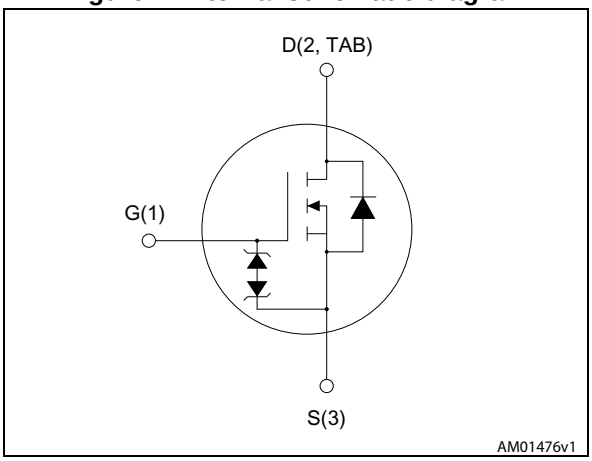


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STB10N95K5	950 V	0.8 Ω	8 A	130 W
STF10N95K5				30 W
STP10N95K5				130 W
STW10N95K5				

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These N-channel Zener-protected Power MOSFETs are designed using ST's revolutionary avalanche-rugged very high voltage SuperMESH™ 5 technology, based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance, and ultra-low gate charge for applications which require superior power density and high efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB10N95K5	10N95K5	D²PAK	Tape and reel
STF10N95K5		TO-220FP	Tube
STP10N95K5		TO-220	
STW10N95K5		TO-247	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP	D²PAK, TO-220, TO-247	
V_{GS}	Gate- source voltage	±30		V
I_D	Drain current (continuous) at T_C = 25 °C	8(1)	8	A
I_D	Drain current (continuous) at T_C = 100 °C	5(1)	5	A
I_{DM} (2)	Drain current (pulsed)	32		A
P_{TOT}	Total dissipation at T_C = 25 °C	30	130	W
I_{AR}	Max current during repetitive or single pulse avalanche	2.5		A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V)	122		mJ
dv/dt (3)	Peak diode recovery voltage slope	4.5		V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	50		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T_C=25 °C)	2500		V
T_j T_{stg}	Operating junction temperature Storage temperature	- 55 to 150		°C

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 8$ A, di/dt $\leq$ 100 A/µs, $V_{DS(peak)} \leq V_{(BR)DSS}$.
4. $V_{SD} \leq 760$ V

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220FP	D²PAK	TO-220, TO-247	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	4.2	0.96		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb max	62.5		62.5	°C/W
$Rt_{hj\text{-}pcb}$(1)	Thermal resistance junction-pcb max		30		°C/W

1. When mounted on 1 inch² FR-4, 2 Oz copper board

2 Electrical characteristics

(Tcase =25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	950			V
I_{DSS}	Zero gate voltage, V_{GS} = 0 drain current	V_{DS} = 950 V			1	µA
		V_{DS} = 950 V, T_C=125 °C			50	µA
I_{GSS}	Gate-body leakage current	V_{GS} = ± 20 V; V_{DS}=0			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4 A		0.65	0.8	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =100 V, f=1 MHz, V_{GS}=0	-	630	-	pF
C_{oss}	Output capacitance		-	50	-	pF
C_{rss}	Reverse transfer capacitance		-	0.6	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 760 V	-	77	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	28	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	6.5	-	Ω
Q_g	Total gate charge	V_{DD} = 760 V, I_D = 8 A V_{GS} =10 V *(see Figure 20)*	-	22	-	nC
Q_{gs}	Gate-source charge		-	5	-	nC
Q_{gd}	Gate-drain charge		-	15	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 475 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 19)*	-	22	-	ns
t_r	Rise time		-	14	-	ns
$t_{d(off)}$	Turn-off-delay time		-	51	-	ns
t_f	Fall time		-	15	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		8	A
I_{SDM} (1)	Source-drain current (pulsed)		-		32	A
V_{SD} (2)	Forward on voltage	I_{SD} = 8 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs V_{DD}= 60 V *(see Figure 21)*	-	404		ns
Q_{rr}	Reverse recovery charge		-	5.2		µC
I_{RRM}	Reverse recovery current		-	25.5		A
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs V_{DD}= 60 V T_J = 150 °C *(see Figure 21)*	-	596		ns
Q_{rr}	Reverse recovery charge		-	6.9		µC
I_{RRM}	Reverse recovery current		-	23		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK and TO-220

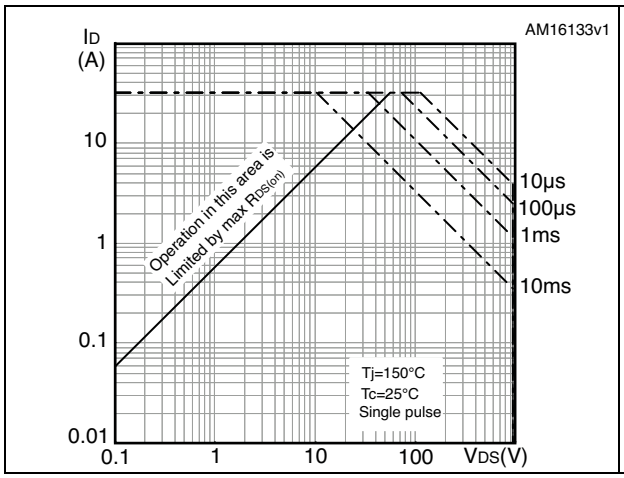


Figure 3. Thermal impedance for D²PAK and TO-220

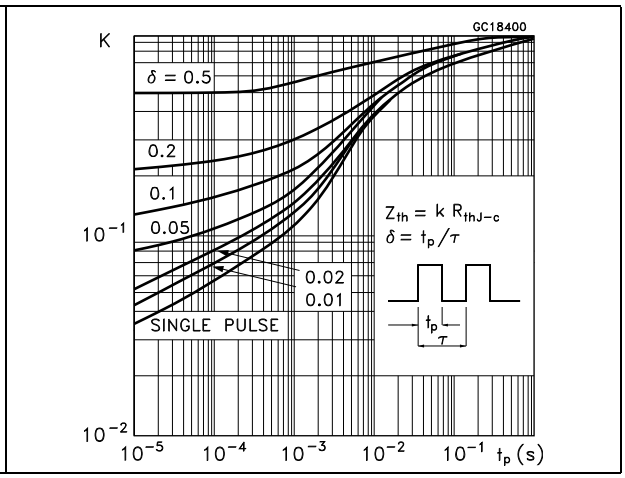


Figure 4. Safe operating area for TO-220FP

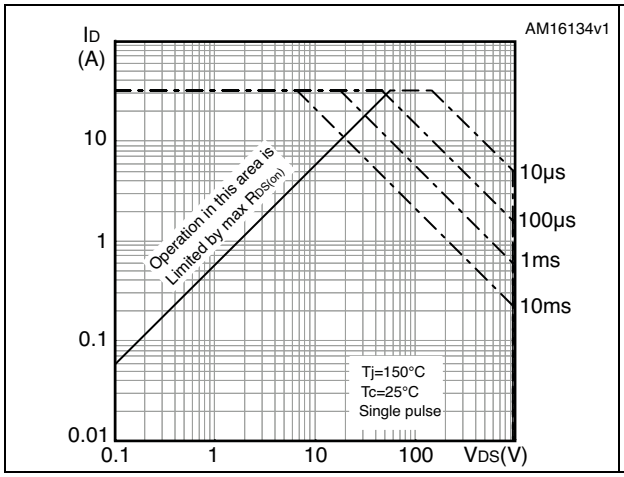


Figure 5. Thermal impedance for TO-220FP

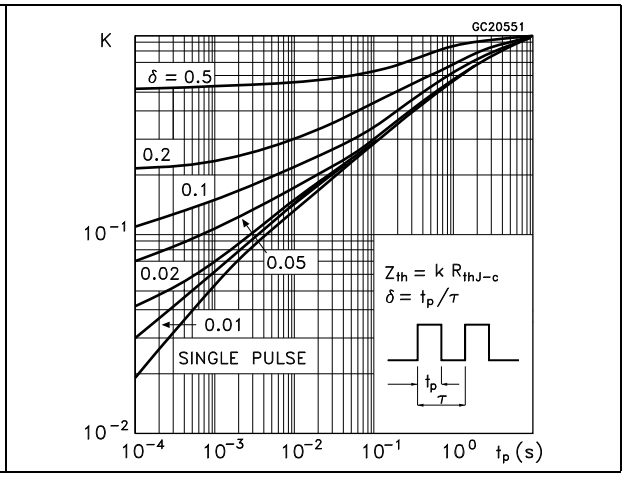


Figure 6. Safe operating area for TO-247

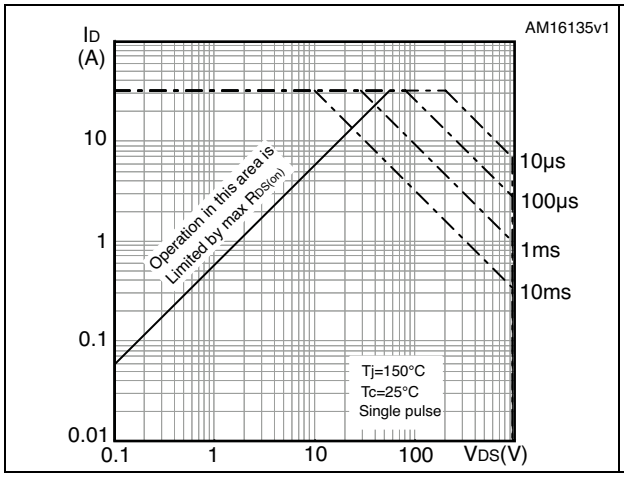


Figure 7. Thermal impedance for TO-247

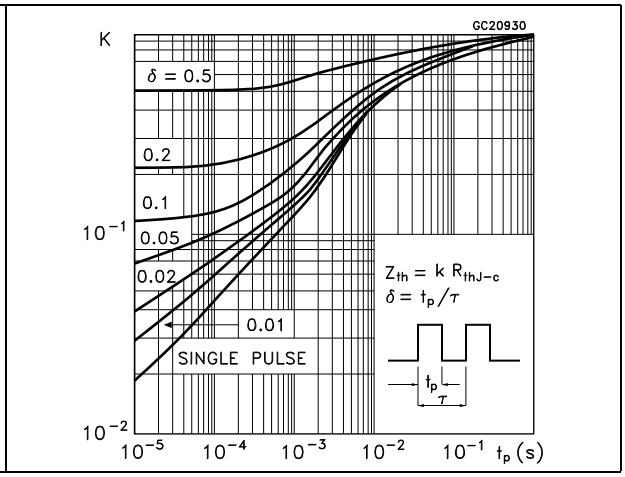


Figure 8. Output characteristics

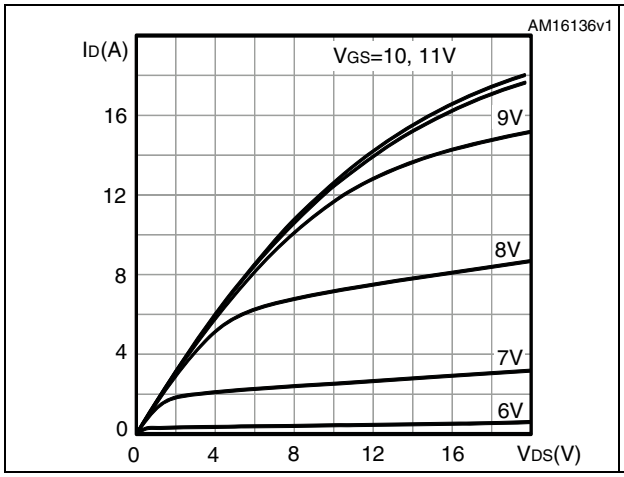


Figure 9. Transfer characteristics

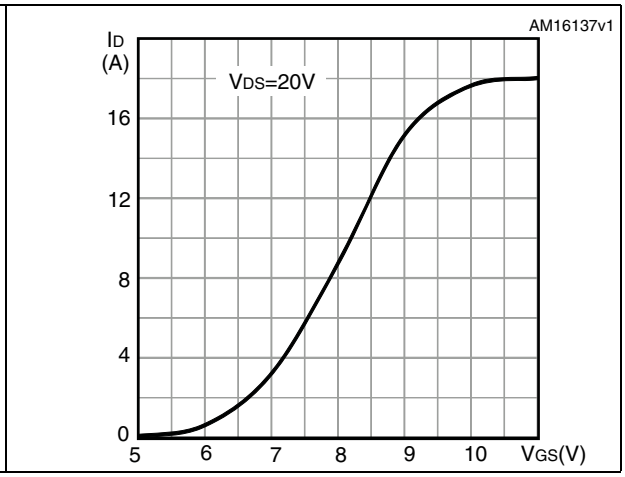


Figure 10. Gate charge vs gate-source voltage

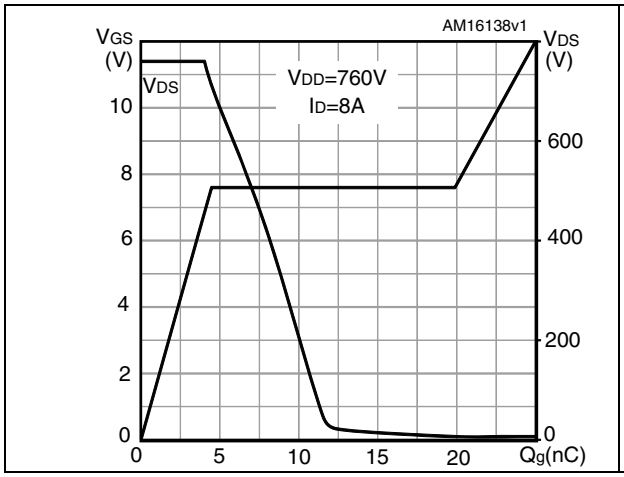


Figure 11. Static drain-source on-resistance

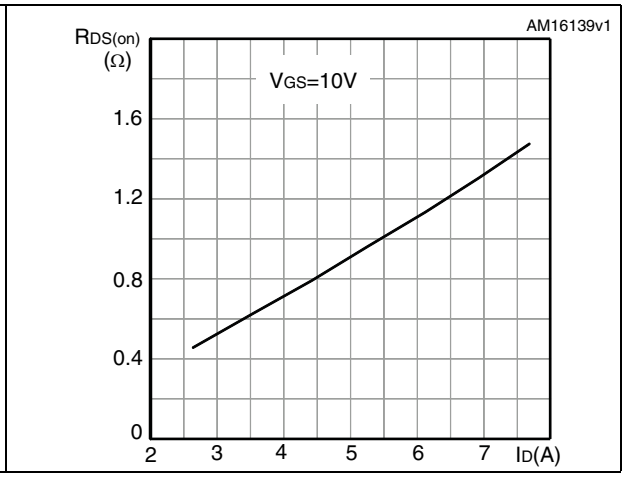


Figure 12. Capacitance variations

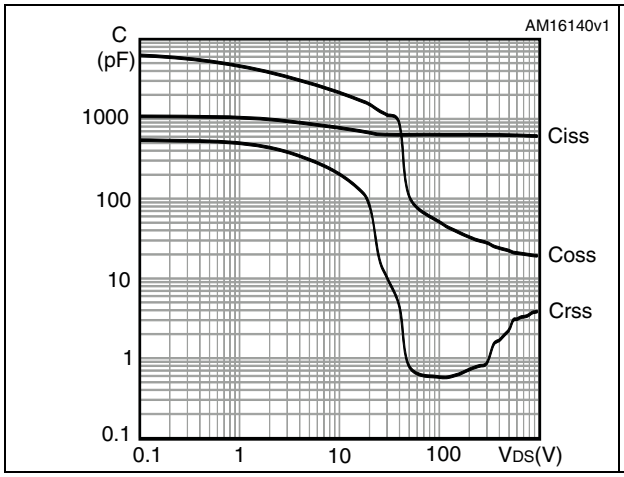


Figure 13. Output capacitance stored energy

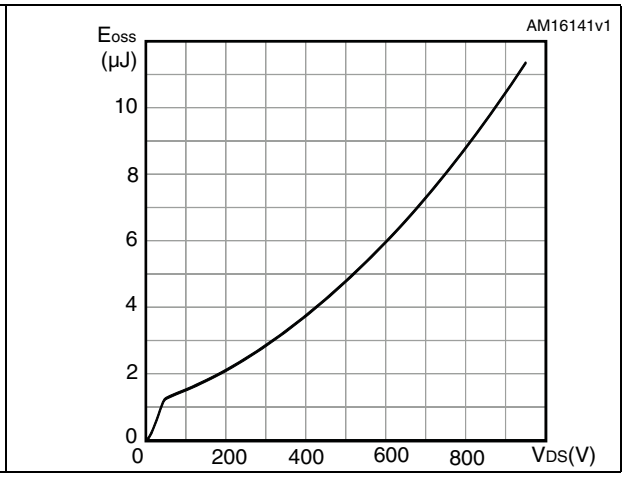


Figure 14. Normalized gate threshold voltage vs temperature

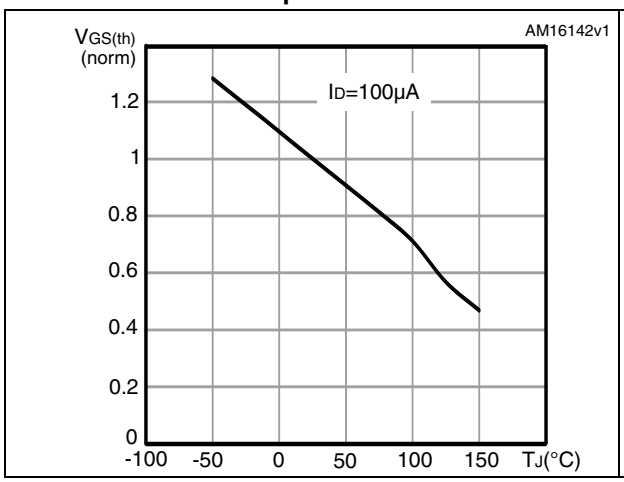


Figure 15. Normalized on-resistance vs temperature

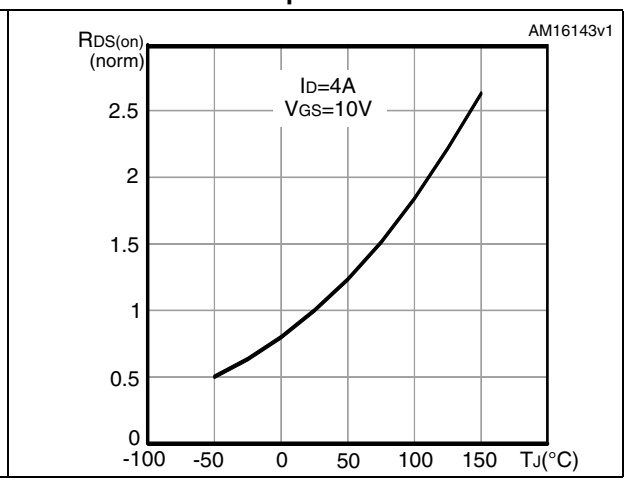


Figure 16. Normalized V_{DS} vs temperature

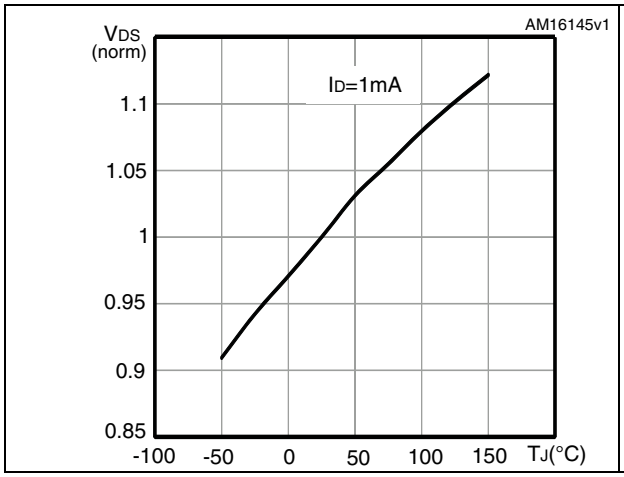


Figure 17. Source-drain diode forward characteristics

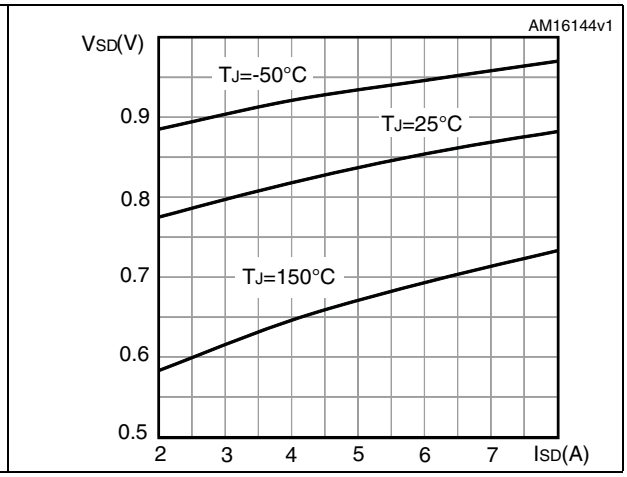
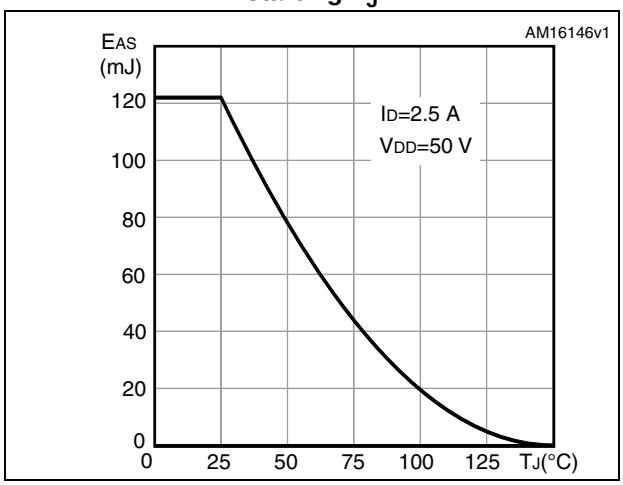


Figure 18. Maximum avalanche energy vs starting T_J



3 Test circuits

Figure 19. Switching times test circuit for resistive load

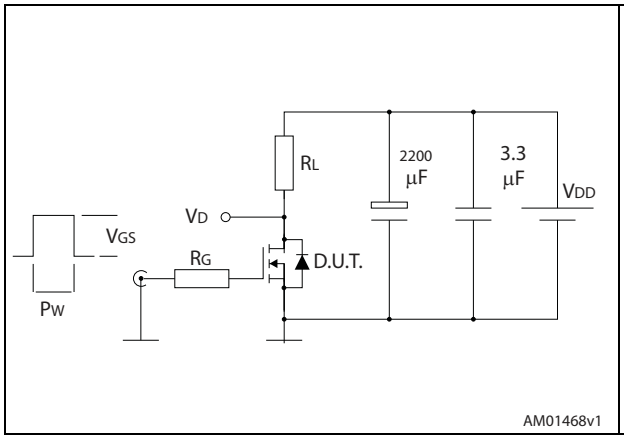


Figure 20. Gate charge test circuit

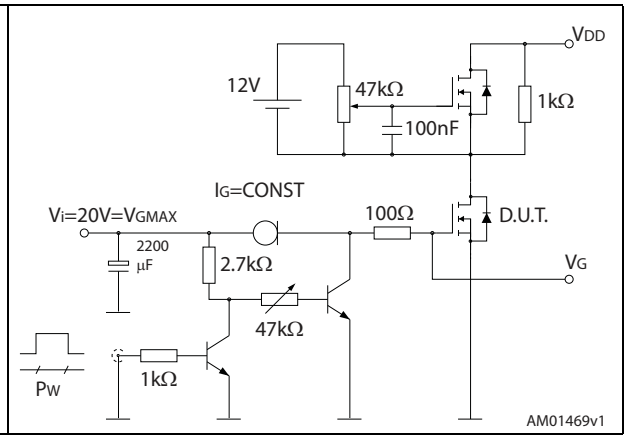


Figure 21. Test circuit for inductive load switching and diode recovery times

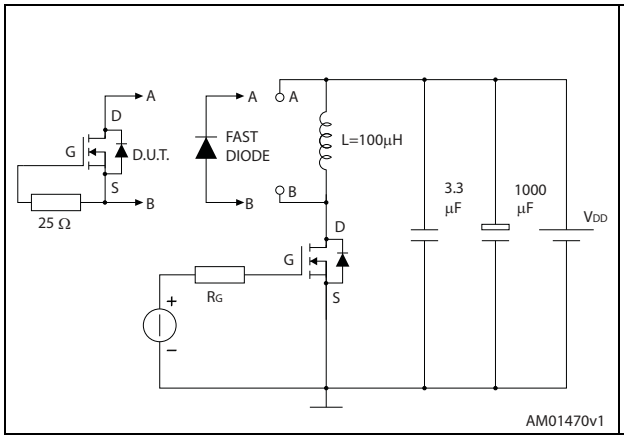


Figure 22. Unclamped inductive load test circuit

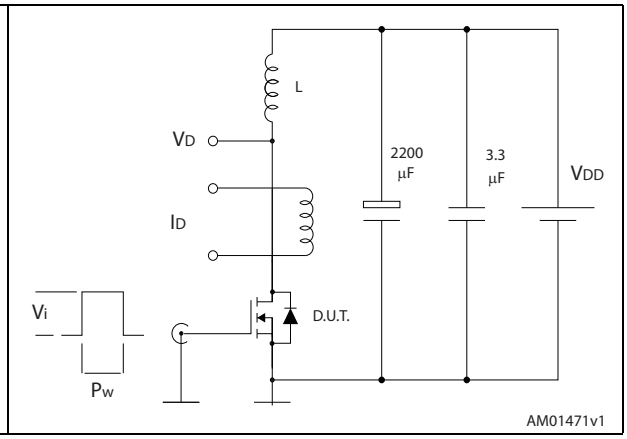


Figure 23. Unclamped inductive waveform

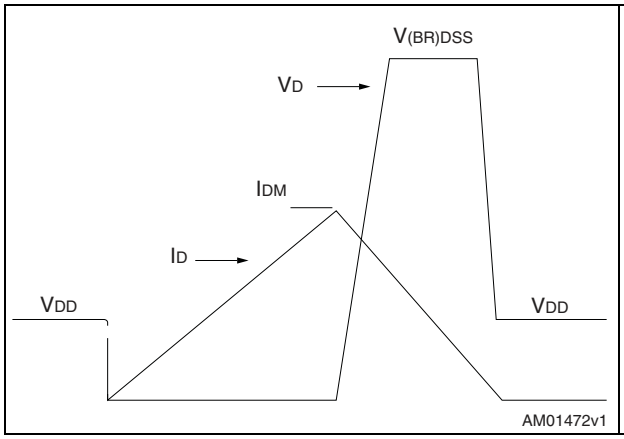
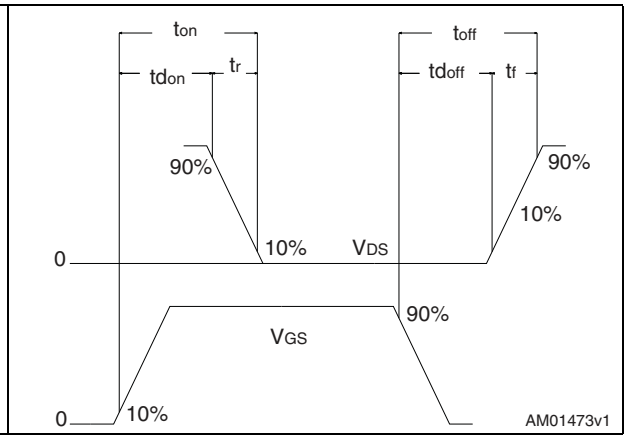


Figure 24. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

Figure 25. D²PAK (TO-263) drawing

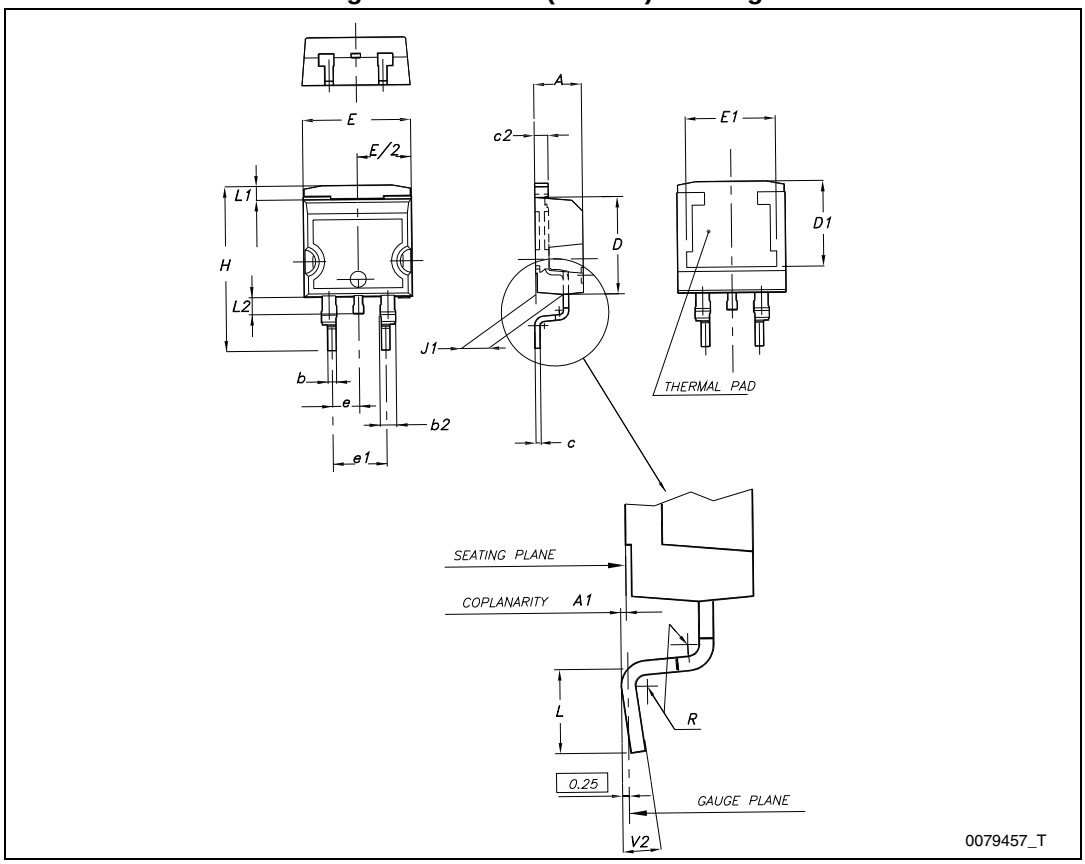


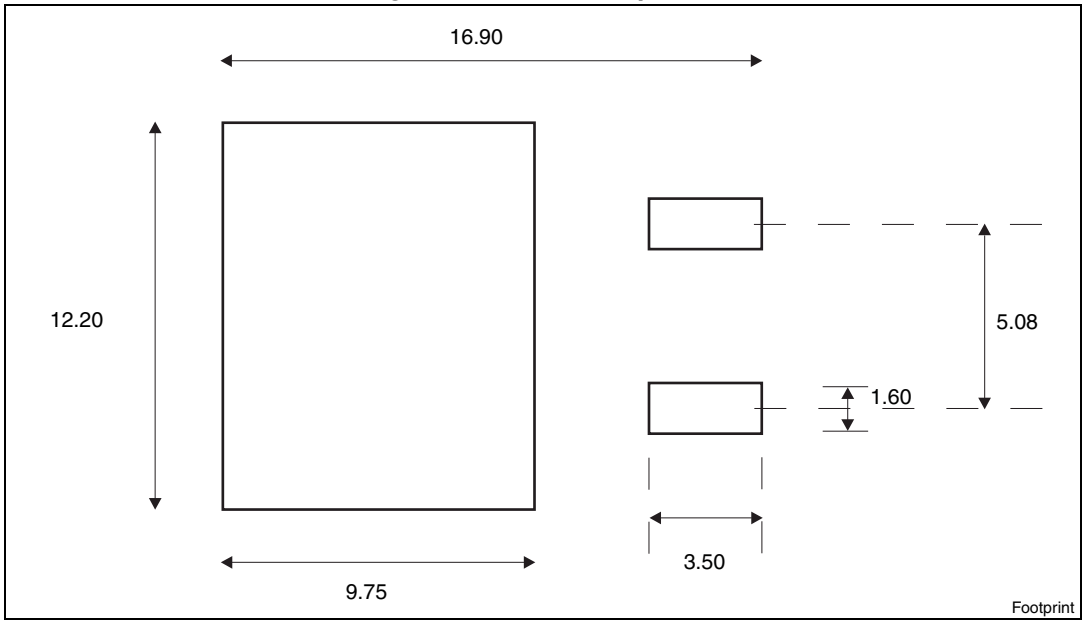
Table 9. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85

Table 9. D²PAK (TO-263) mechanical data (continued)

Dim.	mm		
	Min.	Typ.	Max.
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 26. D²PAK footprint[(a)]



a. All dimension are in millimeters

Figure 27. TO-220FP drawing

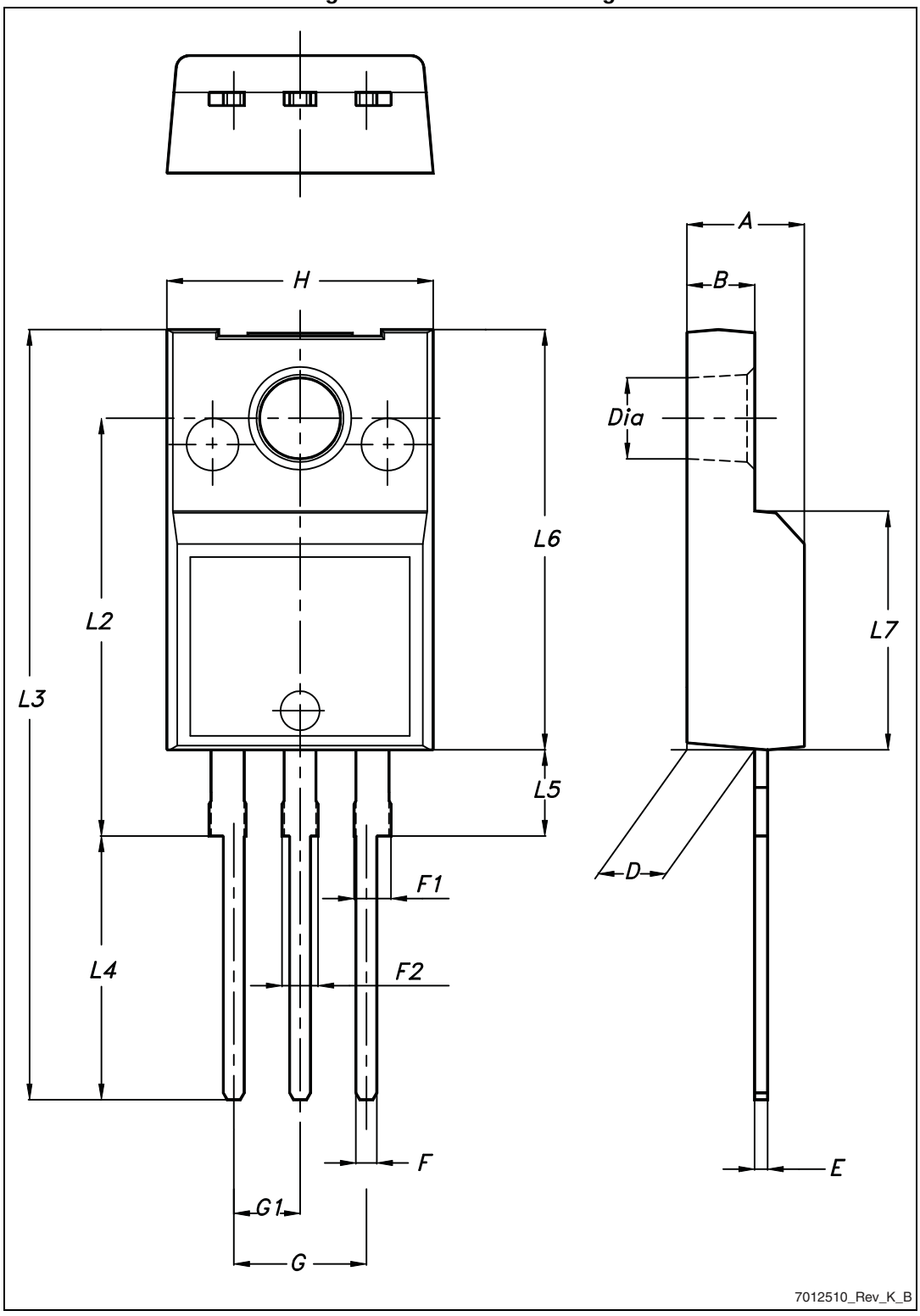


Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 28. TO-220 type A drawing

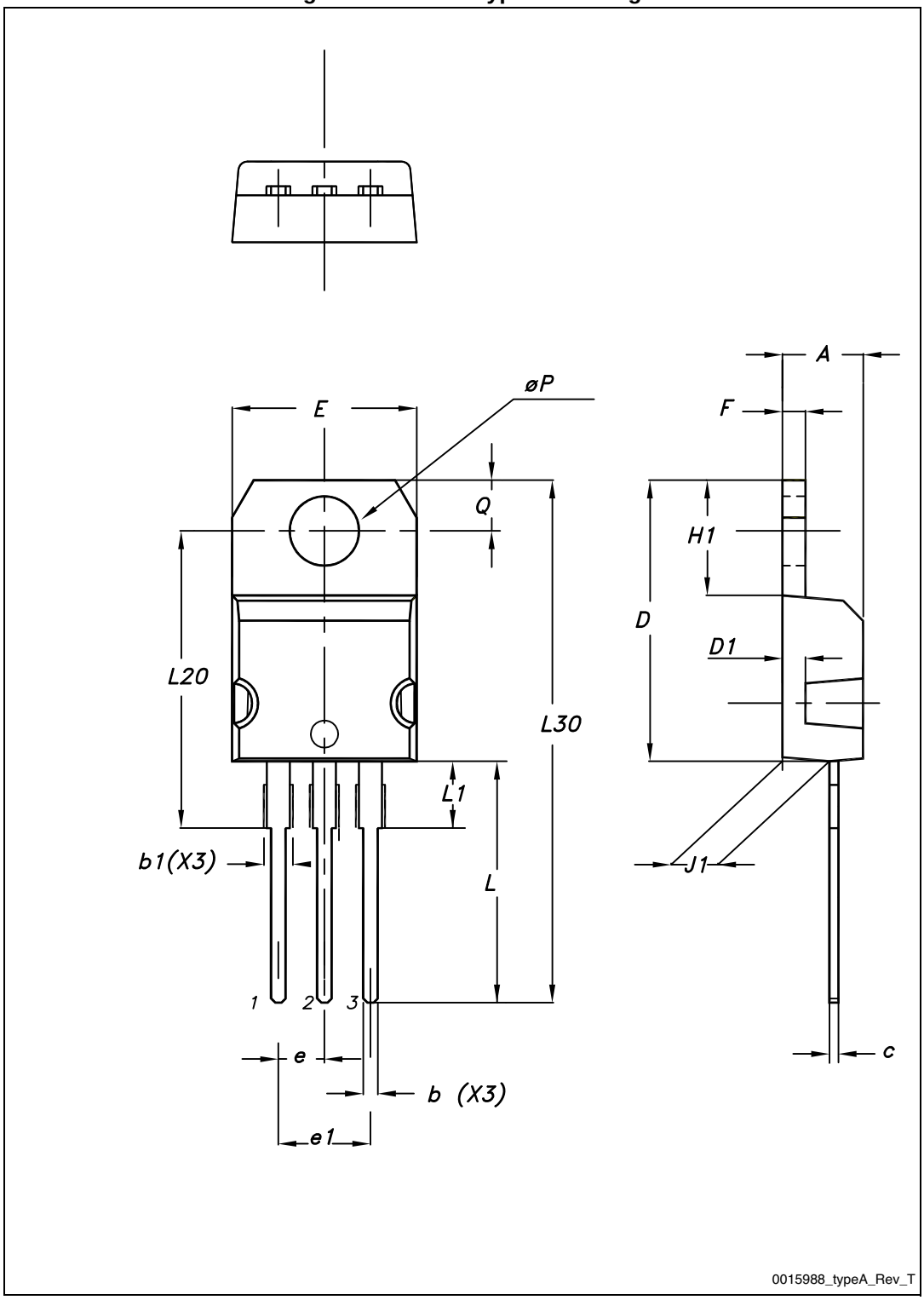


Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 29. TO-247 drawing

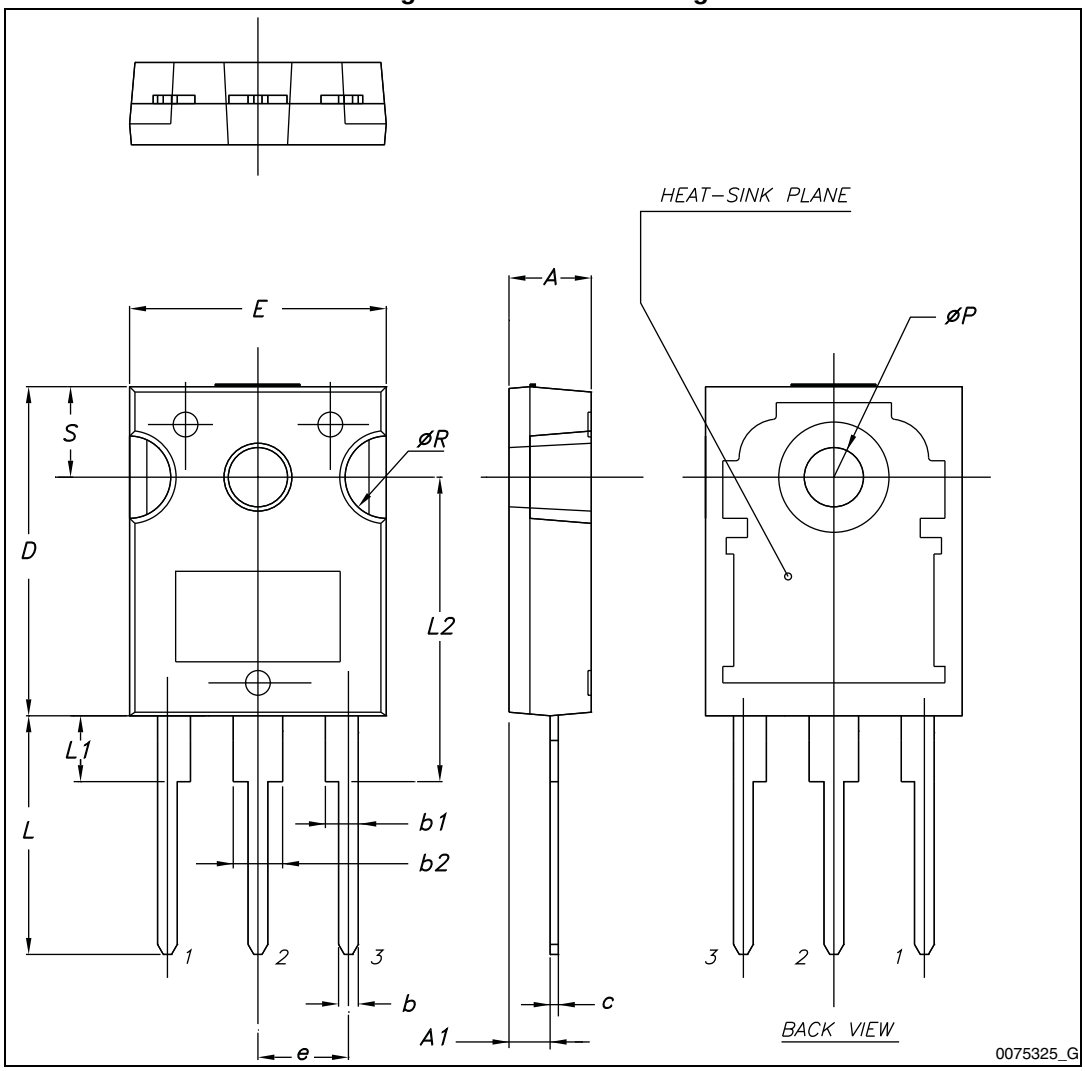


Table 12. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75

Table 12. TO-247 mechanical data (continued)

Dim.	mm.		
	Min.	Typ.	Max.
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
∅P	3.55		3.65
∅R	4.50		5.50
S	5.30	5.50	5.70

5 Packaging mechanical data

Figure 30. Tape

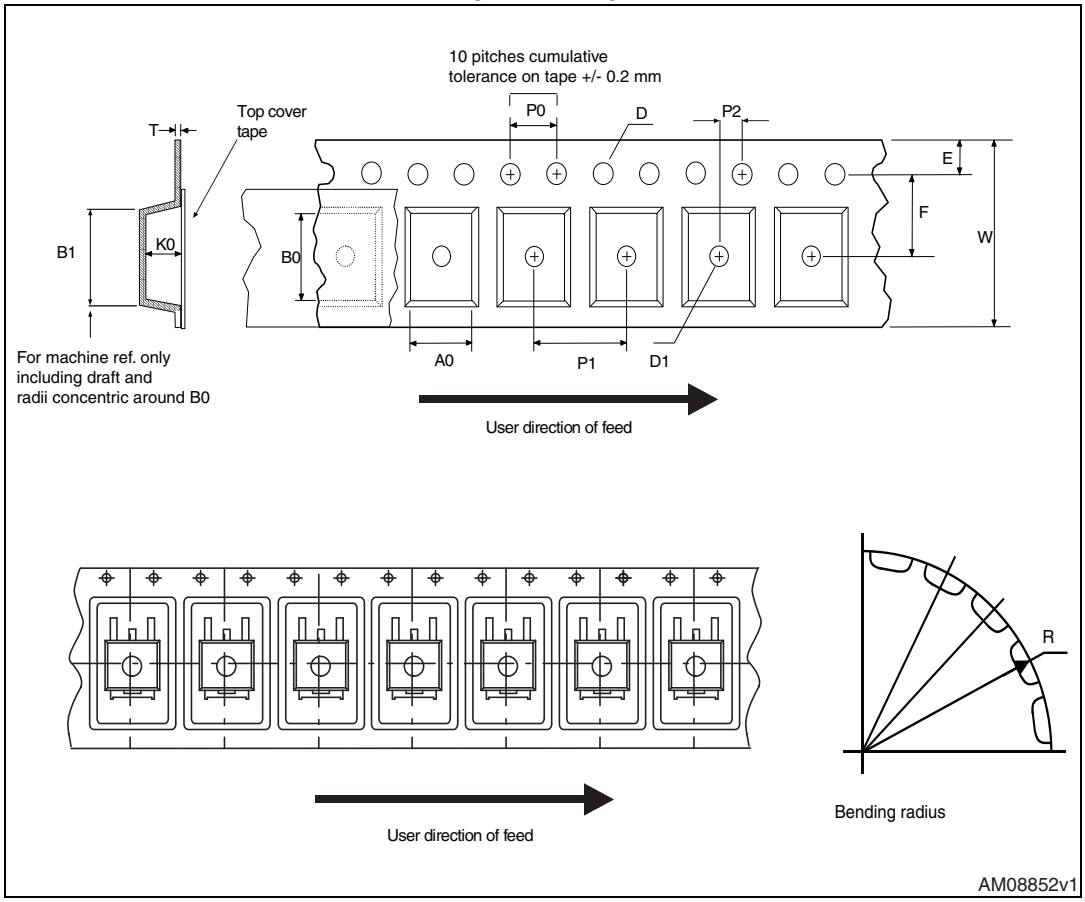


Figure 31. Reel

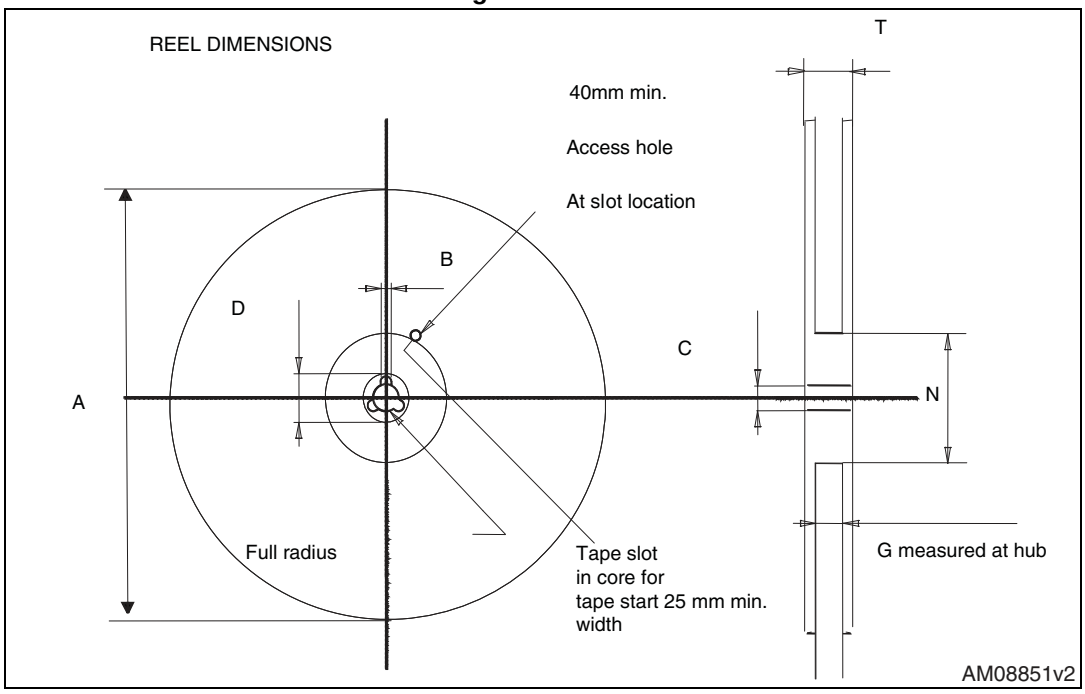


Table 13. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Table 14. Document revision history

Date	Revision	Changes
24-Jun-2013	1	First release.
07-Oct-2013	2	– Added: D^2PAK package – Modified: note *4* in *Table 2* – Added: Thermal resistance junction-pcb max parameter – Modified: typical values in *Table 5*, *6* and *7* – Added: *Section 2.1: Electrical characteristics (curves)* – Updated: *Section 4: Package mechanical data* – Minor text changes
29-Jan-2014	3	– Datasheet status promoted from preliminary data to production data – Minor text changes

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