MyMENSCH™

Microcomputer

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DOCUMENT REVISION HISTORY

Version	Date	Author	Description
1.0	13-May-2019	Bill Mensch, David Gray	Initial Document Entry
1.0	12-July-2019	Bill Mensch, David Gray	Update Section 2.1 and 2.3 to reflect REV A, B, and C FPGA Assignments.

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1.0 Introduction

MyMENSCH™ (W65Cx65MMC) is a small printed circuit board (PCB), 1.50" x 2.75", designed for rapid prototyping of microcontrollers for sensing, processing, communicating and actuating (SPCA). MyMENSCH™ was designed for developing customized application specific versions of the W65C165i1M08SC, W65C165i1M08SA, and W65C165i1M16SA 8-bit and W65C265i1M16SA 8/16-bit families of microcontrollers. Visit http://wdc65xx.com/MyMENSCH/ for additional information.

1.1 Feature List

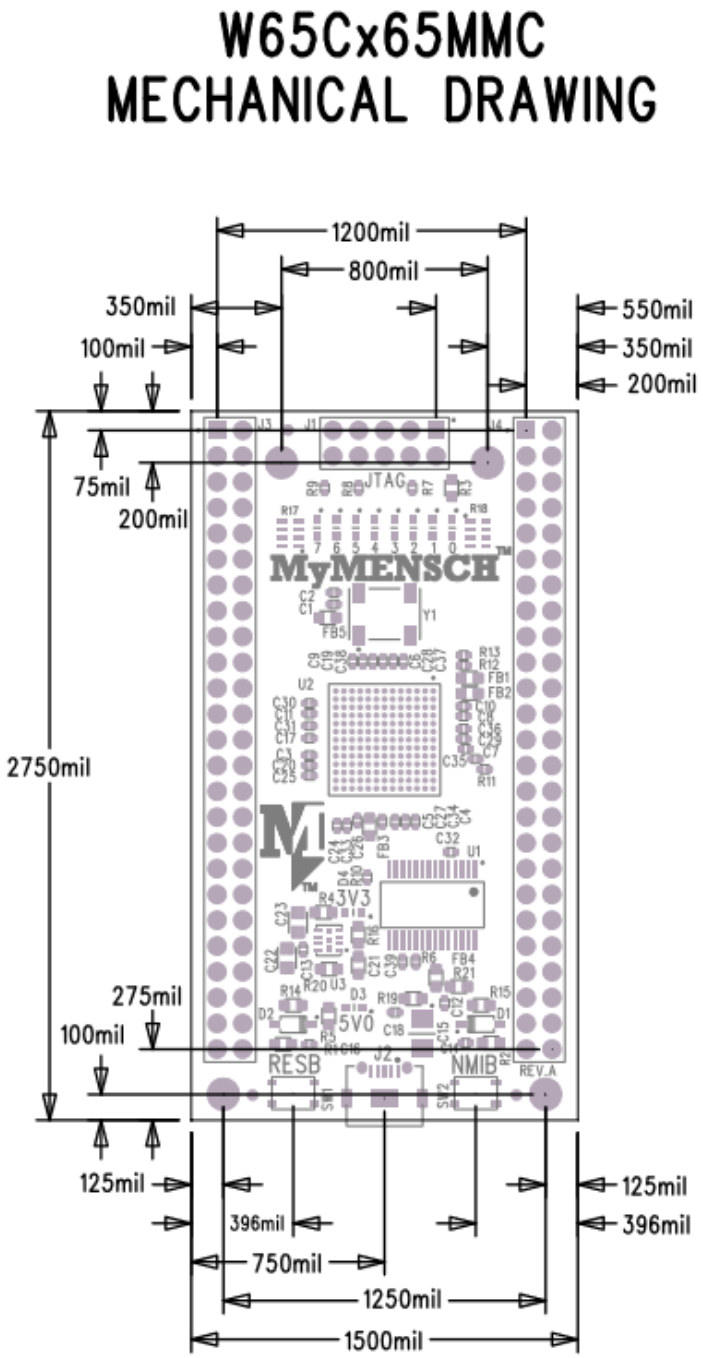
- Designed for MAX10 169 BGA packaged FPGAs
- Designed for FPGA to ASIC Design and Manufacturing flow
- Voltage regulated 3.3 volts derived from USB 5.0 volt supply.
- All IO pins are 3.3V.
- FTDI245 or FTDI240x USB-to-parallel Code and Debug port available on Rev-A and B
- CH340C USB-to-UART Code and Debug port on Rev-C
- MyMENSCH™ Monitor for application use with selected peripherals
- WDCTools Assembly and C language development support
- Four (4) 3v3 power and four (4) VSS pins
- JTAG pins available on J4 on Rev-A
- Dedicated AGND, ADC_IN0, 3v3REF, 5vBAT, and VIA_B_PB6 on J4 are available on Rev-B and C
- Two 2x25 pin connectors for 92 IO pins provide quick prototyping
- LEDs connected to 8 GPIO ports for debug and status indicators
- Rapid prototyping daughter board concept support
- RESB and NMIB buttons
- 14.7456 MHz oscillator hooked to ball G5 of the FPGA.
- JTAG port for test, debug, FLASH memory, and programmable logic

1.2 Intel MAX 10 Device Maximum Resources

Maximum Resource Counts for Intel MAX 10 Devices			
Resource Device	**M08SC**	**M08SA**	**M16SA**
Logic Elements (LE) (K)	8	8	16
M9K Memory Blocks (1 KB)	42	42	61
User Flash Memory Max (KB) with EKP	32	114	184
User Flash Memory Max (KB) without EKP	90	172	296
18 × 18 Multiplier	24	24	45
PLL (Max)	1	1	1
169 BGA Package	Yes	Yes	Yes
GPIO (Max IO Count 169 BGA Package)	130	130	130
Internal Configuration Image	1	1	1
ADC	0	1	1

1.3 Mechanical Drawing Diagram

The mechanical drawing indicates the measurements of significant items and locations of the W65Cx65MMC. There are three version Rev-A, Rev-B, and Rev-C shown at the bottom of J4. Rev-A and Rev-B have FTDI245 and FTDI240X USB-to-Parallel code and debug ports and Rev-C has a CH340C USB-to-UART code and debug port. Rev-A has JTAG pins on J4 while Rev-B and Rev-C has a dedicated analog ground AGND, analog input ADC_IN0, analog reference 3v3REF, 5vBAT for suppling 5 volts or receiving backup battery from a daughterboard, and VIA_B_PB6 on J4.



1.4 Board Schematic

The board schematics for Rev-A, Rev-B, and Rev-C are available on-line at WDC65xx.com/support/documentation.

1.5 Power Supply Considerations

See the USB 5v0 specification for more information. MyMENSCH™ operates all circuitry from 3v3. Rev-A has JTAG pins on J4 instead of analog AGND, ADC_IN0, 3v3REF, and 5vBAT available on Rev-B and Rev-C.

1.6 Intel PSG MAX10 FPGA Considerations

The signals on the FPGA are **not** meant to work with 5V inputs. Applying a 5V input to the FPGA could cause damage. See the Intel PSG MAX10 Datasheets for more information.

1.7 RESET and NMIB Buttons

RESB signal is hooked to FPGA Ball H4. NMIB signal is hooked to FPGA Ball H5.

1.8 Light Emitting Diodes (LEDs)

MyMENSCH™ Microcomputer has 8x LEDs connected to GPIO_B within the W65C165i1 design. The LED furthest to the left is LED7 and is connected to GPIO_B7. The LED furthest to the right is LED0 and is connected to GPIO_B0. The FPGA ball assignments are as follows:

GPIO_B	LED Signal	FPGA Ball
GPIO_B7	LED7	M2
GPIO_B6	LED6	M1
GPIO_B5	LED5	L2
GPIO_B4	LED4	L1
GPIO_B3	LED3	K2
GPIO_B2	LED2	K1
GPIO_B1	LED1	J2
GPIO_B0	LED0	J1

2.0 Connectors

Following are descriptions of W65Cx65MMC connectors.

2.0 JTAG Connector J1

The top J1 JTAG port is used for test, debug, FLASH, and Programmable logic configuration.

J1 – JTAG Connector					
Pin	*Signal Name*	*FPGA Ball*	*Pin*	*Signal Name*	*FPGA Ball*
1	TCK	G2	2	GND	-
3	TDO	F6	4	VCC	-
5	TMS	G1	6	NC	-
7	NC	-	8	JTAGEN	-
9	TDI	F5	10	GND	-

2.1 J2 USB Connector and FTDI245/FTDI240x Code/Debug Port

Connector J2 is the uUSB connector that provides 5V power to the board. The USB signals are connected to a FTDI245 (Rev-A) or FTDI240x (Rev-B) USB to FIFO interface controller. The Code and Debug port interface is through two GPIO ports connected to the Max10 FPGA to interface with the FTDI245/FTDI240x USB controller. This interface is similar to the interface that is on the W65C02SXB and W65C816SXB development boards. Below is a table showing each FTDI Signal and corresponding GPIO signal:

GPIO	FTDI Signal	FPGA Ball Rev-A	FPGA Ball Rev-B
GPIO_C7	USB_D7	F10	F10
GPIO_C6	USB_D6	D13	E9
GPIO_C5	USB_D5	D11	H8
GPIO_C4	USB_D4	G10	F13
GPIO_C3	USB_D3	D12	J7
GPIO_C2	USB_D2	G9	G9
GPIO_C1	USB_D1	F9	F9
GPIO_C0	USB_D0	E10	E12
GPIO_D0	USB_TXEB	H8	D11
GPIO_D1	USB_RXFB	E9	D13
GPIO_D2	USB_RDB	F13	G10
GPIO_D3	USB_WR	E12	E10
GPIO_D5	USB_PWRENB	E13	H9

2.2 J2 USB Connector and CH340C Code/Debug Port (Rev-C)

Connector J2 is the uUSB connector that provides 5V power to the board. The USB signals are connected to a CH340C USB to Serial interface controller. The Code and Debug port interface is through two GPIO ports connected to the Max10 FPGA to interface with the CH340C USB controller. This interface is similar to the interface that is on the W65C134SXB and W65C265SXB development boards. Below is a table showing each CH340 Signal and corresponding FPGA signal:

FPGA SIGNAL	CH340 Signal	FPGA Ball
ACIA_A_RXD	USB_TXD	G9
ACIA_A_TXD	USB_RXD	F13
RTSB_A_E7	USB_CTSB	G10
CTSB_A_E1	USB_RTSB	E13
340_RESB	USB_DTRB	F9

2.3 Left IO Connector J3 Ball Assignments

The J3 left connector has 46 IO, 2x 3v3 power and 2x VSS pins. Signal Names for individual microcontrollers are shown in the microcontroller datasheet. NA are Non-Assigned logic IO pins that are assigned by the FPGA microcontroller chosen.

J3 – Left Expansion Connector					
Pin	***Signal Name***	***(Rev-A) FPGA Ball (Rev-B,C)***	***Pin***	***Signal Name***	***FPGA Ball***
1	VSS	-	2	VDD	-
3	NA	L4	4	NA	L3
5	NA	K6	6	NA	K5
7	NA	M3	8	NA	N2
9	NA	M4	10	NA	N3
11	NA	M5	12	NA	N4
13	NA	L5	14	NA	N5
15	NA	N7	16	NA	N6
17	NA	N8	18	NA	M7
19	NA	M9	20	NA	M8
21	NA	M10	22	NA	N9
23	NA	M11	24	NA	N10
25	NA	N12	26	NA	N11
27	NA	M13	28	NA	M12
29	NA	L13	30	NA	L12
31	NA	K13	32	NA	K12
33	NA	K8	34	NA	J8
35	NA	J9	36	NA	L10
37	NA	K10	38	NA	L11
39	NA	K11	40	NA	J10
41	NA	(H9) or (J12)	42	NA	H10
43	NA	(J12) or (K7)	44	NA	J13
45	NA	H13	46	NA	G12
47	NA	G13	48	NA	F12
49	VDD	-	50	VSS	-

2.4 Right IO Connector J4 Ball Assignments

The J4 right connector has 46 IO, 2x 3v3 power and 2x VSS pins. Signal names for individual microcontrollers are shown in the microcontroller datasheet. NA are Non-Assigned logic pins. NA (ADC_Inx) are dual function pins that can be either logic IO or analog input pins. JTAG pins are available on Rev-A not on Rev-B and Rev-C.

J4 – Right Expansion Connector					
Pin	***Signal Name***	***FPGA Ball***	***Pin***	(Rev-A) ***Signal Name*** (Rev-B,C)	***(Rev-A) FPGA Ball (Rev-B,C)***
1	VDD	-	2	VSS	-
3	NA	H3	4	(JTAG_TCK) or (AGND)	(G2) or (E2)
5	NA	H1	6	(JTAG_TDI) or (ADC_IN0)	(F5) or (D2)
7	NA	H2	8	(JTAG_TDO) or (3v3REF)	(F6) or (D3)
9	NA (ADC_IN5)	F1	10	(JTAG_TMS) or (5vBAT)	(G1) or (-)
11	NA (ADC_IN6)	E1	12	(JTAG_EN) or (VIA_B_PB6)	(E5) or (F4)
13	NA (ADC_IN7)	C1	14	NA (ADC_IN1)	D1
15	NA (ADC_IN8)	B1	16	NA (ADC_IN2)	C2
17	NA	B2	18	NA (ADC_IN3)	E3
19	NA	A2	20	NA (ADC_IN4)	E4
21	NA	B3	22	NA	E6
23	NA	B4	24	NA	A3
25	NA	B5	26	NA	A4
27	NA	B6	28	NA	A5
29	NA	B7	30	NA	A6
31	NA	A7	32	NA	D9
33	NA	A8	34	NA	E8
35	NA	C9	36	NA	F8
37	NA	C10	38	NA	A9
39	NA	B10	40	NA	A10
41	NA	B11	42	NA	A11
43	NA	B12	44	NA	A12
45	NA	B13	46	NA	C11
47	NA	C13	48	NA	C12
49	VSS	-	50	VDD	-

3.0 Notices and Ordering Information

3.1 FCC Compliance

The Western Design Center, Inc. (WDC) provides the enclosed product under the following conditions: This board is intended for use for Engineering Development or Evaluation Purposes ONLY and is not considered by WDC to be a finished consumer product. This board should be handled with caution using good electronics handling practices. This board is compliant per RoHS/Green directives. It does not fall within the scope of directives such as FCC, CE, and UL. It generates uses and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules.

3.2 Ordering Information

The W65Cx65MMC_Rev-A, W65Cx65MMC_Rev-B, and W65Cx65MMC_Rev-C is available from WDC Direct and our distribution partners. For information please visit: http://wdc65xx.com/MyMENSCH/