1.2MHz/1.2A Buck Converter with Programmable Average Input Current Limit

General Description

The RT8032 is a synchronous, step-down DC/DC converter with input current limit function. The average input current limit can be programmed by an external resistor. Its input voltage range is from 3V to 5.5V and provides an adjustable regulated output voltage from 0.8V to 5V while delivering up to 1.2A of output current. The internal synchronous low on-resistance power switches increase efficiency and eliminate the need for an external Schottky diode. Current mode operation with external compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

The RT8032 is operated in forced continuous PWM Mode which minimizes ripple voltage and reduces the noise and RF interference. The 100% duty cycle in Low Dropout Operation can maximize the battery life.

Ordering Information

RT8032□□

- Package Type
  QW : WDFN-12L 4x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

Features

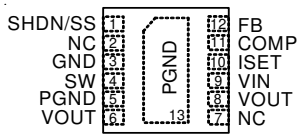
- **Programmable Average Input Current Limit**
- **3V to 5.5V Input Range**
- **1.2A Output Current**
- **Up to 95% Efficiency**
- **1.2MHz Switching Frequency**
- **No Schottky Diode Required**
- **Force Continues Mode Operation**
- **Low $R_{DS(ON)}$ Internal Switches : 230mΩ**
- **Small 12-Lead WDFN Package**
- **External Compensation for Optimal Transient Response**
- **External Soft-Start**
- **Input Over Voltage Protection**
- **RoHS Compliant and Halogen Free**

Applications

- Distributed Power Systems
- Battery Charger
- DSL Modems
- Pre-Regulator for Linear Regulators
- 3G/3.5G Data Card

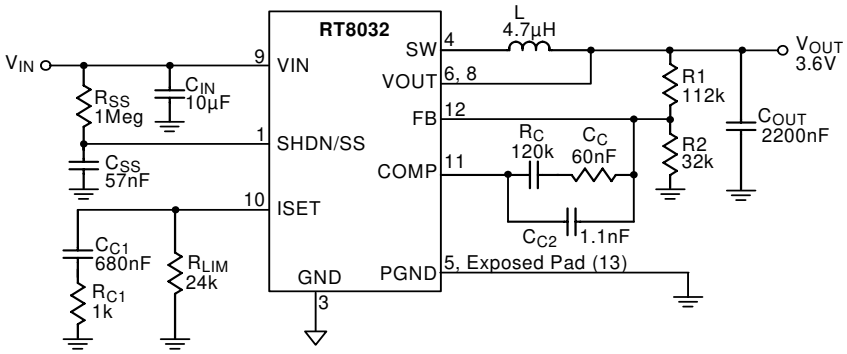
Pin Configurations

(TOP VIEW)



WDFN-12L 4x3

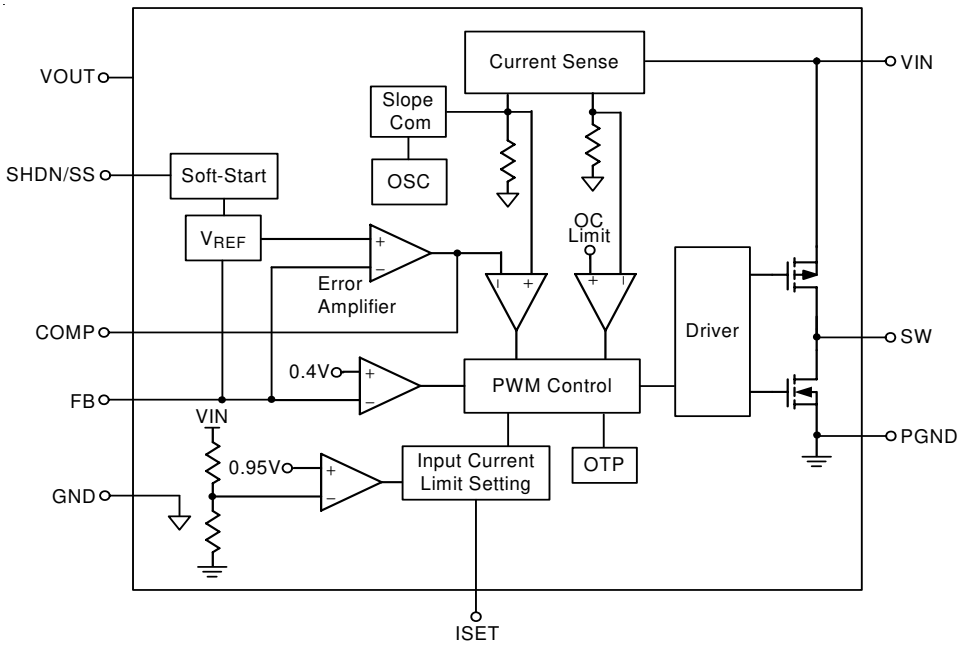
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	SHDN/SS	Shutdown and Soft-Start Control Input. Connect this pin to a supply voltage that is >1.4V to enable the IC and to a supply voltage that is <0.4V to shutdown the IC. An RC network from the shutdown command signal to the pin will provide a soft-start function by the rising time of the FB pin
2, 7	NC	No Internal Connection.
3	GND	Ground. Return the feedback resistive dividers to this ground, which in turn connects to PGND at one point.
4	SW	Internal Power MOSFET Switches Output. Connect this pin to the output inductor.
5, 13 (Exposed Pad)	PGND	Power Ground. The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.
6, 8	VOUT	Output of the Converter. A filter capacitor is placed from V_{OUT} to GND.
9	VIN	Power Input. Internal VCC for the IC. A 10µF ceramic capacitor is recommended as close as to VIN and GND as possible
10	ISET	Average Input Current Limit Setting. Place a resistor and capacitor in parallel from the pin to GND
11	COMP	Error Amplifier Output. The current comparator threshold increases with the control voltage. Connect external compensation elements to the Pin to stabilize the control loop.
12	FB	Feedback Input. Receives the feedback voltage from a resistive divider connected across the output.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- –0.3V to 6V
- Switching Voltage, SW ---------- –0.3V to (V_{IN}+ 0.3V)
- Other I/O Pin Voltages ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-12L 4x3 ---------- 1.667W
- Package Thermal Resistance (Note 2)
  WDFN-12L 4x3, θ_{JA} ---------- 60°C/W
  WDFN-12L 4x3, θ_{JC} ---------- 7.5W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Feedback Reference Voltage		V_{REF}		0.784	0.8	0.816	V
DC Bias Current (PVDD, VDD total)			Active, Not Switching, V_{FB} = 0.75V	--	550	--	μA
			EN =0	--	--	1	μA
Under Voltage Lockout Threshold			V_{IN} Rising	2.3	2.43	2.55	V
			V_{IN} Falling	2.13	2.29	2.43	V
Switching Frequency				1	1.2	1.4	MHz
EN Threshold	Logic-High Voltage	V_{IH}	V_{EN} Rising	1.4	--	--	V
	Logic-Low Voltage	V_{IL}	V_{EN} Falling	--	--	0.4	V
Switch On Resistance, High		R_{PMOS}	I_{SW} = 0.2A	--	230	--	mΩ
Switch On Resistance, Low		R_{NMOS}	I_{SW} = 0.2A	--	230	--	mΩ
Input Average Current Limit		I_{AVG}	R_{LIM} = 25.5kΩ	0.4	0.45	0.5	A
Peak Current Limit		I_{LIM}		1.6	1.9	--	A
Output Voltage Line Regulation			V_{IN} = 3V to 5.5V	--	0.1	1	%/V
Output Voltage Load Regulation			0mA < I_{LOAD} < 1.2A	--	--	1	%

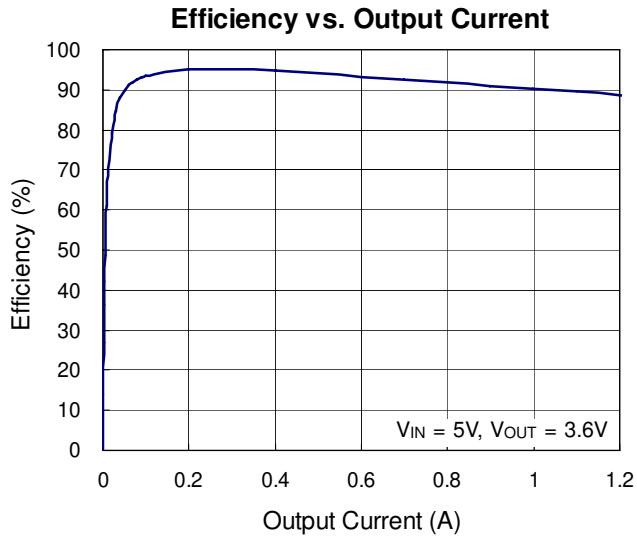
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

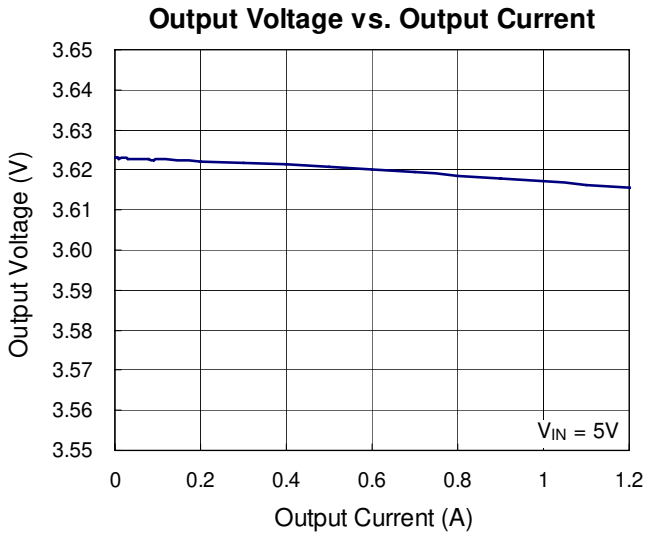
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on 4-layers high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

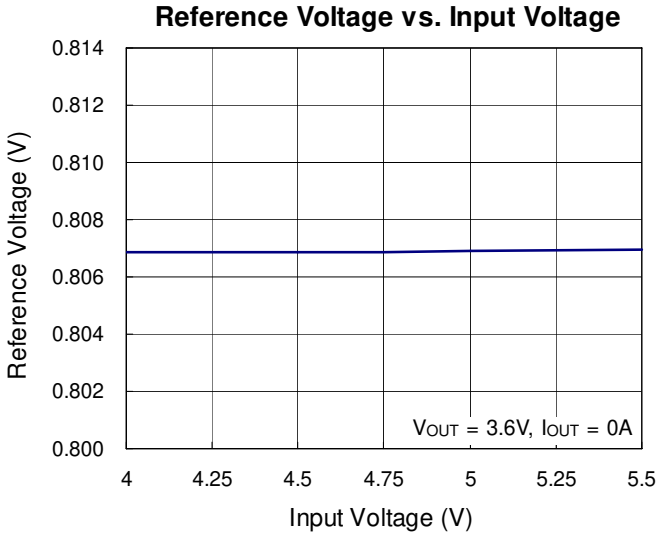
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

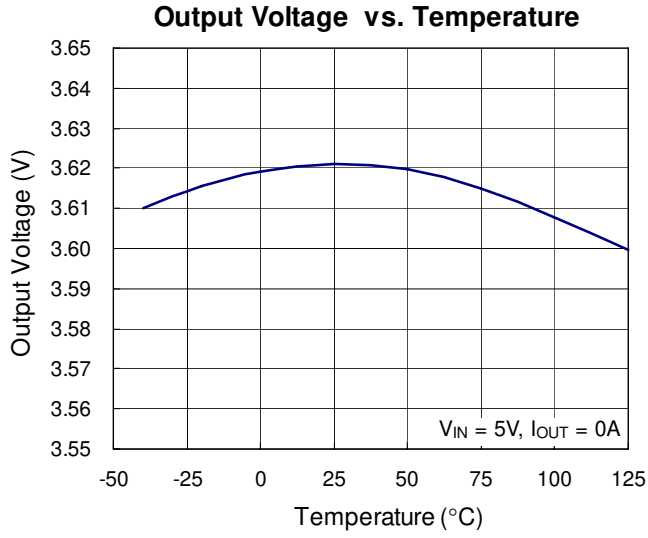
Note 4. The device is not guaranteed to function outside its operating conditions.

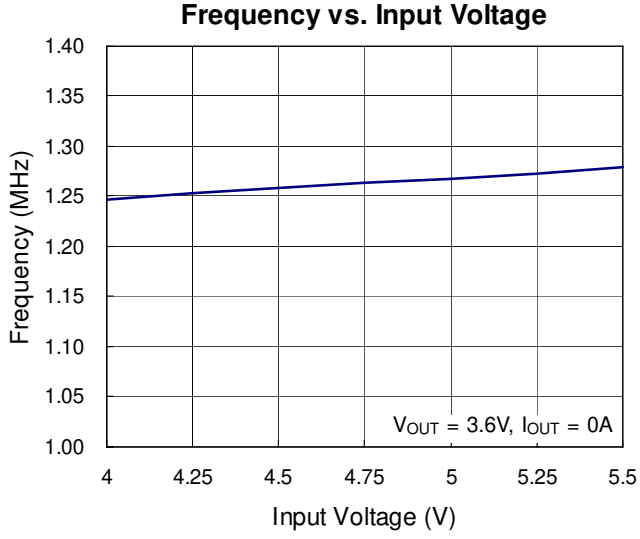
Typical Operating Characteristics

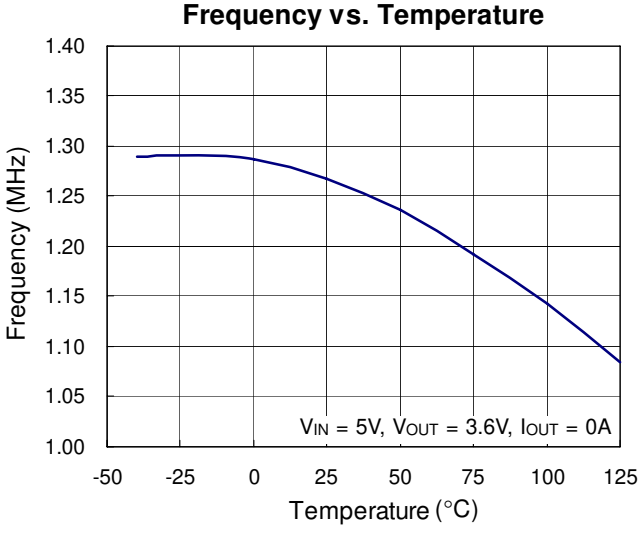




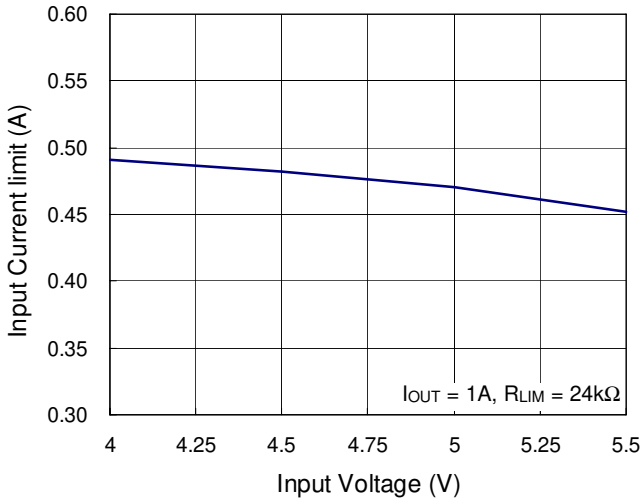




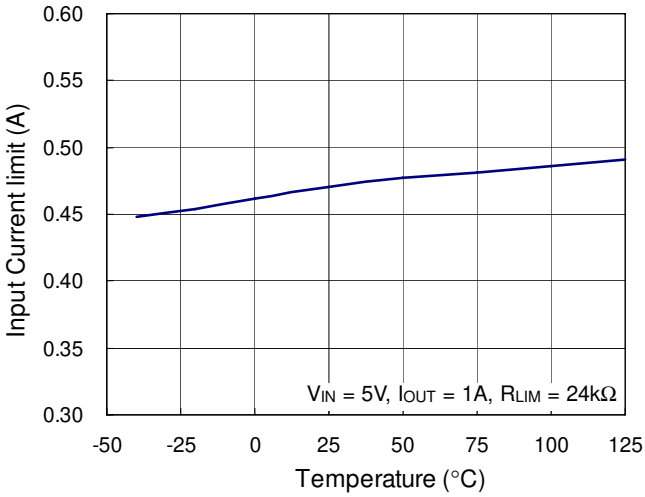




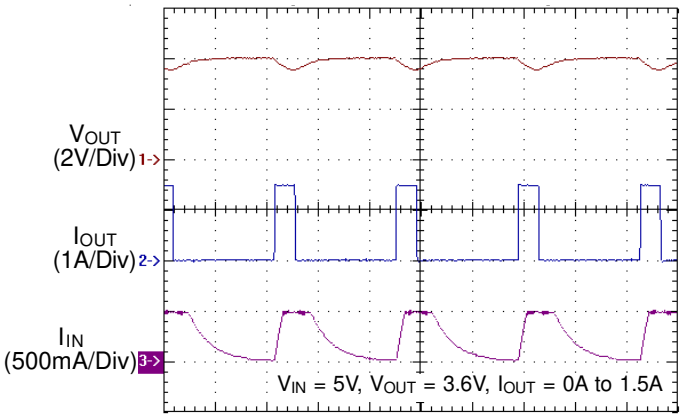
Input Current Limit vs input Voltage



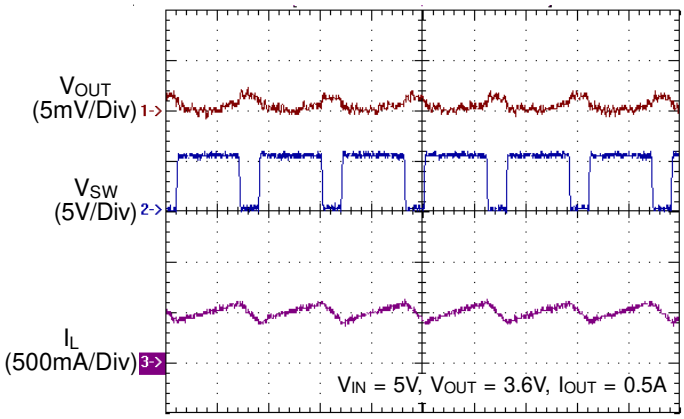
Input Current limit vs Temperature



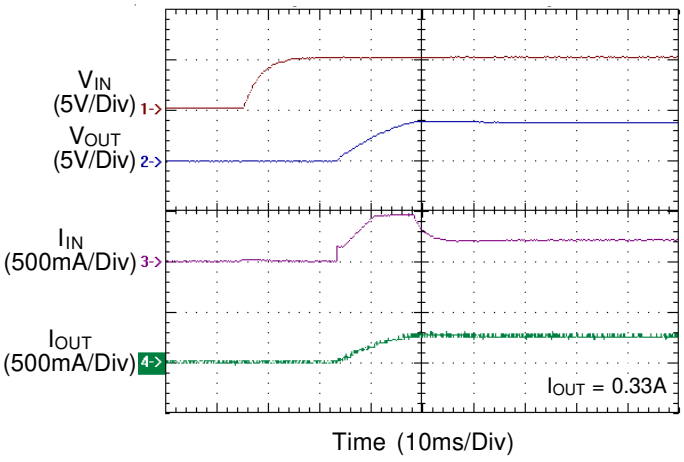
Input Current Limit



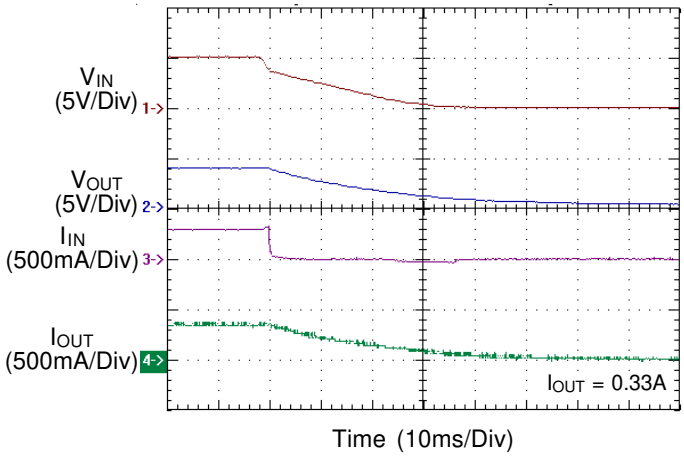
Switching



Power On from V_{IN}



Power Off from V_{IN}



Application Information

Output Voltage Programming

The output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} equals to 0.8V typical.

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

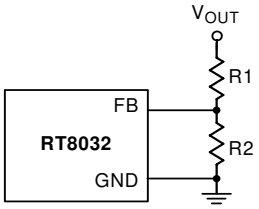


Figure 1. Setting the Output Voltage

Input Average Current Limit Setting

The input current limit circuit is programmed by an external resistor on ISET. This allows the user to program a maximum average input current. For applications such as USB that the current from the bus must be limited, the value of R_{LIM} and C_{C1} can be calculated as following equation.

R_{LIM} = 0.8 / (70 x 10^{-6} x I_{IN} (A))

C_{C1} = 16 x 10^{-6} / R_{LIM}, R_{C1} = 1kΩ

Soft-Start

The soft-start function is combined with shutdown. When the SHDN/SS pin is brought above 1V (typ.), the IC will be enabled. The components of R_{SS} and C_{SS} provide a slow ramping voltage on the SHDN/SS pin to provide a soft-start function.

Input Over Voltage Protection

The RT8032 equips input over voltage protection function. When the input voltage exceeds 6V, the next switching cycle of the IC will be terminated. Once the input voltage is lower than 6V, the IC will enter normal operation again.

100% Duty Cycle Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle and eventually reaching 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the internal P-MOSFET and the inductor.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right]\left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or mollypermalloy cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “ hard” , which means that inductance collapses abruptly when the peak design current is exceeded.

This result in an abrupt increase in inductor ripple current and consequent output voltage ripple.

Do not allow the core to saturate!

Different core materials and shapes will change the size/ current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs. size requirements and any radiated field/EMI requirements.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8032, The maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WDFN-12L 4x3 packages, the thermal resistance θ_{JA} is 60°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (60°C/W) = 1.667W for WDFN-12L 4x3

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT8032 package, the Figure 2 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

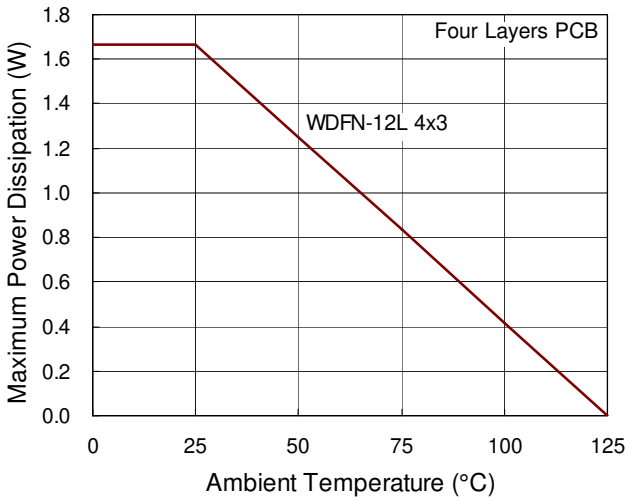


Figure 2. Derating Curves for RT8032 Package

Layout Consideration

Follow the PCB layout guidelines for optimal performance

of RT8032.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- LX node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the LX node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8032.
- Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.
- An example of PCB layout guide is shown in Figure 3 for reference.

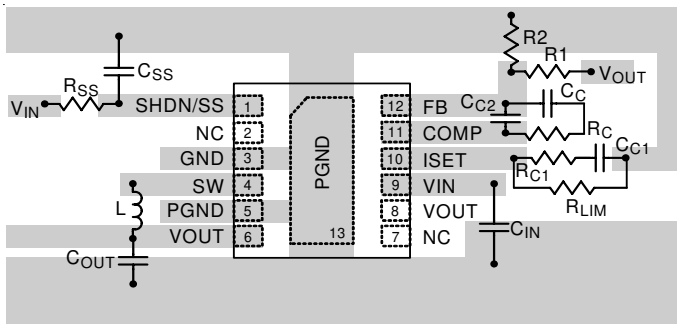


Figure 3. PCB Layout Guide

Recommended component selection for Typical Application

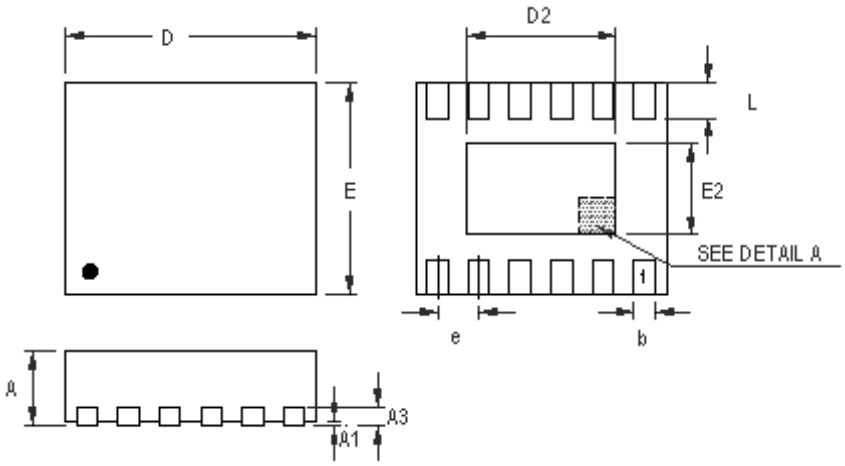
Table 1. Inductors

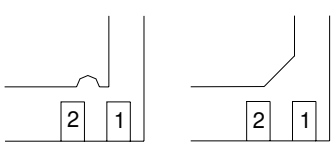
Component Supplier	Series	Inductance (μH)	DCR (mΩ)	Current Rating (mA)	Dimensions (mm)
TAIYO YUDEN	NR3015	4.7	120	1020	3x3x1.5

Table 2. Capacitors for C_{IN} and C_{OUT}

Component Supplier	Part No.	Capacitance (μF)	Case Size
TDK	C2012X5R0J106M	10	0805
TAIYO YUDEN	JMK212BJ106ML	10	0805
VISHAY	592D228X06R3X2T269	2200	1415x7.37x2.2 (mm)

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	3.950	4.050	0.156	0.159
D2	3.250	3.350	0.128	0.132
E	2.950	3.050	0.116	0.120
E2	1.650	1.750	0.065	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 12L DFN 4x3 Package

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