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## 2-Channel 5-Level High-Speed Ultrasound Driver IC

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### Features

- Advanced CMOS Technology
- $\pm 4.75$  to 12.9V Gate Drive Voltage
- 2A Output Source and Sink Current
- 6.5 ns Rise and Fall Time with 1 nF Load
- 10 ns Propagation Delay
- $\pm 2$  ns Matched Delay Times
- 12 Matched Channels
- 1.8V to 3.3V CMOS Logic Interface
- Smart Logic Threshold
- Low-inductance Package

### Applications

- Medical Ultrasound Imaging
- Piezoelectric Transducer Drivers
- Metal Flaw Detection
- Non-destructive Testing (NDT)

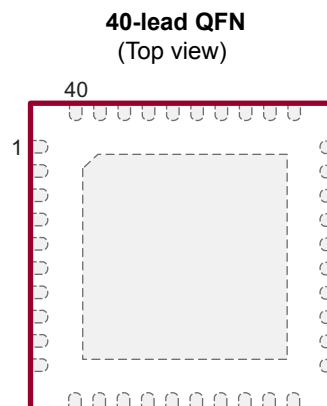
### General Description

The MD1715, paired with Microchip's TC8020, forms a 2-channel five-level high-voltage high-speed transmit pulser chip set. The chip set is designed for medical ultrasound imaging applications but can also be used for metal flaw detection, NDT and piezoelectric transducer drivers.

The MD1715 is a 2-channel logic controller circuit with 12 low-impedance MOSFET gate drivers. There are two sets of control logic inputs—one for Channel A and one for Channel B. Each channel consists of three pairs of MOSFET gate drivers. These drivers are designed to match the drive requirements of Microchip's TC8020.

The TC8020 is the output stage of the pulser, with six pairs of MOSFETs. Each pair consists of a P-channel and an N-channel MOSFET. They are designed to have the same impedance and can provide typical peak currents of  $\pm 3.5$ A at 200V.

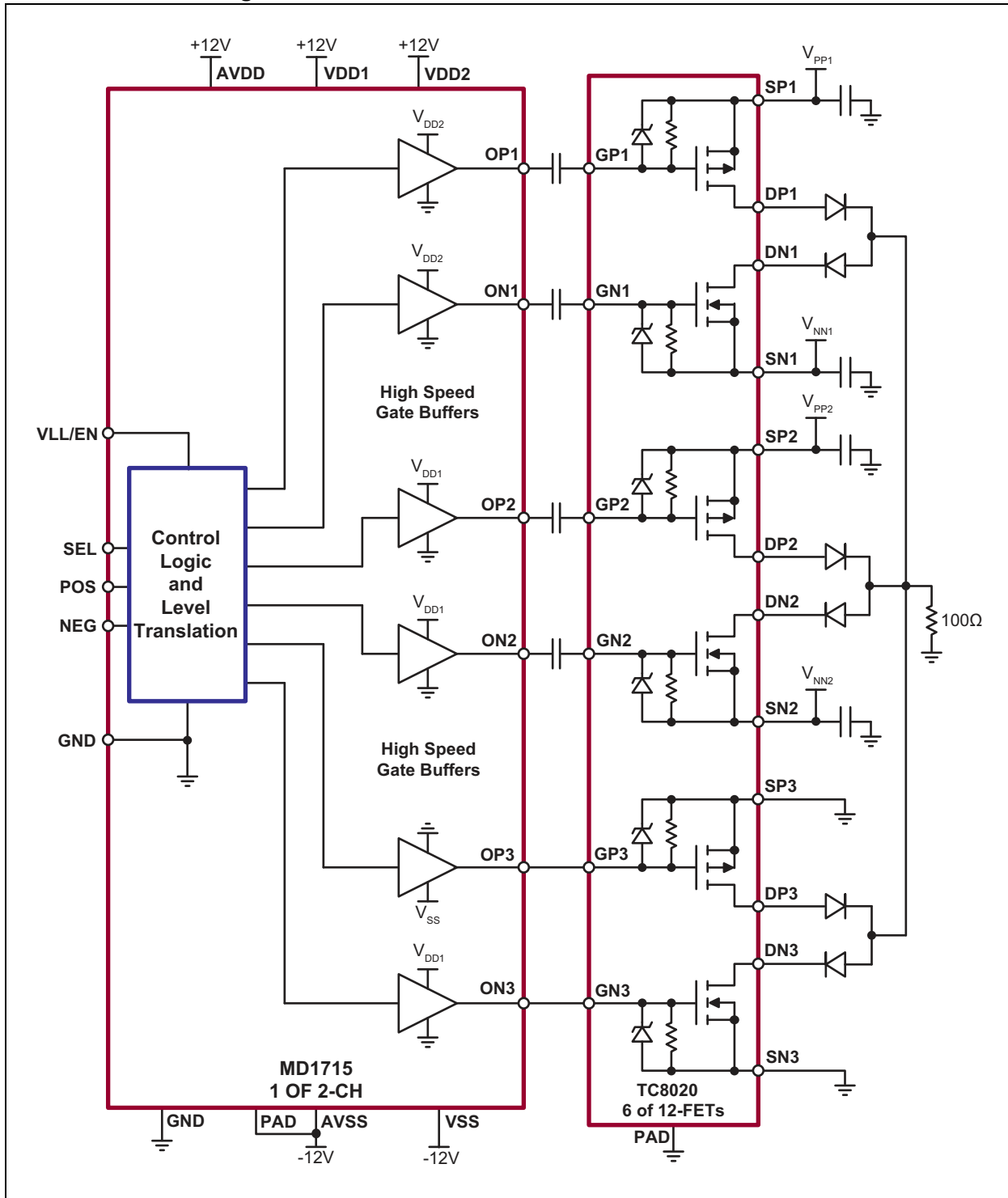
### Package Type



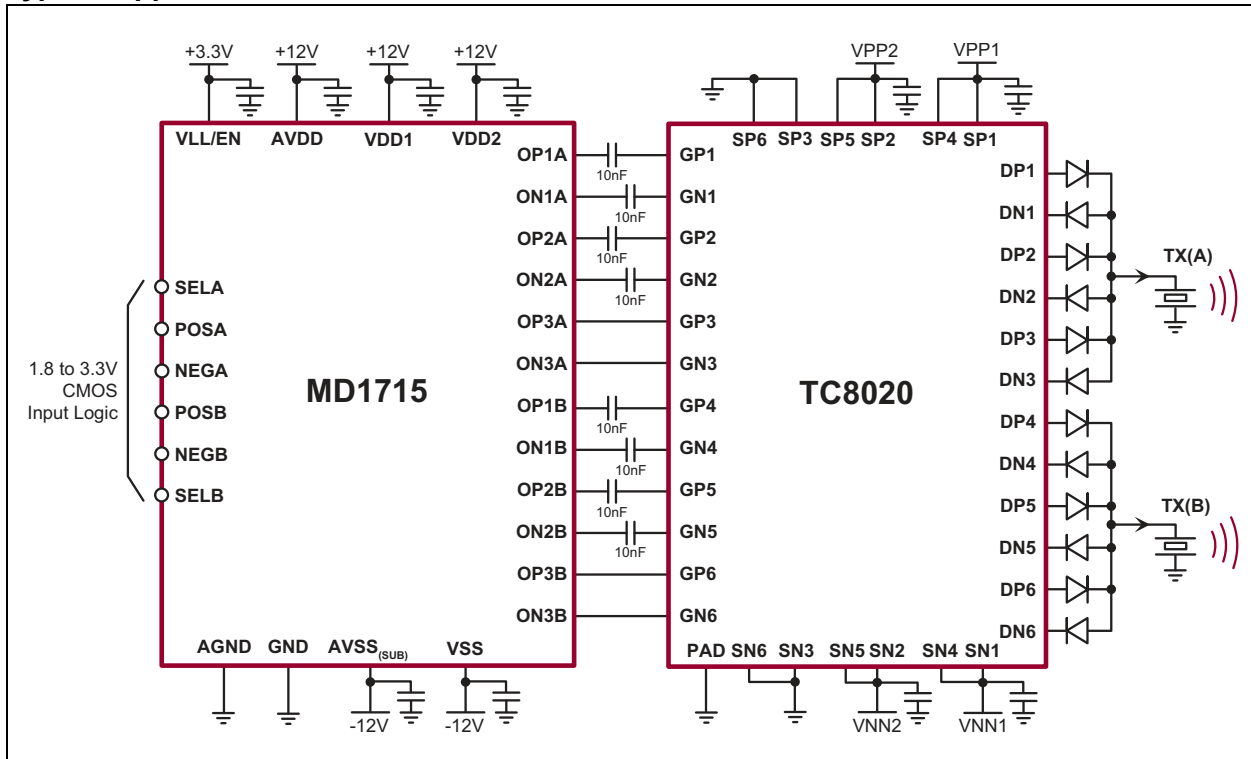
See [Table 2-1](#) for pin information.

# MD1715

## Functional Block Diagram



## Typical Application Circuit



# MD1715

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

GND and AGND, Ground	0V
Logic Input Pin, $V_{LL}$	-0.5V to +5.5V
Positive Gate Drive Supply, $AV_{DD}$ , $V_{DD1}$ , $V_{DD2}$	-0.5V to +14.5V
Negative Gate Drive Supply, $AV_{SS}$ , $V_{SS}$	-14.5V to +0.5V
Operating Junction Temperature, $T_J$	0°C to +125°C
Storage Temperature, $T_S$	-65°C to +150°C
Power Dissipation:	
40-lead QFN (Note 1)	1.3W

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note 1:** 1 oz. four-layer 3 inches x 4 inches PCB

### OPERATING SUPPLY VOLTAGES AND CURRENTS

**Electrical Specifications for Operating Supply Currents:** Over operating conditions unless otherwise specified,  $V_{LL} = 3.3V$ ,  $AV_{DD} = V_{DD1} = V_{DD2} = +12V$ ,  $AV_{SS} = V_{SS} = -12V$ ,  $T_A = 25^\circ C$

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply	$V_{LL}$	1.8	3.3	3.6	V	
Positive Analog Supply	$AV_{DD}$	8	—	12.9	V	$AV_{DD} \geq (V_{DD1} \text{ or } V_{DD2})$
Positive Gate Drive Supply	$V_{DD2}$ , $V_{DD1}$	4.75	—	12.9	V	
Negative Gate Drive Supply	$AV_{SS}$ , $V_{SS}$	-12.9	—	-4.75	V	
Logic Reference Current	$I_{VLL}$	—	10	—	$\mu A$	$V_{LL} = 3.3V$
$AV_{DD}$ Power-down Current	$I_{AVDDQ}$	—	0.4	—	mA	EN = 0, all inputs low
$V_{SS}$ Power-down Current	$I_{VSSQ}$	—	0.1	—	mA	
$V_{DD1}$ Power-down Current	$I_{VDD1Q}$	—	10	25	$\mu A$	EN = 0, all inputs low
$V_{DD2}$ Power-down Current	$I_{VDD2Q}$	—	10	25	$\mu A$	
$AV_{DD}$ Power-up Current	$I_{AVDDEN}$	—	2	3	mA	EN = 1, all inputs low
$V_{SS}$ Power-up Current	$I_{VSSEN}$	—	0.7	1	mA	
$V_{DD1}$ Power-up Current	$I_{VDD1EN}$	—	10	—	$\mu A$	EN = 1, all inputs low
$V_{DD2}$ Power-up Current	$I_{VDD2EN}$	—	10	—	$\mu A$	
$AV_{DD}$ CW 5 MHz Current	$I_{AVDDCW}$	—	10	—	mA	A and B Channels on at 5 MHz, no load, $V_{DD1} = 12V$ , $V_{DD2} = 5V$
$V_{SS}$ CW 5 MHz Current	$I_{VSSCW}$	—	5	—	mA	
$V_{DD1}$ CW 5 MHz Current	$I_{VDD1CW}$	—	25	—	mA	A and B Channels on at 5 MHz, no load, $V_{DD1} = 5V$ , $V_{DD2} = 12V$
$V_{DD2}$ CW 5 MHz Current	$I_{VDD2CW}$	—	25	—	mA	A and B Channels on at 5 MHz, no load, $V_{DD1} = 12V$ , $V_{DD2} = 5V$

## DC ELECTRICAL CHARACTERISTICS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions	
<b>P-CHANNEL AND N-CHANNEL GATE DRIVER OUTPUTS</b>							
Output Sink Resistance	P-Channel	$R_{SINK}$	—	5	6	$\Omega$	$I_{SINK} = 100 \text{ mA}$
	N-Channel		—	5	6	$\Omega$	$I_{SINK} = 100 \text{ mA}$
Output Source Resistance	P-Channel	$R_{SOURCE}$	—	5	6	$\Omega$	$I_{SOURCE} = 100 \text{ mA}$
	N-Channel		—	5	6	$\Omega$	$I_{SOURCE} = 100 \text{ mA}$
Peak Output Sink Current	P-Channel	$I_{SINK}$	1.7	2	—	A	
	N-Channel		1.7	2	—	A	
Peak Output Source Current	P-Channel	$I_{SOURCE}$	1.7	2	—	A	
	N-Channel		1.7	2	—	A	
<b>LOGIC INPUTS</b>							
Chip Disable Low Voltage	$V_{ENL}$	0	—	0.3	V	VLL/EN is a dual function pin	
Input Logic High Voltage	$V_{IH}$	$0.8 V_{LL}$	—	$V_{LL}$	V		
Input Logic Low Voltage	$V_{IL}$	0	—	$0.2 V_{LL}$	V		
Input Logic High Current	$I_{IH}$	—	—	1	$\mu\text{A}$		
Input Logic Low Current	$I_{IL}$	-1	—	—	$\mu\text{A}$		

## AC ELECTRICAL CHARACTERISTICS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>Electrical Specifications:</b> Over operating conditions unless otherwise specified, $V_{LL} = 3.3\text{V}$ , $AV_{DD} = V_{DD1} = V_{DD2} = +12\text{V}$ , $AV_{SS} = V_{SS} = -12\text{V}$ , $T_A = 25^\circ\text{C}$						
Input Rise and Fall Time	$t_{irf}$	—	—	10	ns	Logic input edge speed requirement
Output Rise Time	$t_r$	—	6.5	—	ns	1 nF load, input signal rise/fall time 2 ns ( <a href="#">Timing Waveforms</a> )
Output Fall Time	$t_f$	—	6.5	—	ns	
Output Rise Delay	$t_{dr}$	—	10	—	ns	
Output Fall Delay	$t_{df}$	—	10	—	ns	
Rise and Fall Time Matching	$ t_r - t_f $	—	1	—	—	For each channel
Propagation Delay Matching	$ t_{dr} - t_{df} $	—	1	—	—	
Delay Time Matching	$t_{dm}$	—	$\pm 2$	—	ns	Channel to channel and device to device
Output Jitter	$\Delta t_j$	—	20	—	ps	$V_{DD} = 10\text{V}$
IC Enable Time	$t_{EN\_ON}$	—	25	50	$\mu\text{s}$	
IC Disable Time	$t_{EN\_OFF}$	—	0.5	2	$\mu\text{s}$	
Second Harmonic Distortion	HD2	-40	—	—	dB	

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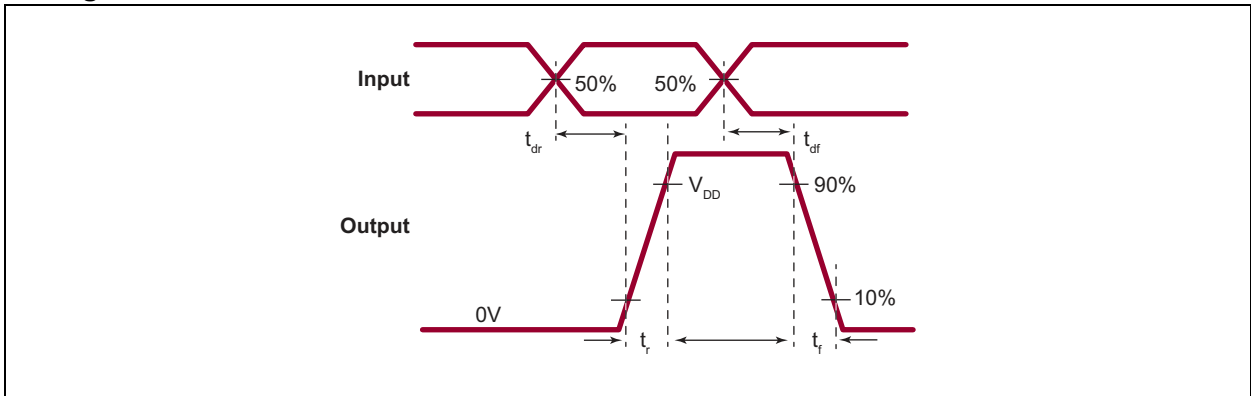
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## TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>TEMPERATURE RANGE</b>						
Operating Junction Temperature	$T_J$	-0	—	+125	°C	
Storage Temperature	$T_S$	-65	—	+150	°C	
<b>PACKAGE THERMAL RESISTANCE</b>						
40-lead QFN	$\theta_{JA}$	—	24	—	°C/W	

## Timing Waveforms



# MD1715

## 2.0 PIN DESCRIPTION

The details on the pins of MD1715 are listed on [Table 2-1](#). See [Package Type](#) for the location of pins.

**TABLE 2-1: PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	SELA	SEL input logic control for Channel A. See <a href="#">Table 3-1</a> .
2	POSA	POS input logic control for Channel A. See <a href="#">Table 3-1</a> .
3	NEGA	NEG input logic control for Channel A. See <a href="#">Table 3-1</a> .
4	VLL/EN	Logic High reference voltage and chip enable input
5	AVDD	Positive supply voltage of analog circuitry. AVDD should be at the same or higher potential than the highest voltages of VDD1 or VDD2.
6	AGND	Digital ground
7	AVSS	Negative supply voltage of analog circuitry and connection of IC substrate. Should be at the same potential as VSS.
8	SELB	SEL input logic control for Channel B. See <a href="#">Table 3-2</a> .
9	POSB	POS input logic control for Channel B. See <a href="#">Table 3-2</a> .
10	NEGB	NEG input logic control for Channel B. See <a href="#">Table 3-2</a> .
11	VDD2	Positive supply voltage of the gate drivers for the output stages OP1 and ON1 in Channel A and Channel B. VDD2 can be at a different voltage than VDD1.
12	OP1B	First output P-channel gate driver for Channel B
13	VDD1	Positive supply voltage of the gate drivers for the output stages OP2, ON2 and ON3 in Channel A and Channel B. VDD1 can be at a different voltage than VDD2.
14	GND	Power ground
15	OP2B	Second output P-channel gate driver for Channel B
16	VDD2	Positive supply voltage of the gate drivers for the output stages OP1 and ON1 in Channel A and Channel B. VDD2 can be at a different voltage than VDD1.
17	ON1B	First output N-channel gate driver for Channel B
18	GND	Power ground
19	VDD1	Positive supply voltage of the gate drivers for the output stages OP2, ON2 and ON3 in Channel A and Channel B. VDD1 can be at a different voltage than VDD2.
20	ON2B	Second output N-channel gate driver for Channel B
21	GND	Power ground
22	ON3B	Damping output N-channel gate driver for Channel B
23	VSS	Negative supply voltage for the gate drive of OP3. Should be the same voltage as AVSS.
24	OP3B	Damping output P-channel gate driver for Channel B
25	GND	Power ground
26	VSS	Negative supply voltage for gate drive of OP3. Should be the same voltage as AVSS.
27	OP3A	Damping output P-channel gate driver for Channel A
28	GND	Power ground



**TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)**

Pin Number	Pin Name	Description
29	GND	Power ground
30	ON3A	Damping output N-channel gate driver for Channel A
31	ON2A	Second output N-channel gate driver for Channel A
32	VDD1	Positive supply voltage of the gate drivers for the output stages OP2, ON2 and ON3 in Channel A and Channel B. VDD1 can be at a different voltage than VDD2.
33	GND	Power ground
34	ON1A	First output N-channel gate driver for Channel A
35	VDD2	Positive supply voltage of the gate drivers for the output stages OP1 and ON1 in Channel A and Channel B. VDD2 can be at a different voltage than VDD1.
36	OP2A	Second output P-channel gate driver for Channel A
37	GND	Power ground
38	VDD1	Positive supply voltage of the gate drivers for the output stages OP2, ON2 and ON3 in Channel A and Channel B. VDD1 can be at a different voltage than VDD2.
39	OP1A	First output P-channel gate driver for Channel A
40	VDD2	Positive supply voltage of the gate drivers for the output stages OP1 and ON1 in Channel A and Channel B. VDD2 can be at a different voltage than VDD1.
Center Pad	Thermal Pad	IC substrate, must connect to AVSS externally

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## 3.0 FUNCTIONAL DESCRIPTION

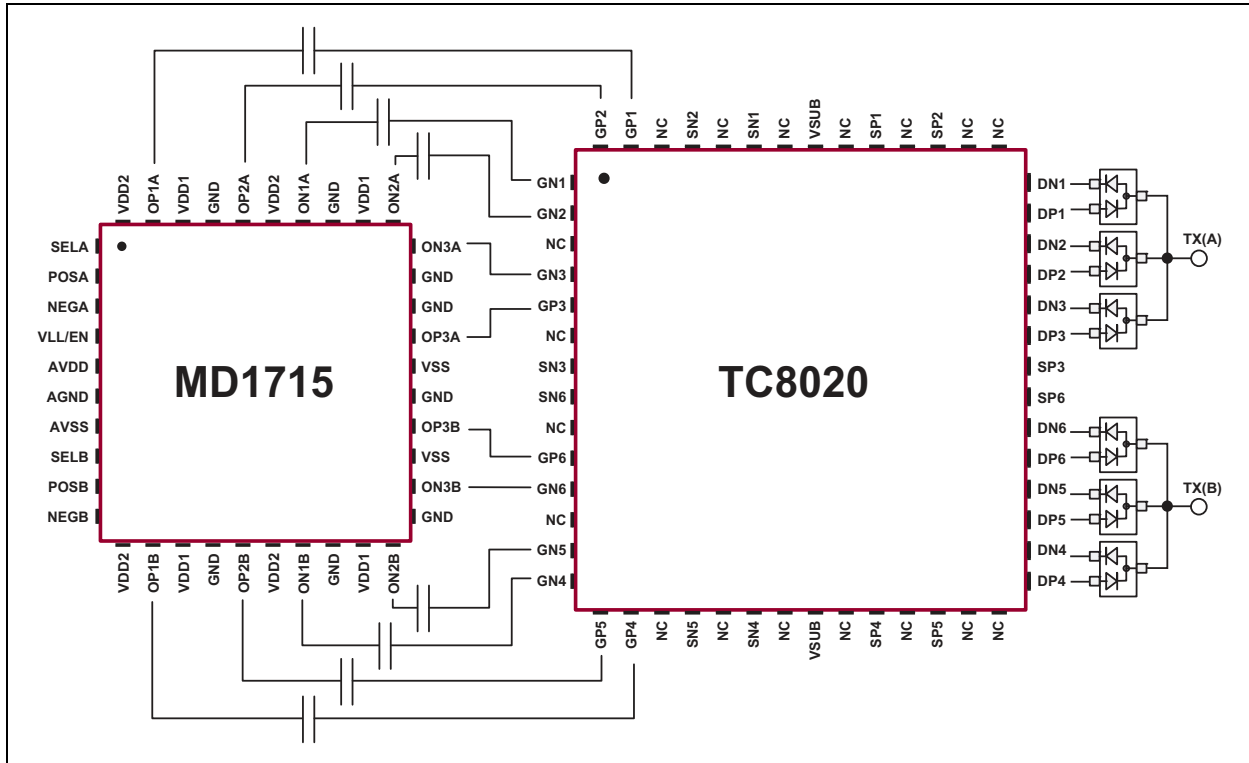


FIGURE 3-1: Circuit Pin Layout.

**TABLE 3-1: TRUTH FUNCTION TABLE FOR CHANNEL A**

EN	Logic Inputs A			SP1 to DP1	SN1 to DN1	SP2 to DP2	SN2 to DN2	SP3 to DP3	SN3 to DN3
	SELA	POSA	NEGA						
1	0	0	0	OFF	OFF	OFF	OFF	<b>ON</b>	<b>ON</b>
1	0	0	1	OFF	OFF	OFF	<b>ON</b>	OFF	OFF
1	0	1	0	OFF	OFF	<b>ON</b>	OFF	OFF	OFF
1	0	1	1	OFF	OFF	OFF	OFF	OFF	OFF
1	1	0	0	OFF	OFF	OFF	OFF	<b>ON</b>	<b>ON</b>
1	1	0	1	OFF	<b>ON</b>	OFF	OFF	OFF	OFF
1	1	1	0	<b>ON</b>	OFF	OFF	OFF	OFF	OFF
1	1	1	1	OFF	OFF	OFF	OFF	OFF	OFF

**TABLE 3-2: TRUTH FUNCTION TABLE FOR CHANNEL B**

EN	Logic Inputs B			SP4 to DP4	SN4 to DN4	SP5 to DP5	SN5 to DN5	SP6 to DP6	SN6 to DN6
	SELB	POSB	NEGB						
1	0	0	0	OFF	OFF	OFF	OFF	<b>ON</b>	<b>ON</b>
1	0	0	1	OFF	OFF	OFF	<b>ON</b>	OFF	OFF
1	0	1	0	OFF	OFF	<b>ON</b>	OFF	OFF	OFF
1	0	1	1	OFF	OFF	OFF	OFF	OFF	OFF
1	1	0	0	OFF	OFF	OFF	OFF	<b>ON</b>	<b>ON</b>
1	1	0	1	OFF	<b>ON</b>	OFF	OFF	OFF	OFF
1	1	1	0	<b>ON</b>	OFF	OFF	OFF	OFF	OFF
1	1	1	1	OFF	OFF	OFF	OFF	OFF	OFF
0	X	X	X	OFF	OFF	OFF	OFF	<b>ON</b>	<b>ON</b>
0→1	0	0	0	EN transitions from low to high or high to low should occur at all logic inputs low.					
1→0	0	0	0						

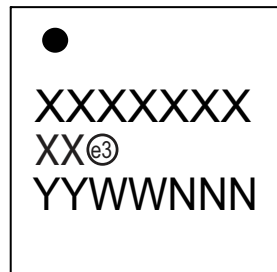
# MD1715

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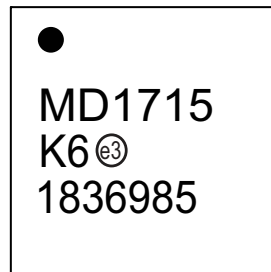
## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

40-lead QFN

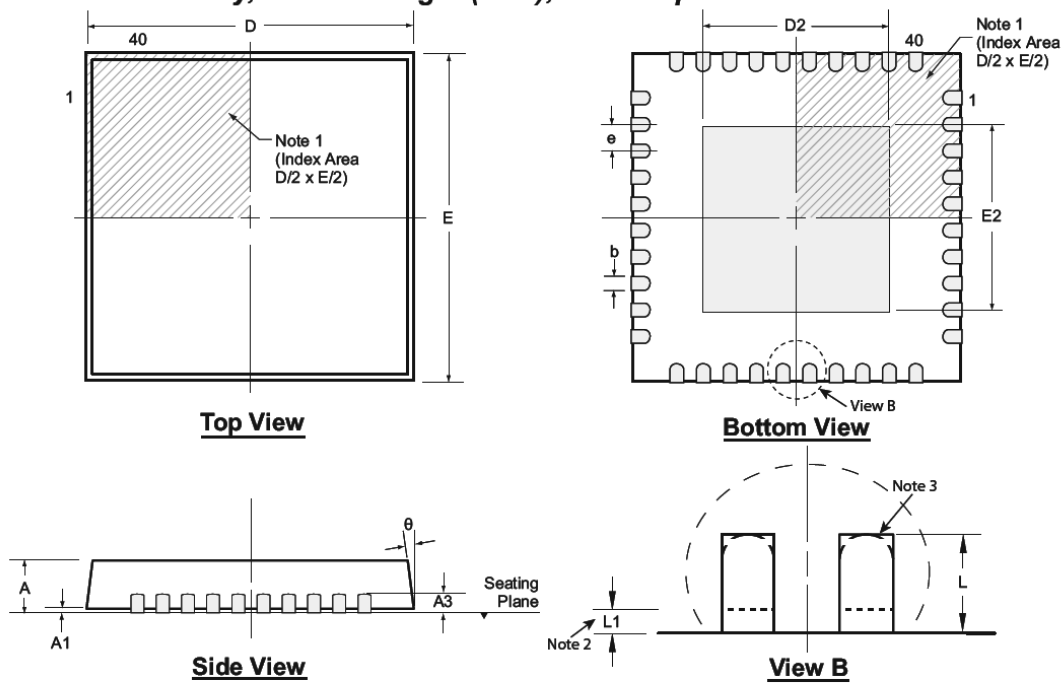


Example



<b>Legend:</b>	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC <sup>®</sup> designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.	

## 40-Lead QFN Package Outline (K6) 6.00x6.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at [www.microchip.com/packaging](http://www.microchip.com/packaging).

**Notes:**

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier, an embedded metal marker, or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol	A	A1	A3	b	D	D2	E	E2	e	L	L1	$\theta^\circ$	
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	5.85*	1.05	5.85*	1.05	0.50 BSC	0.30 <sup>†</sup>	0.00	0
	NOM	0.90	0.02		0.25	6.00	-	6.00	-		0.40 <sup>†</sup>	-	-
	MAX	1.00	0.05		0.30	6.15*	4.45	6.15*	4.45		0.50 <sup>†</sup>	0.15	14

JEDEC Registration MO-220, Variation VJJD-6, Issue K, June 2006.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

# MD1715

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NOTES:

## APPENDIX A: REVISION HISTORY

### Revision A (January 2018)

- Converted Supertex Doc# DSFP-MD1715 to Microchip DS20005921A
- Changed the package marking format
- Changed the quantity of the 40-lead VQFN K6 M935 package from 2000/Reel to 3000/Reel
- Made minor text changes throughout the document

# MD1715

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>XX</u>	-	<u>X</u>	-	<u>X</u>
Device	Package Options		Environmental		Media Type
Device:	MD1715	=	2-Channel 5-Level High-Speed Ultrasound Driver IC		
Package:	K6	=	40-lead VQFN		
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Types:	(blank)	=	490/Tray for a K6 Package		
	M935	=	3000/Reel for a K6 Package		

**Examples:**

a) MD1715K6-G: 2-Channel 5-Level High-Speed Ultrasound Driver IC, 40-lead VQFN, 490/Tray

b) MD1715K6-G-M935: 2-Channel 5-Level High-Speed Ultrasound Driver IC, 40-lead VQFN, 3000/Reel



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